

DESCRIPTION

The HY51V16160B is the new generation and fast dynamic RAM organized 1,048,576 x 16-bit. The HY51V16160B utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY51V16160B to be packaged in a standard 42/42pin plastic SOJ, 44/50 pin TSOP-II and Reverse TSOP-II.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of $3.3V \pm 10\%$ tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 1.6mW (SL-part)
Max. CMOS standby 0.7mW (SL-part)
3.6mW
Max. TTL standby 7.2mW
Max. operating

Speed	Power
60	324mW
70	288mW
80	252mW

- Single power supply of $3.3V \pm 10\%$
- TTL compatible inputs and outputs
- Fast access and cycle time

Speed	trAC	tCAC	tpc
60	60ns	15ns	40ns
70	70ns	20ns	45ns
80	80ns	20ns	50ns

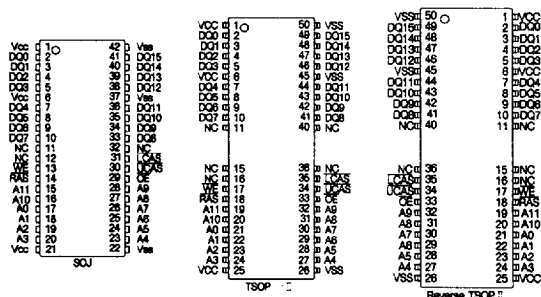
- Fast page mode operation
- 2CAS inputs for upper and lower byte control
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh and Self Refresh capability
- 4096 refresh cycles / 256ms (SL-part)
4096 refresh cycles / 64ms

PIN DESCRIPTION

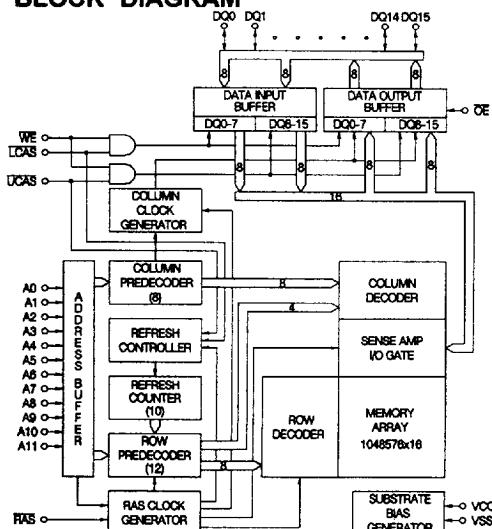
RAS	Row Address Strobe
LCAS, UCAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A11*	Address input
DQ0-DQ15	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

*A8-A11 are applied to row address input only

PIN CONNECTION



BLOCK DIAGRAM



This document is a general product description and is subject to change without notice. Hyundai Electronics does not assume any responsibility for use of circuits described. No patent licences are implied.

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	- 55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	- 1.0 to 4.6	V
VCC	Voltage on VCC Relative to Vss	- 1.0 to 4.6	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	1.0	W
TSOLDER	Soldering Temperature • Time	260 • 10	°C • sec

NOTE: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	3.0	3.3	3.6	V
VSS	Ground	0	0	0	V
VIH	Input High Voltage	2.0	-	VCC+0.3	V
VIL	Input Low Voltage	- 0.3	-	0.8	V

NOTE: All voltages are referenced to VSS.

DC CHARACTERISTICS

(TA=0°C to 70°C, VCC=3.3V±10%, VSS=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC+0.3V All other pins not under test=VSS		-10	10	μA	
ILO	Output Leakage Current (High impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	trc = trc (min.)	60 70 80	- - -	90 80 70	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS	SL-part	- -	2 1	mA	
ICC3	VCC Supply Current, RAS-only refresh	trc = trc (min.)	60 70 80	- - -	90 80 70	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tpc = tpc (min.)	60 70 80	- - -	90 80 70	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	SL-part	- -	1 200	mA μA	5
ICC6	VCC Supply Current, CAS-before- RAS Refresh	trc = trc (min.)	60 70 80	- - -	90 80 70	mA	1,3
ICC7	VCC Supply Current, Battery Back up (SL-part only)	trc = 6.25ms, CAS = CBR cycling or 0.2V OE & WE = VCC-0.2V or 0.2V A0-A11 = VCC-0.2V or 0.2V DQ0-DQ15 = 0.2V, VCC-0.2V or open	trAS ≤ 300ns trAS ≤ 1μs	- -	350 450	μA	4,5
ICC8	VCC Supply Current, Self Refresh (SL-part only)	RAS & CAS ≤ 0.2V other pins same as ICC7		-	450	μA	5
VOL	Output Low Voltage	IOL = 2.0mA		-	0.4	V	
VOH	Output High Voltage	IOH = -2.0mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4 and ICC6 depend on cycle rates.
2. ICC1, ICC3, ICC4 and ICC6 are dependent on output loading. Specified values are obtained with the output open.
3. ICC is specified as an average current. ICC1, ICC3, ICC6, Address can be changed maximum two times while RAS = VIL. In ICC4, Address can be changed maximum once while CAS = VIH.
4. trAS(max.)=1μs is only applied to refresh of battery backup but trAS(max.)=10μs is applied to normal functional operation .
5. ICC5(max.) = 200 μA and ICC7 and ICC8 are applied to SL-parts only.

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 10%, Vss=0V, unless otherwise noted.) NOTE : 3,7,8

#	SYMBOL	PARAMETER	HY51V16160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	155	-	170	-	200	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	45	-	50	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	80	-	80	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	8,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	8,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	8,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	45	ns	8,15
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	8
10	tOFF	Output Buffer Turn-off Delay from CAS	0	15	0	15	0	15	ns	11
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	6
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse width	15	10K	15	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	15	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	15
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	20
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	15
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	15
26	tRAL	Column Address to RAS Lead Time	30	-	35	-	40	-	ns	
27	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	15
28	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	13,15
29	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	15
30	tWCH	Write Command Hold Time	15	-	15	-	15	-	ns	15
31	tWP	Write Command Pulse Width	10	-	10	-	10	-	ns	
32	tRWL	Write Command to RAS Lead Time	20	-	20	-	20	-	ns	
33	tCWL	Write Command to CAS Lead Time	20	-	20	-	20	-	ns	22
34	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	15,25
35	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	15,25
36	tREF	Refresh Period (4096 cycles)	-	64	-	64	-	64	ms	18
		SL-part	-	256	-	256	-	256	ms	
37	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	15,16
38	tCWD	CAS to WE Delay Time	45	-	50	-	50	-	ns	16
39	tRWD	RAS to WE Delay Time	85	-	95	-	105	-	ns	16
40	tAWD	Column Address to WE Delay Time	55	-	60	-	65	-	ns	16

AC CHARACTERISTICS

(continued)

#	SYMBOL	PARAMETER	HY51V16160BJC/TC/RC/SLJC/SLTC/SLRC						UNIT	NOTE
			- 60		- 70		- 80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
41	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	15
42	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	15
43	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	15
44	tCPT	CAS Precharge Time (CBR Counter Test)	30	-	35	-	40	-	ns	20
45	tROH	RAS Hold Time Referenced to OE	10	-	10	-	10	-	ns	
46	tOEA	OE Access Time	-	15	-	20	-	20	ns	
47	tOED	OE to Data Delay	15	-	20	-	20	-	ns	
48	tOEZ	Output Buffer Turn Off Delay Time	0	15	0	15	0	15	ns	15
49	tOEH	OE Command Hold Time	15	-	20	-	20	-	ns	
50	tCPWD	WE Delay Time from CAS Precharge	55	-	65	-	75	-	ns	16
51	tRHCP	RAS Hold Time from CAS Precharge	40	-	40	-	50	-	ns	
52	tWRP	WE to RAS Precharge Time(CBR Cycle)	10	-	10	-	10	-	ns	
53	tWRH	WE to RAS Hold Time(CBR Cycle)	10	-	10	-	10	-	ns	
54	tRASS	RAS Pulse Width (Self Refresh Cycle)	100	-	100	-	100	-	μs	
55	tRPS	RAS Precharge Time (Self Refresh Cycle)	110	-	130	-	150	-	ns	
56	tCHS	CAS Hold Time (Self Refresh Cycle)	50	-	50	-	50	-	ns	

NOTE:

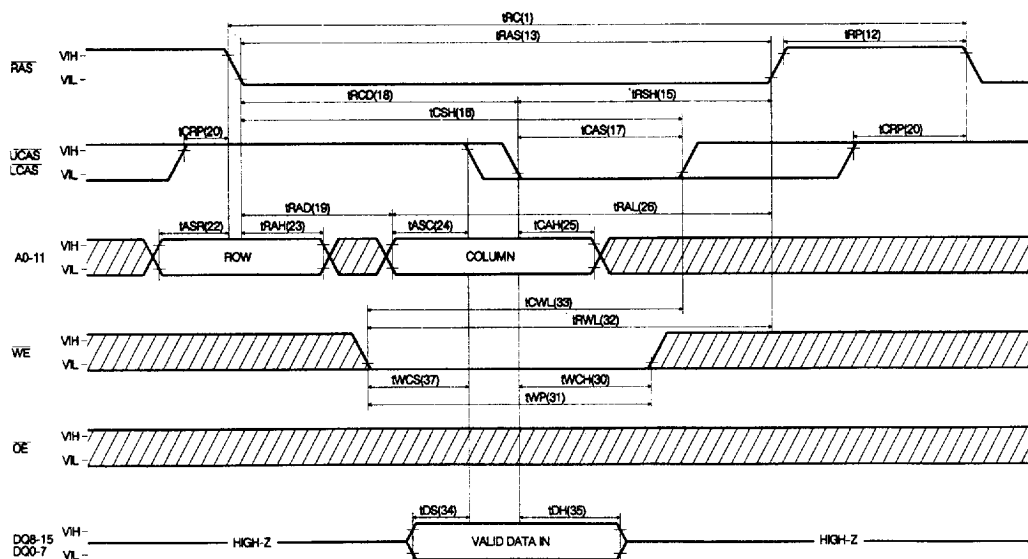
1. Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
2. All voltages referenced to VSS.
3. An initial pause of 200 μ s is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles are required.
4. Address can be changed once or less while $\overline{\text{RAS}} = \text{VIL}$. In case of changed once or less during a Fast Page Mode cycle (tPC).
5. AC measurements assume tT 3ns.
6. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between VIH and VIL.
7. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (TA = 0 to 70°C) is assured.
8. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 1TTL load and 100pF.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met.
tRCD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met.
tRAD(max.) is specified as a reference point only. If tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tOFF(max.), tREZ(max.), tWEZ(max.) and tOEZ(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. The tCRP requirement should be applicable for $\overline{\text{RAS}}$ / $\overline{\text{CAS}}$ cycles preceded by any cycle.
13. Either tRCH or tRRH must be satisfied for a read cycle.
14. Parameter tWP is applicable for a late write cycle. For early write cycle., tWCH must be met.
15. These parameters are referenced to $\overline{\text{UCAS}}$ or $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in Read-Modify-Write cycles.
16. twCS, tRWD, tCWD, tAWD, and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If twCS $\geq$ twCS(min.), the cycle is an early write cycle and the data output pin will remain open circuit(high impedance) through the entire cycle. If tRWD $\geq$ tRWD(min.), tCWD $\geq$ tCWD(min.), tAWD $\geq$ tAWD(min.), and tCPWD $\geq$ tCPWD(min.) (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of condition of the data out (at access time) is interminated.
17. If $\overline{\text{RAS}}$ goes to high before $\overline{\text{CAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{CAS}}$ high going. If $\overline{\text{CAS}}$ goes to high before $\overline{\text{RAS}}$ high going, the open circuit condition of the output is achieved by $\overline{\text{RAS}}$ high going.
18. 4096 cycles of Burst Refresh must be executed within 64ms after exiting Self Refresh.
19. tASC, tCAH are reference to the earlier $\overline{\text{CAS}}$ falling edge.
20. tCP and tCPT are measured when both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ are high state.
21. tCWD is referenced to the later $\overline{\text{CAS}}$ falling edge at word read-modify-write cycle.
22. tCWL must be satisfied by both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ for 16-bits access cycles.
23. tCSR is referenced to earlier $\overline{\text{CAS}}$ falling low before $\overline{\text{RAS}}$ transition low.
24. tCHR is referenced to the later $\overline{\text{CAS}}$ rising high after $\overline{\text{RAS}}$ transition low.
25. tDS, tDH is independently specified for lower byte DQ(0-7), upper byte DQ(8-15).

CAPACITANCE

(TA=25°C, Vcc=3.3V $\pm$ 10%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A11)	-	5	pF
CIN2	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	-	7	pF
CDQ	Data Input/Output Capacitance (DQ0-DQ15)	-	7	pF

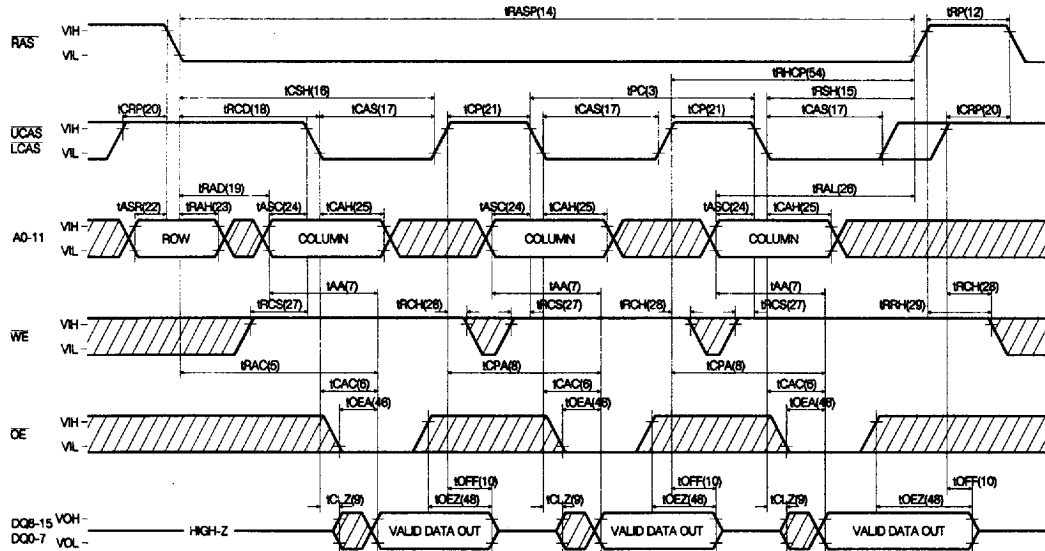
READ CYCLE



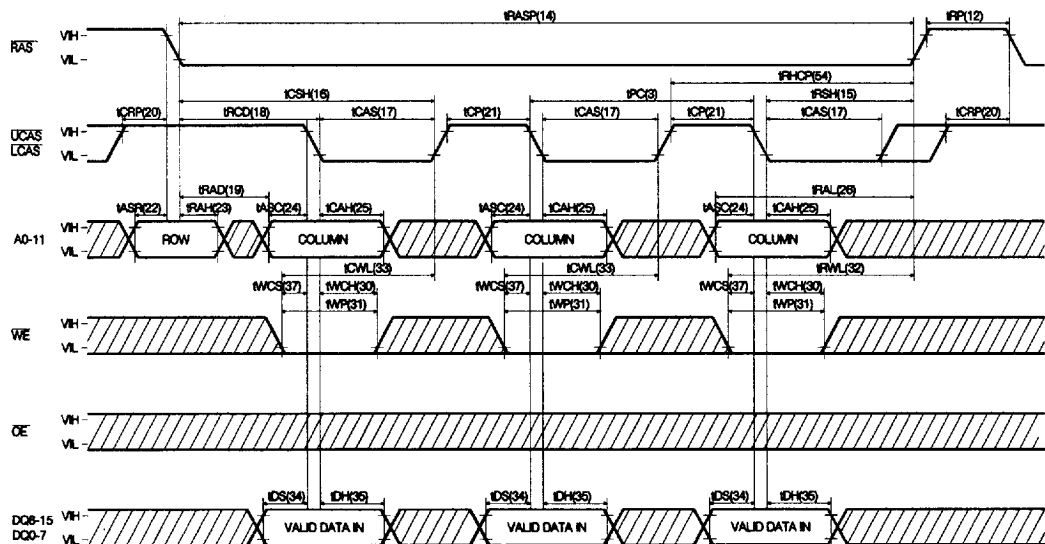
The timing diagram illustrates the relationship between several control and data signals for the 64K16000. The signals and their timing parameters are as follows:

- RAS**: Row Address Strobe. Timing parameters include $t_{RC}(1)$ (total row cycle), $t_{RCD}(18)$ (row-to-column delay), $t_{CSH}(19)$ (row setup), $t_{RPH}(12)$ (row pulse high), $t_{RCP}(20)$ (row-to-column precharge), $t_{RAS}(22)$ (row access time), and $t_{RAH}(23)$ (row afterburn).
- UCAS**: Column Address Strobe. Timing parameters include $t_{CAS}(17)$ (column access time) and $t_{CPH}(20)$ (column pulse high).
- AD-11**: Address Data Bus. It shows **ROW** and **COLUMN** periods. Timing parameters include $t_{RAD}(19)$ (row address delay), $t_{ASC}(24)$ (address-to-column delay), $t_{CAH}(25)$ (column afterburn), and $t_{RAL}(26)$ (row address latency).
- WE**: Write Enable. Timing parameters include $t_{CWL}(33)$ (column write latency) and $t_{RWL}(32)$ (row write latency).
- OE**: Output Enable. Timing parameters include $t_{WPS}(31)$ (write pulse setup), $t_{OBS}(48)$ (output burst setup), $t_{OED}(47)$ (output enable delay), $t_{OS}(34)$ (output setup), and $t_{OH}(35)$ (output hold).
- DQ8-15 / DQ0-7**: Data Bus. It shows **HIGH-Z** and **VALID DATA IN** periods.

FAST PAGE MODE READ CYCLE



FAST PAGE MODE EARLY WRITE CYCLE



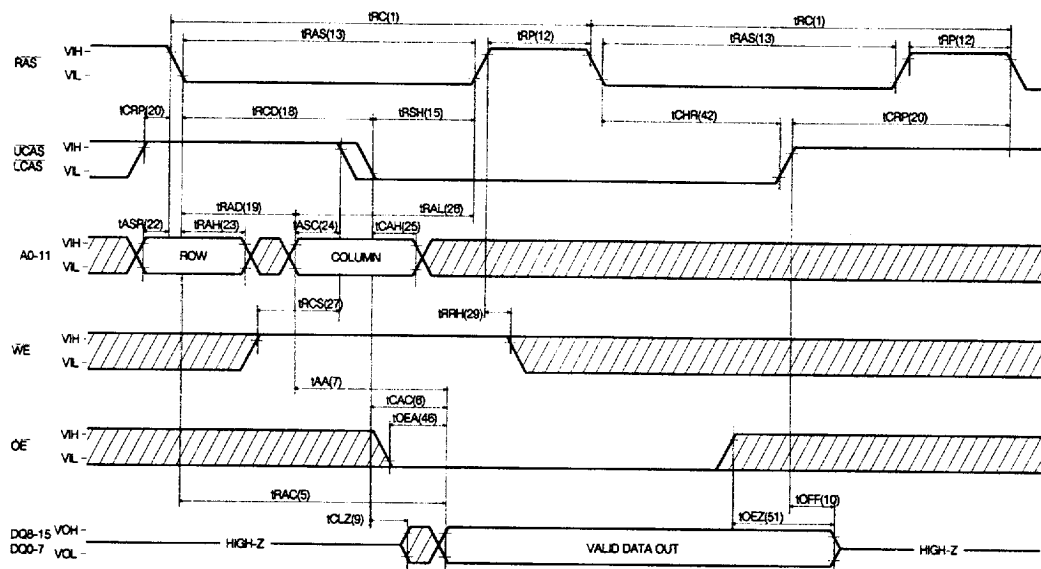
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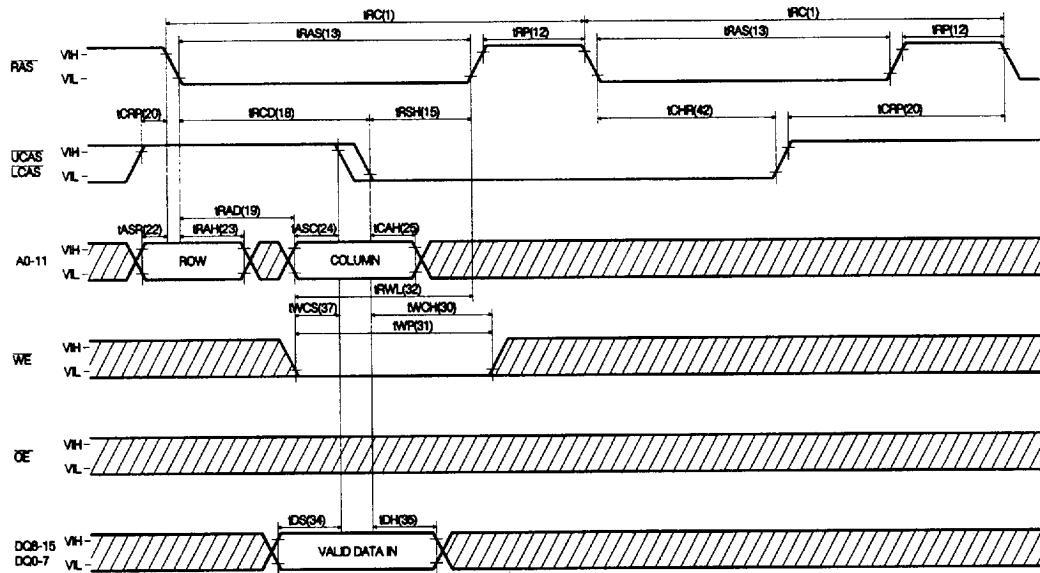
The diagram shows the timing of the 68000 microprocessor signals. The signals are:

- RAS**: RAS signal, with levels V_{IH} and V_{IL} . Timing parameters shown are RAS_{12} , RAS_{13} , and RQ_1 .
- DCAS**: Data Cache Address Strobe signal, with levels V_{IH} and V_{IL} . Timing parameters shown are RPC_{43} , ICP_{21} , $ICSR_{41}$, and ICH_{42} .
- WE**: Write Enable signal, with levels V_{IH} and V_{IL} . Timing parameters shown are $JOFF_{10}$ and $HIGH-Z$.
- DQ0-7**: Data bus signals, with levels V_{OH} and V_{OL} . Timing parameters shown are $JOFF_{10}$ and $HIGH-Z$.

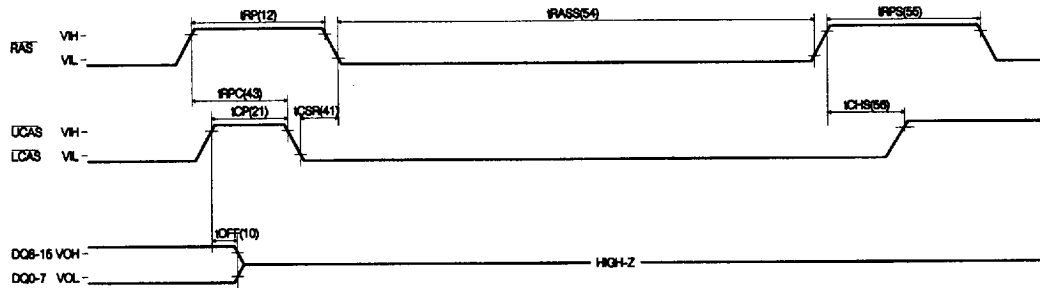
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (WRITE)

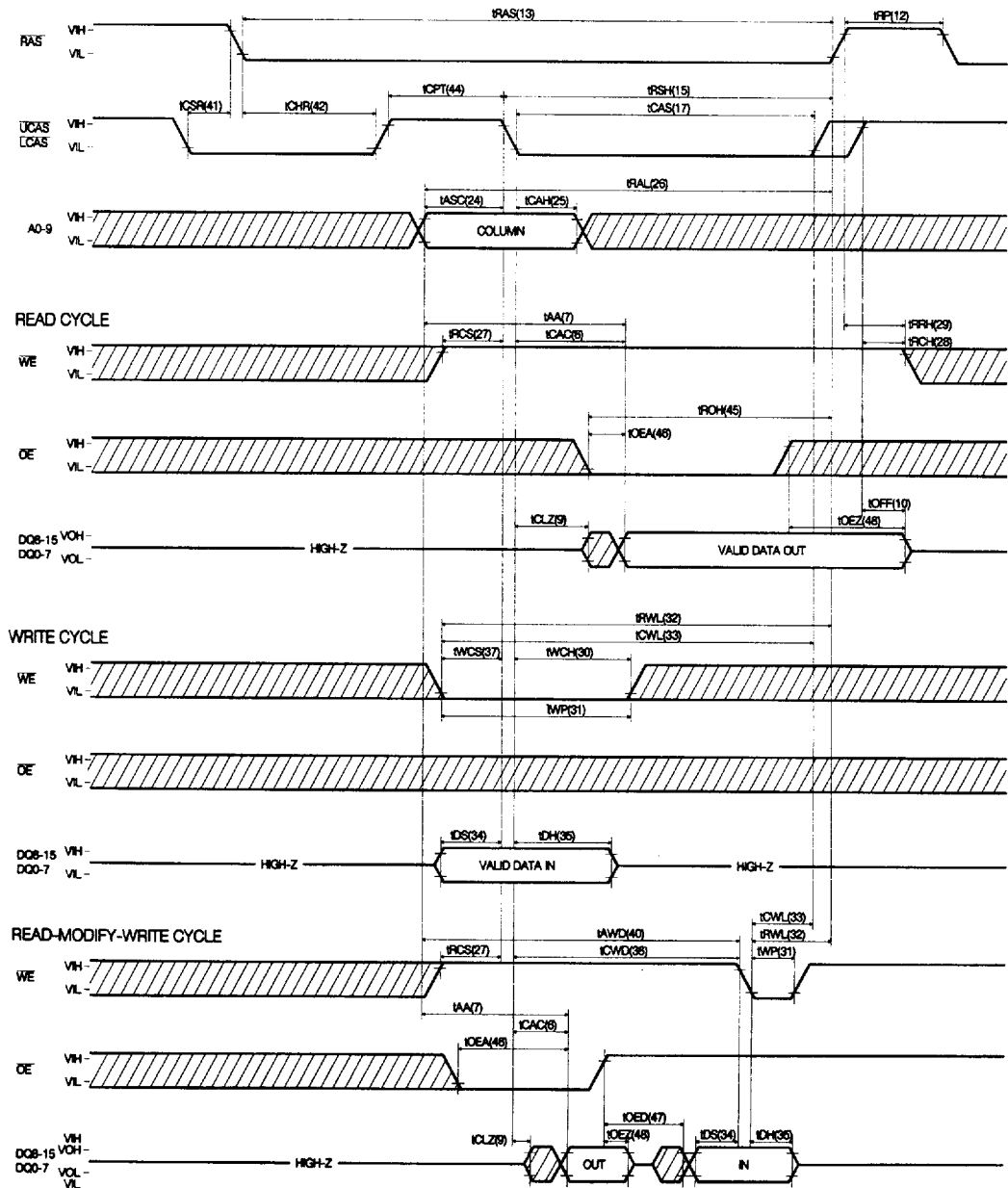


CAS-BEFORE-RAS SELF REFRESH CYCLE



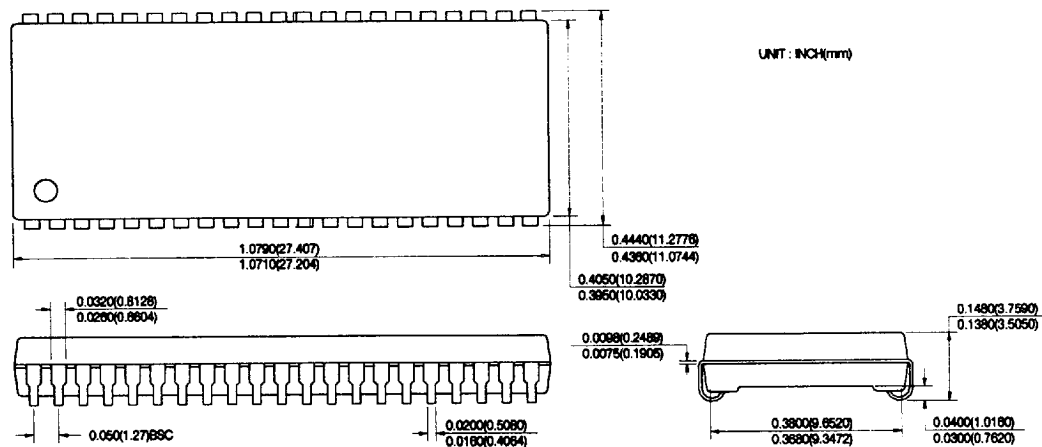
NOTE : A0-11, OE and WE = "H" or "L"

CAS-BEFORE-RAS REFRESH COUNTER TEST CYCLE

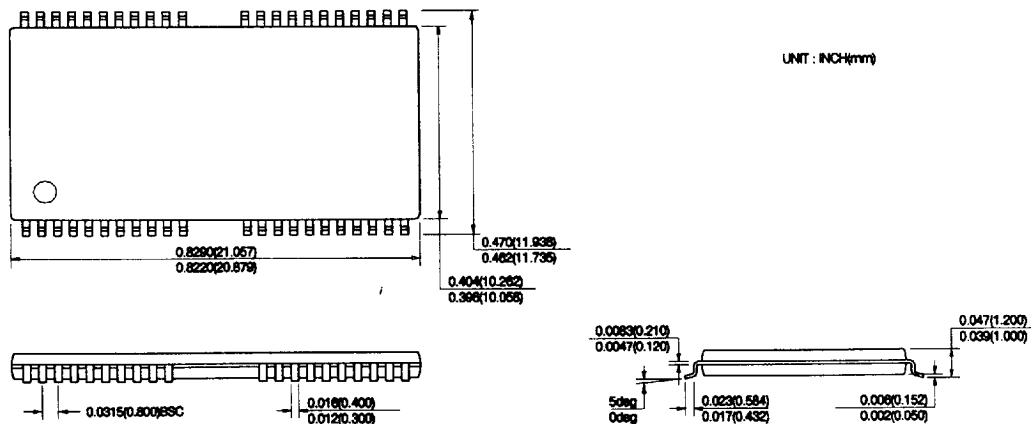


PACKAGE INFORMATION

400 mil 42/42 pin Small Outline J-form Package (JC)



400 mil 44/50 pin Thin Small Outline Package (TC) (RC)



ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY51V16160BJC	60/70/80		SOJ
HY51V16160BSLJC	60/70/80	SL-part	SOJ
HY51V16160BTC	60/70/80		TSOP-II
HY51V16160BSLTC	60/70/80	SL-part	TSOP-II
HY51V16160BRC	60/70/80		TSOP-II(R)
HY51V16160BSLRC	60/70/80	SL-part	TSOP-II(R)