

DESCRIPTION

This family is a 1M bit dynamic RAM organized 1,048,576 x 1-bit configuration with Fast Page mode CMOS DRAMs. Fast Page mode offers high speed of random access memory within the same row. The circuit and process design allow this device to achieve high performance and low power dissipation. Optional features are access time(60, 70 or 80ns) and power consumption (Normal or Low power). Hyundai's advanced circuit design and process technology allow this device to achieve high bandwidth, low power consumption and high reliability.

FEATURES

- Fast Page Mode operation
- Read-modify-write Capability
- TTL compatible inputs and outputs
- /CAS-before-/RAS, /RAS-only, Hidden and Self refresh capability
- Max. Active power dissipation
- JEDEC standard pinout
- 20/26-pin SOJ (300mil)
- Single power supply of $5V \pm 10\%$
- Early Write or output enable controlled write
- Fast access time and cycle time

Speed	Power
60	467mW
70	412mW
80	357mW

Speed	tRAC	tCAC	tPC
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Refresh cycle

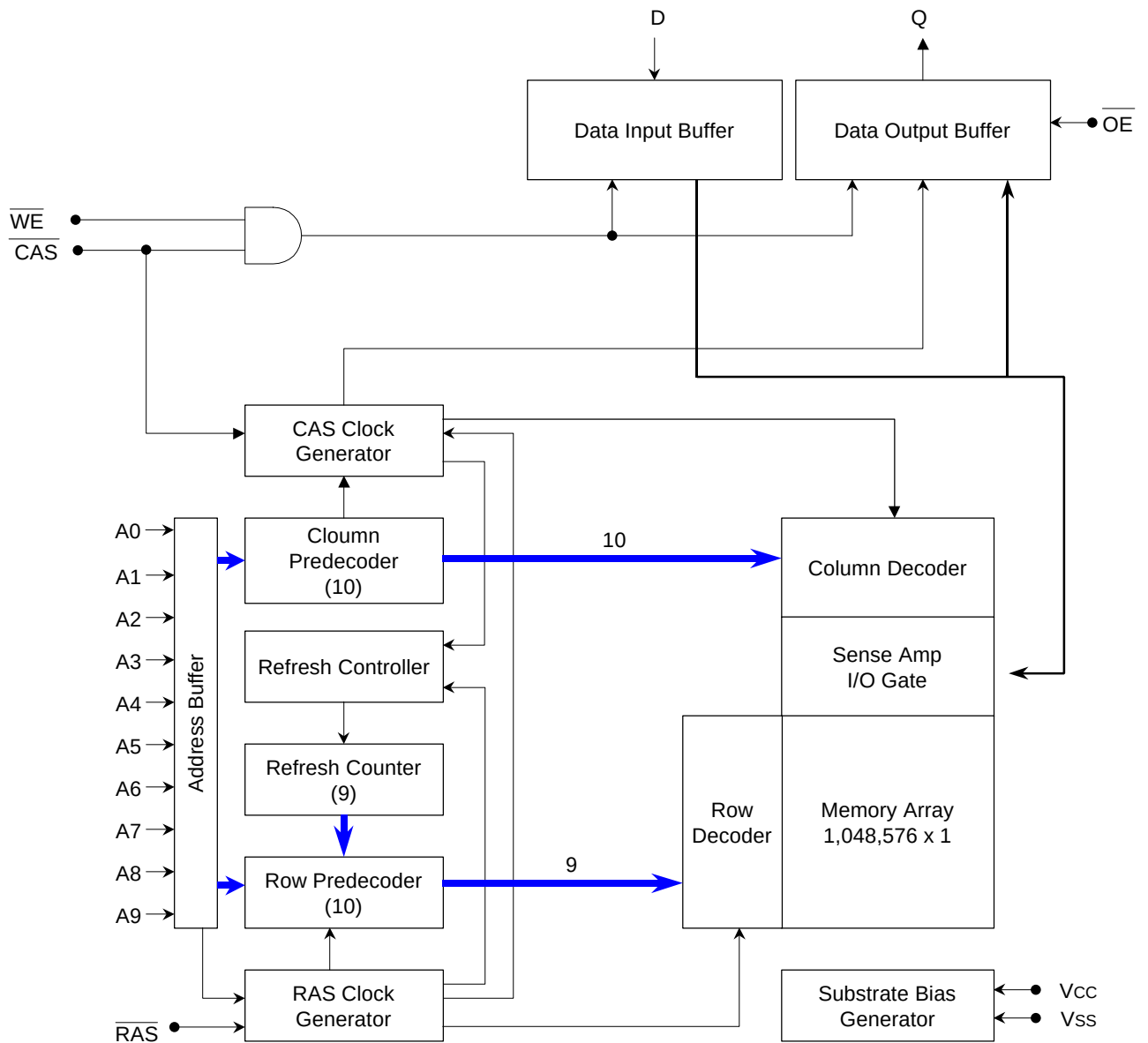
Part number	Refresh	Normal	L-part
HY531000A	512	8ms	64ms

ORDERING INFORMATION

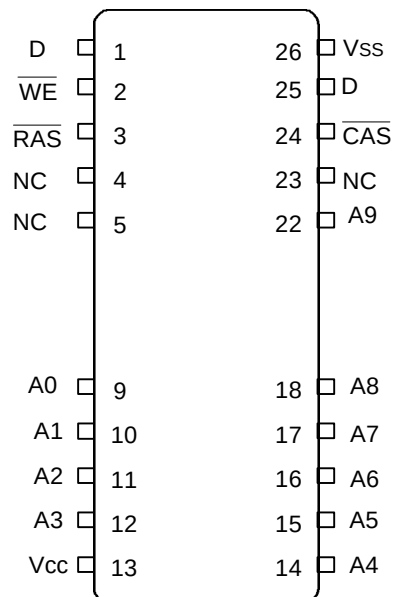
Part Name	Refresh	Power	Package
HY531000AJ	512		20/26Pin SOJ
HY531000ALJ	512	L-part	20/26Pin SOJ

*L : Low power

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Marking Side)



20/26 Pin Plastic SOJ (300mil)

PIN DESCRIPTION

Pin Name	Parameter
/RAS	Row Address Strobe
/CAS	Column Address Strobe
/WE	Write Enable
/OE	Output Enable
A0~A9	Address Input
D	Data Input
Q	Data Output
Vcc	Power (5V)
Vss	Ground

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Unit
T _A	Ambient Temperature	0 to 70	°C
T _{STG}	Storage Temperature	-55 to 150	°C
V _{IN} , V _{OUT}	Voltage on Any Pin relative to V _{SS}	-1.0 to 7.0	V
V _{CC}	Voltage on V _{CC} relative to V _{SS}	-1.0 to 7.0	V
I _{OS}	Short Circuit Output Current	50	mA
P _D	Power Dissipation	0.9	W
T _{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec

Note : Operation at or above Absolute Maximum Ratings can adversely affect device reliability

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

Symbol	Parameter	Min	Typ	Max	UNIT
V _{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	V _{CC} +1.0	V
V _{IL}	Input Low Voltage	-1.0	-	0.8	V

Note : All voltages are referenced to V_{SS}.

DC OPERATING CHARACTERISTICS

Symbol	Parameter	Test condition	Min	Max	Unit
I _{LI}	Input Leakage Current (Any input)	V _{SS} ≤ V _{IN} ≤ V _{CC} All other pins not under test = V _{SS}	-10	10	μA
I _{LO}	Output Leakage Current (Any input)	V _{SS} ≤ V _{OUT} ≤ V _{CC} /RAS & /CAS at V _{IH}	-10	10	μA
V _{OL}	Output Low Voltage	I _{OL} = 4.2mA	-	0.4	V
V _{OH}	Output High Voltage	I _{OH} = -5.0mA	2.4	-	V

DC CHARACTERISTICS

(TA = 0°C to 70°C, VCC = 5V ± 10%, VSS = 0V, unless otherwise noted.)

Symbol	Parameter	Test condition	Speed	Max.	Unit
Icc1	Operating Current	/RAS, /CAS Cycling tRC = tRC(min)	60 70 80	85 75 65	mA
Icc2	TTL Standby Current	/RAS, /CAS ≥ VIH(min) Other inputs ≥ VSS		2	mA
Icc3	/RAS-only Refresh Current	/RAS Cycling, /CAS = VIH tRC = tRC(min)	60 70 80	85 75 65	mA
Icc4	Fast Page mode Current	/CAS Cycling, /RAS = VIL tPC = tPC(min)	60 70 80	70 55 45	mA
Icc5	CMOS Standby Current	/RAS = /CAS ≥ VCC - 0.2V	L-part	1 200	mA μA
Icc6	/CAS-before-/RAS Refresh Current	/RAS & /CAS = 0.2V tRC = tRC(min.)	60 70 80	85 75 65	mA
Icc7	Battery Back-up Current (L-part)	tRC=125μs /CAS = CBR cycling or 0.2V /OE & /WE = VCC - 0.2V Address = VCC-0.2V or 0.2V D = VCC-0.2, 0.2V or Open Q = open	tRAS ≤ 300ns	300	μA
			tRAS ≤ 1us	400	

Note

- Icc1, Icc3, Icc4, Icc6 and Icc7 depend on output loading and cycle rates.
- Specified values are obtained with output unloaded.
- Icc is specified as an average current. In Icc1, Icc3, Icc6, address can be changed only once while /RAS=VIL. In Icc4, address can be changed maximum once while /CAS=VIH within one cycle time tPC.
- Only tRAS(max) = 1μs is applied to refresh of battery backup but tRAS(max) = 10μs is to applied to normal functional operation.
- Icc5(max.), Icc7 are applied to L-part only.

AC CHARACTERISTICS

(T_A = 0 °C to 70 °C, V_{CC} = 5V ± 10% , V_{SS} = 0V, unless otherwise noted.)

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
t _{RC}	Random read or write cycle time	110	-	130	-	150	-	ns	
t _{RWC}	Read-modify-write cycle time	130	-	155	-	175	-	ns	
t _{PC}	Fast Page mode cycle time	40	-	40	-	45	-	ns	
t _{PRWC}	Fast Page mode read-modify-write cycle time	60	-	65	-	70	-	ns	
t _{RAC}	Access time from /RAS	-	60	-	70	-	80	ns	4,9,10
t _{CAC}	Access time from /CAS	-	15	-	20	-	20	ns	4,9
t _{AA}	Access time from column address	-	30	-	35	-	40	ns	4,10
t _{CPA}	Access time from /CAS precharge	-	35	-	35	-	40	ns	4,
t _{CLZ}	/CAS to output low impedance	0	-	0	-	0	-	ns	4
t _{OFF}	Output Buffer Turn-off Dealy Time	0	20	0	20	0	20	ns	4
t _T	Transition time(rise and fall)	3	50	3	50	3	50	ns	3
t _{RP}	/RAS precharge time	40	-	50	-	60	-	ns	
t _{RAS}	/RAS pulse width	60	10K	70	10K	80	10K	ns	
t _{RASP}	/RAS pulse width(Fast Page Mode)	60	100K	70	100K	80	100K	ns	
t _{RS}	/RAS hold time	15	-	20	-	20	-	ns	
t _{CS}	/CAS hold time	60	-	70	-	80	-	ns	
t _{CAS}	/CAS pulse width	15	10K	15	10K	20	10K	ns	
t _{RCD}	/RAS to /CAS delay time	20	45	20	50	20	60	ns	9
t _{RAD}	/RAS to column address delay time	15	30	15	35	15	40	ns	10
t _{CRP}	/CAS to /RAS precharge time	5	-	5	-	5	-	ns	15
t _{CP}	/CAS precharge time	10	-	10	-	10	-	ns	17
t _{ASR}	Row address set-up time	0	-	0	-	0	-	ns	
t _{RAH}	Row address hold time	10	-	10	-	10	-	ns	
t _{ASC}	Column address set-up time	0	-	0	-	0	-	ns	13
t _{CAH}	Column address hold time	15	-	15	-	15	-	ns	
t _{AR}	Column address hold time from /CAS	45	-	50	-	55	-	ns	
t _{RAL}	Column address to /RAS lead time	25	-	30	-	35	-	ns	
t _{RCS}	Read command set-up time	0	-	0	-	0	-	ns	
t _{RCH}	Read command hold time referenced to /CAS	0	-	0	-	0	-	ns	6
t _{RRH}	Read command hold time referenced to /RAS	0	-	0	-	0	-	ns	6
t _{WCH}	Write command hold time	15	-	15	-	15	-	ns	
t _{WCR}	Write command hold time from /RAS	45	-	50	-	55	-	ns	
t _{WP}	Write command pulse width	10	-	15	-	15	-	ns	
t _{RWL}	Write command to /RAS lead time	15	-	20	-	20	-	ns	

AC CHARACTERISTICS

Continued

Symbol	Parameter	60ns		70ns		80ns		Unit	Note
		Min	Max	Min	Max	Min	Max		
tcWL	Write command to /CAS lead time	15	-	20	-	20	-	ns	
tDS	Data-in set-up time	0	-	0	-	0	-	ns	7
tDH	Data-in hold time	15	-	15	-	15	-	ns	7
tREF	Refresh period(512 cycles)	8	-	8	-	8	-	ms	11
	Refresh period(L-part)	64	-	64	-	64	-	ms	11
twCS	Write command set-up time	0	-	0	-	0	-	ns	8
tcWD	/CAS to /WE delay time	15	-	20	-	20	-	ns	8
trWD	/RAS to /WE delay time	60	-	70	-	80	-	ns	8
tAWD	Column address to /WE delay time	30	-	35	-	40	-	ns	8
tCSR	/CAS set-up time(CBR cycle)	5	-	5	-	5	-	ns	
tCHR	/CAS hold time(CBR cycle)	15	-	15	-	15	-	ns	
trPC	/RAS to /CAS precharge time	0	-	0	-	0	-	ns	
tcPT	/CAS precharge time(CBR counter test)	40	-	40	-	40	-	ns	
tcpWD	/WE delay time from /CAS precharge	30	-	35	-	40	-	ns	8
trHCP	/RAS hold time from /CAS precharge	30	-	35	-	35	-	ns	

NOTE

1. An initial pause of 200 μ s is required after power-up followed by 8 /RAS only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CBR refresh cycles instead of 8 /RAS-only refresh cycles are required.
2. AC measurements assume $t_T=5$ ns
3. VIH(min.) and VIL(max.) are reference levels for measuring timing of input signals. Transition times are measured between VIH(min.) and VIL(max.).
4. Measured at VOH=2.0V and VOL=0.8V with a load equivalent to 2TTL loads and 100pF.
5. tOFF(max.) defines the time at which the output achieves in early write cycles and to /WE leading edge in Read-Modify-Write cycles.
6. Either trCH or trRH must be satisfied for a read cycle.
7. These parameters are referenced to /CAS leading edge in early write cycles and to /WE leading edge in read-modify-write cycles.
8. twCS, trWD, tcWD, tAWD and tCPWD are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $twCS \geq twCS(min.)$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $trWD \geq trWD(min.)$, $tcWD \geq tcWD(min.)$, $tAWD \geq tAWD(min.)$, and $tCPWD \geq tCPWD(min.)$, the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. Operation within the tRCD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. If tRCD is greater than the specified tRCD(max.) limit, then access time is controlled by tCAC.
10. Operation within the tRAD(max.) limit insures that tRAC(max.) can be met. tRAD(max.) is specified as a reference point only. tRAD is greater than the specified tRAD(max.) limit, then access time is controlled by tAA.
11. tREF(max.)=64ms is applied to L-parts only. (HY531000ALS and HY531000ALJ)

CAPACITANCE

(TA = 25°C, VCC = 5V $\pm$ 10%, VSS = 0V and f=1MHz, unless otherwise noted.)

Symbol	Parameter	Typ.	Max	Unit
CIN1	Input Capacitance (A0~A9)	-	5	pF
CIN2	Input Capacitance (/RAS, /CAS, /WE)	-	7	pF
COUT	Data Output Capacitance (Q)	-	7	pF