

DESCRIPTION

The HY534256A is the 2nd generation and fast dynamic RAM organized 262,144 x 4-bit. The HY534256A utilizes Hyundai's CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operating margins to the users. Multiplexed address inputs permit the HY534256A to be packaged in a standard 300mil 20 pin PDIP, 20/26 pin SOJ.

The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipments. System oriented feature includes single power supply of 5V± 10% tolerance and direct interfacing capability with high performance logic families such as Schottky TTL.

FEATURES

- Low power dissipation
Max. battery back-up 2.2mW (L-Part)
Max. CMOS standby 1.1mW (L-part)
5.5mW

Max. TTL standby 11.0mW

Max. operating

Speed	Power
60	495mW
70	440mW
80	385mW

- Single power supply of 5V± 10%
- TTL compatible inputs and outputs
- Fast access Time

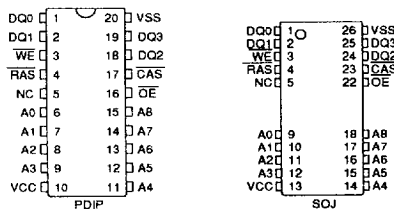
Speed	t _{RAC}	t _{CAC}	t _{PC}
60	60ns	15ns	40ns
70	70ns	20ns	40ns
80	80ns	20ns	45ns

- Fast page mode operation
- Read-Modify-Write capability
- CAS-before-RAS, RAS-only, Hidden refresh
- 512 refresh cycles / 64ms (L-part)
512 refresh cycles / 8ms

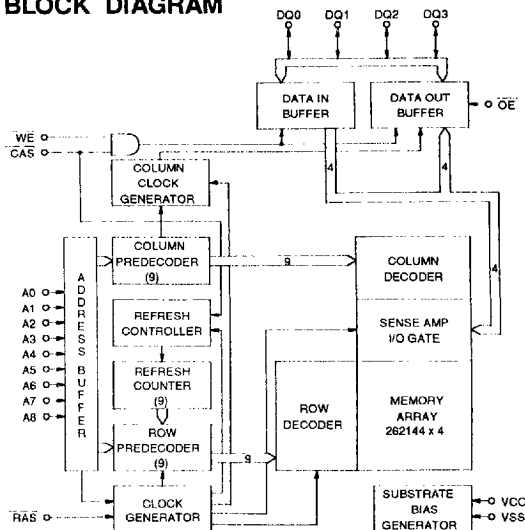
PIN DESCRIPTION

RAS	Row Address Strobe
CAS	Column Address Strobe
WE	Write Enable
OE	Output Enable
A0-A8	Address Input
DQ0-DQ3	Data Input/Output
VCC	Power (+ 5V)
VSS	Ground

PIN CONNECTION



BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	RATING	UNIT
TA	Ambient Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
VIN, VOUT	Voltage on Any Pin Relative to Vss	-1.0 to 7.0	V
VCC	Voltage on Vcc Relative to Vss	-1.0 to 7.0	V
Ios	Short Circuit Output Current	50	mA
PD	Power Dissipation	0.60	W
TSOLDER	Soldering Temperature• Time	260•10	°C•sec

NOTE : Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(TA= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
VCC	Supply Voltage	4.5	5.0	5.5	V
VIH	Input High Voltage	2.4	-	Vcc+ 1.0	V
VIL	Input Low Voltage	-1.0	-	0.8	V

NOTE : All voltages are referenced to Vss.

DC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/ POWER	MIN.	MAX.	UNIT	NOTE
ILI	Input Leakage Current (Any Input Pins)	VSS ≤ VIN ≤ VCC All other pins not under test= VSS		-10	10	μA	
ILO	Output Leakage Current (High Impedance State)	VSS ≤ VOUT ≤ VCC RAS & CAS at VIH		-10	10	μA	
ICC1	VCC Supply Current, Operating	tRC= tRC (min.)	60 70 80	- - -	90 80 70	mA	1,2,3
ICC2	VCC Supply Current, TTL Standby	RAS & CAS at VIH, other inputs ≥ VSS		-	2	mA	
ICC3	VCC Supply Current, RAS-only refresh	tRC= tRC (min.)	60 70 80	- - -	90 80 70	mA	1,3
ICC4	VCC Supply Current, Fast Page mode	tPC= tPC (min.)	60 70 80	- - -	70 60 50	mA	1,2,3
ICC5	VCC Supply Current, CMOS Standby	RAS & CAS ≥ VCC-0.2V	L-part	-	1 0.2	mA	5
ICC6	VCC Supply Current, CAS-before-RAS refresh	tRC= tRC (min.)	60 70 80	- - -	90 80 70	mA	1,3
ICC7	VCC Supply Current, Battery Back Up (L-part only)	tRC= 125μs, CAS= CBR cycling or 0.2V OE & WE= VCC-0.2V, A0-A8= VCC-0.2V or 0.2V DQ0-DQ3= 0.2V, VCC-0.2V or open	tRAS ≤ 300ns	-	300	μA	1,4,5
			tRAS ≤ 1μs	-	400		
VOL	Output Low Voltage	IOL= 4.2mA		-	0.4	V	
VOH	Output High Voltage	IOH= -5mA		2.4	-	V	

NOTE :

1. ICC1, ICC3, ICC4, ICC6 and ICC7 depend on cycle rate.
2. ICC1 and ICC4 depend on output loading. Specified values are obtained with the output open.
3. It depends on user whether column address is changed or not at least once while RAS= VIH and CAS= VIH.
4. Only tRAS(max.)= 1μs is applied to refresh of battery backup but tRAS(max.)= 10μs is applied to normal functional operation.
5. ICC5(max.)= 0.2mA and ICC7 are applied to L-part only(HY534256ALS and HY534256ALJ).

AC CHARACTERISTICS

(TA= 0°C to 70°C, VCC= 5V± 10%, VSS= 0V, unless otherwise noted.) NOTE : 1, 2, 3

#	SYMBOL	PARAMETER	HY534256AS/AJ/ALS/ALJ						UNIT	NOTE
			-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tRC	Random Read or Write Cycle Time	110	-	130	-	150	-	ns	
2	tRWC	Read-Modify-Write Cycle Time	160	-	185	-	205	-	ns	
3	tPC	Fast Page Mode Cycle Time	40	-	40	-	45	-	ns	
4	tPRWC	Fast Page Mode Read-Modify-Write Cycle Time	90	-	95	-	100	-	ns	
5	tRAC	Access Time from RAS	-	60	-	70	-	80	ns	4,9,10
6	tCAC	Access Time from CAS	-	15	-	20	-	20	ns	4,9
7	tAA	Access Time from Column Address	-	30	-	35	-	40	ns	4,10
8	tCPA	Access Time from CAS Precharge	-	35	-	35	-	40	ns	4
9	tCLZ	CAS to Output Low Impedance	0	-	0	-	0	-	ns	4
10	tOFF	Output Buffer Turn-off Delay	0	20	0	20	0	20	ns	5
11	tT	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	3
12	tRP	RAS Precharge Time	40	-	50	-	60	-	ns	
13	tRAS	RAS Pulse Width	60	10K	70	10K	80	10K	ns	
14	tRASP	RAS Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
15	tRSH	RAS Hold Time	15	-	20	-	20	-	ns	
16	tCSH	CAS Hold Time	60	-	70	-	80	-	ns	
17	tCAS	CAS Pulse Width	15	10K	20	10K	20	10K	ns	
18	tRCD	RAS to CAS Delay	20	45	20	50	20	60	ns	9
19	tRAD	RAS to Column Address Delay Time	15	30	15	35	15	40	ns	10
20	tCRP	CAS to RAS Precharge Time	5	-	5	-	5	-	ns	
21	tCP	CAS Precharge Time	10	-	10	-	10	-	ns	
22	tASR	Row Address Set-up Time	0	-	0	-	0	-	ns	
23	tRAH	Row Address Hold Time	10	-	10	-	10	-	ns	
24	tASC	Column Address Set-up Time	0	-	0	-	0	-	ns	
25	tCAH	Column Address Hold Time	15	-	15	-	15	-	ns	
26	tAR	Column Address Hold Time from RAS	45	-	50	-	55	-	ns	
27	tRAL	Column Address to RAS Lead Time	25	-	35	-	40	-	ns	
28	tRCS	Read Command Set-up Time	0	-	0	-	0	-	ns	
29	tRCH	Read Command Hold Time Referenced to CAS	0	-	0	-	0	-	ns	6
30	tRRH	Read Command Hold Time Referenced to RAS	0	-	0	-	0	-	ns	6
31	tWCH	Write Command Hold Time	10	-	15	-	15	-	ns	
32	tWCR	Write Command Hold Time from RAS	45	-	50	-	55	-	ns	
33	tWP	Write Command Pulse Width	10	-	15	-	15	-	ns	
34	tRWL	Write Command to RAS Lead Time	15	-	20	-	20	-	ns	
35	tCWL	Write Command to CAS Lead Time	15	-	20	-	20	-	ns	
36	tDS	Data-In Set-up Time	0	-	0	-	0	-	ns	7
37	tDH	Data-In Hold Time	15	-	15	-	15	-	ns	7
38	tDHR	Data-In Hold Time Referenced to RAS	45	-	50	-	55	-	ns	
39	tREF	Refresh Period (512 cycles)	-	8	-	8	-	8	ms	
		L-Part	-	64	-	64	-	64		11
40	tWCS	Write Command Set-up Time	0	-	0	-	0	-	ns	8

AC CHARACTERISTICS

(continued)

		HY534256AS/AJ/ALS/ALJ						UNIT	NOTE	
#	SYMBOL	PARAMETER	-60		-70		-80			
			MIN.	MAX.	MIN.	MAX.	MIN.			MAX.
41	tCWD	CAS to WE Delay Time	45	-	50	-	50	-	ns	8
42	tRWD	RAS to WE Delay Time	90	-	100	-	110	-	ns	8
43	tAWD	Column Address to WE Delay Time	60	-	65	-	70	-	ns	8
44	tCSR	CAS Set-up Time (CBR Cycle)	5	-	5	-	5	-	ns	
45	tCHR	CAS Hold Time (CBR Cycle)	10	-	10	-	10	-	ns	
46	tRPC	RAS to CAS Precharge Time	0	-	0	-	0	-	ns	
47	tCPT	CAS Precharge Time (CBR Counter Test)	40	-	40	-	40	-	ns	
48	tROH	RAS Hold Time Reference to OE	10	-	10	-	15	-	ns	
49	tOEA	OE Access Time	-	15	-	20	-	20	ns	
50	tOED	OE to Data Delay	20	-	20	-	20	-	ns	
51	tOEZ	Output Buffer Turn Off Delay Time from OE	0	15	0	15	0	20	ns	5
52	tOEH	OE Command Hold Time	20	-	20	-	20	-	ns	
53	tCPWD	WE Delay Time from CAS Precharge	60	-	65	-	70	-	ns	8
54	tRHCP	RAS Hold Time from CAS Precharge	30	-	35	-	35	-	ns	

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NOTE :

1. An initial pause of 200 μ s is required after power-up followed by 8 **RAS** cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 **CAS**-before-**RAS** initialization cycles instead of 8 **RAS** cycles are required.
2. AC measurements assume $t_T = 5$ ns.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Measured with a load equivalent to 2 TTL loads and 100pF.
5. $t_{OFF}(\text{max.})$ and define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. These parameters are referenced to **CAS** leading edge in early write cycles and to **WE** leading edge in Read-Modify-Write cycles.
8. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and data out pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$, and $t_{CPWD} \geq t_{CPWD}(\text{min.})$, the cycle is a Read-Modify-Write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminated.
9. Operation within the $t_{RCD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
10. Operation within the $t_{RAD}(\text{max.})$ limit insures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
11. $t_{REF}(\text{max.}) = 64$ ms is applied to L-part only (HY534256ALS and HY534256ALJ).

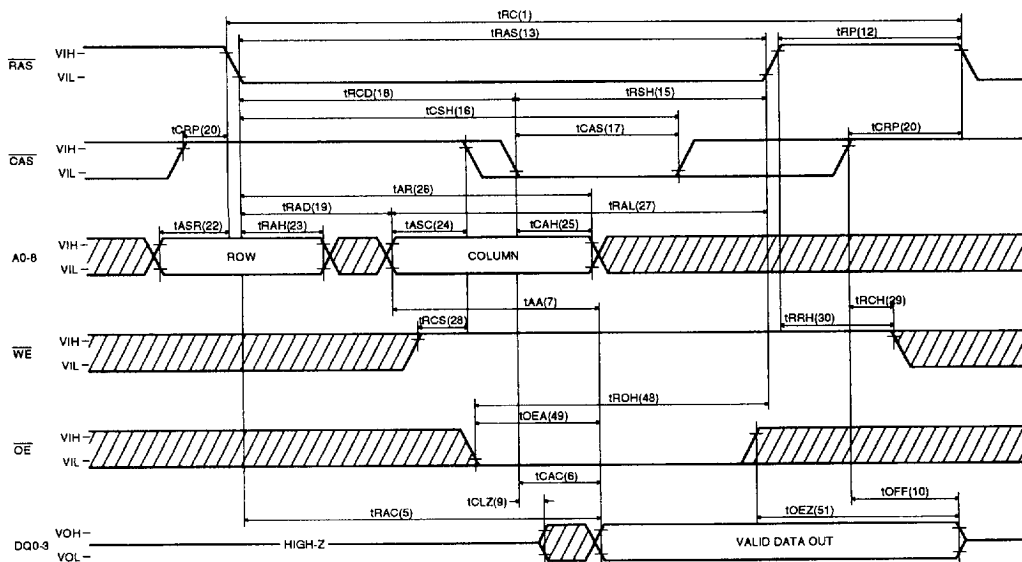
CAPACITANCE

($T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, unless otherwise noted.)

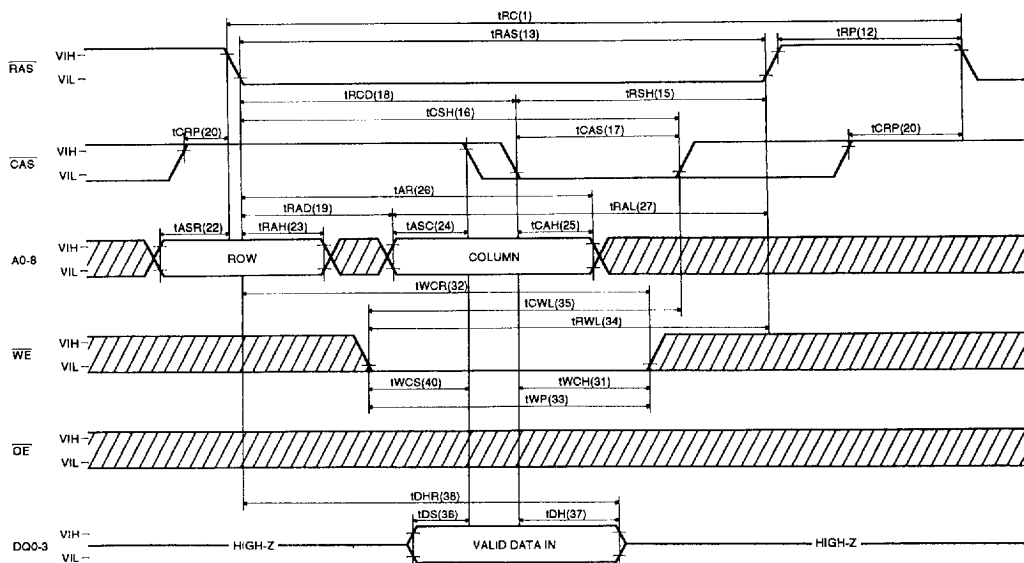
SYMBOL	PARAMETER	TYP.	MAX.	UNIT
CIN1	Input Capacitance (A0-A8, D)	-	5	pF
CIN2	Input Capacitance (RAS, CAS, WE, OE)	-	7	pF
COUT	Output Capacitance (Q)	-	7	pF

TIMING DIAGRAM

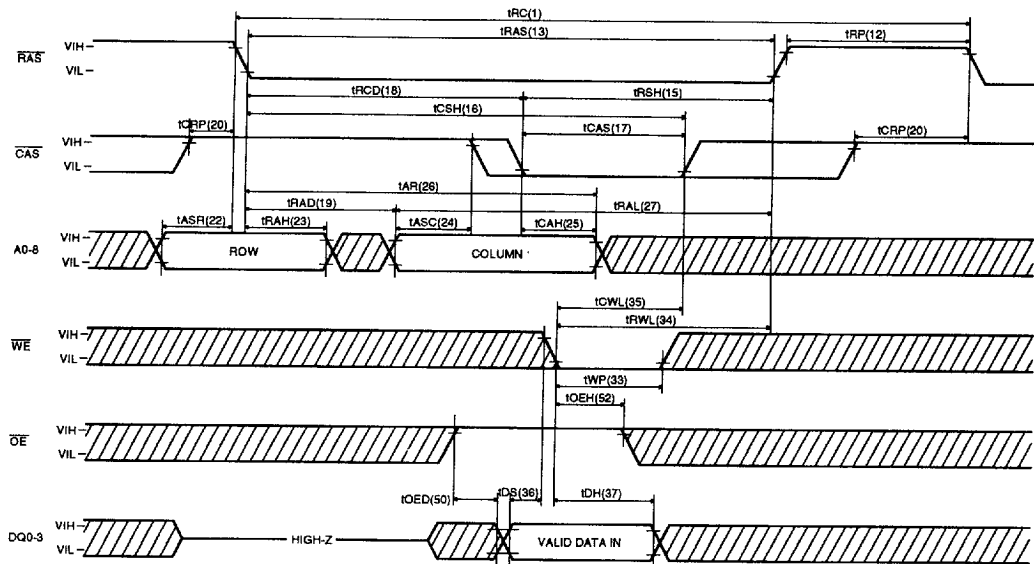
READ CYCLE



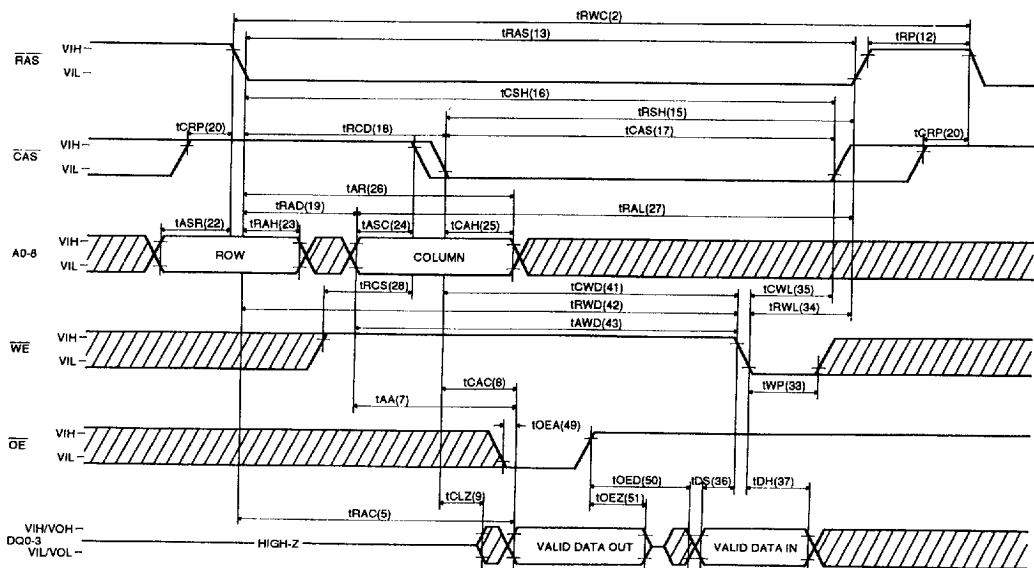
EARLY WRITE CYCLE



WRITE CYCLE ($\overline{OE}$ CONTROLLED WRITE)



READ-MODIFY-WRITE CYCLE



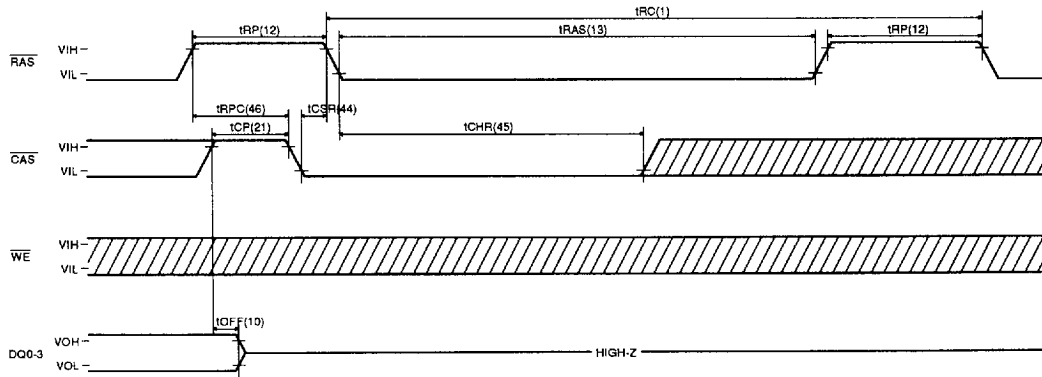
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The diagram shows the timing relationship between RAS, CAS, and ROW signals. RAS is an active-low signal. CAS is an active-low signal. ROW is a bidirectional signal, shown as an input/output buffer. The diagram illustrates the following timing parameters:

- $t_{RC}(1)$: RAS to Column Address Strobe (CAS) delay.
- $t_{RAS}(13)$: RAS pulse width.
- $t_{RP}(12)$: RAS to Data Output Delay.
- $t_{CRP}(20)$: CAS to RAS delay.
- $t_{RPC}(49)$: RAS to Data Output Delay.
- $t_{ASR}(22)$: Address Strobe to Row Address Strobe delay.
- $t_{RAH}(23)$: Row Address Strobe to Row Address Hold delay.

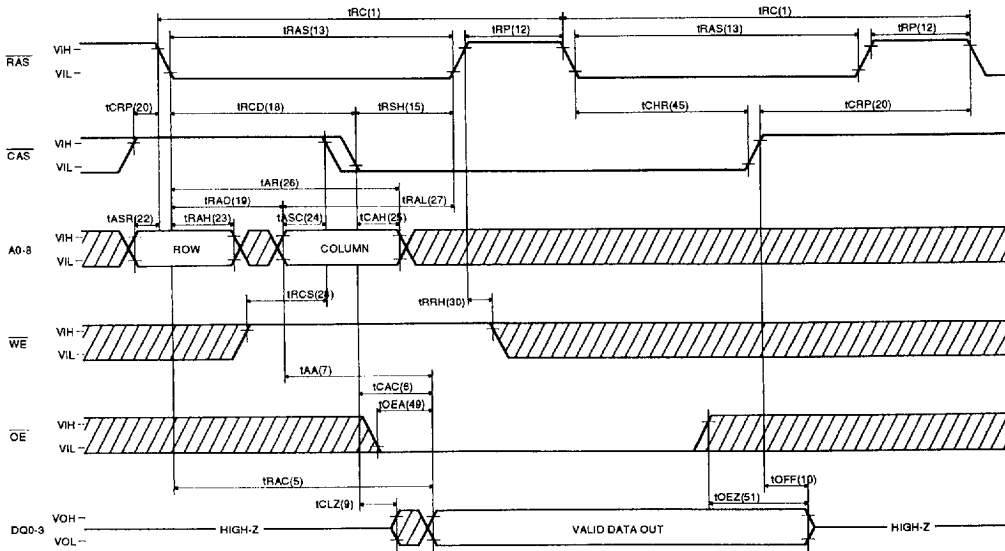
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CAS-BEFORE-RAS REFRESH CYCLE



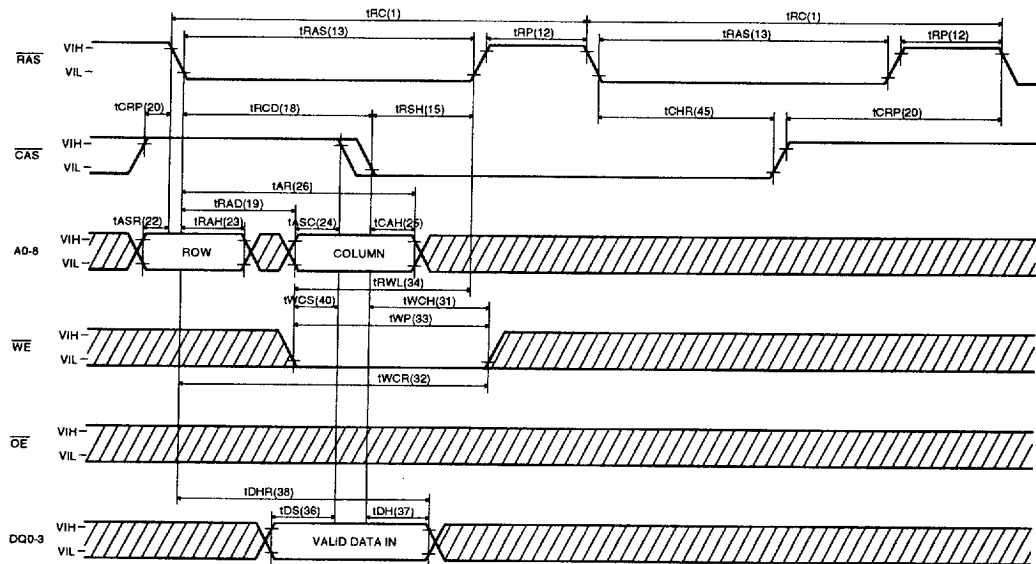
NOTE : A0-8 and OE = "H" or "L"

HIDDEN REFRESH CYCLE (READ)



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HIDDEN REFRESH CYCLE (WRITE)



READ CYCLE

The diagram illustrates the timing relationships for a read cycle. The signals and their timing parameters are as follows:

- WE (Write Enable):** Transitions from V_{IH} to V_{IL} . Timing parameters include $t_{RCS}(28)$ (from V_{IH} to start of valid data out), $t_{AA}(7)$ (from start of valid data out to V_{IL}), $t_{CAC}(5)$ (from V_{IL} to start of valid data out), $t_{RRH}(30)$ (from V_{IL} to end of valid data out), and $t_{RCH}(28)$ (from end of valid data out to V_{IL}).
- OE (Output Enable):** Transitions from V_{IH} to V_{IL} . Timing parameters include $t_{OEa}(49)$ (from V_{IH} to start of valid data out) and $t_{ROH}(48)$ (from start of valid data out to V_{IL}).
- DQ0-3 (Data Bus):** Shows V_{OH} , V_{OL} , and HIGH-Z states. Timing parameters include $t_{CLZ}(9)$ (from HIGH-Z to start of valid data out), $t_{OFF}(10)$ (from end of valid data out to HIGH-Z), and $t_{OEZ}(51)$ (from end of valid data out to V_{OH}/V_{OL}).
- VALID DATA OUT:** The period during which data is valid on the data bus.

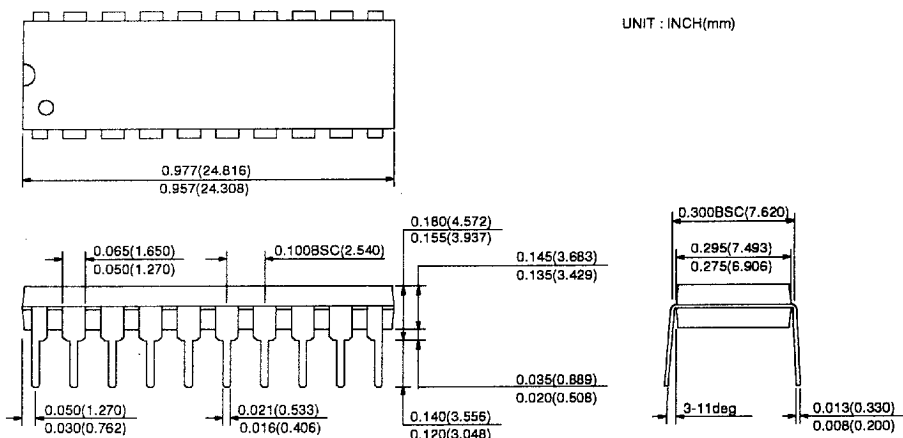
WRITE CYCLE

The diagram illustrates the timing for a write operation. The **WE** (Write Enable) signal is active-low. The **OE** (Output Enable) signal is also active-low. The **DQ0-3** bus is bidirectional, with **VALID DATA IN** indicated during the write cycle. The timing parameters are defined as follows:

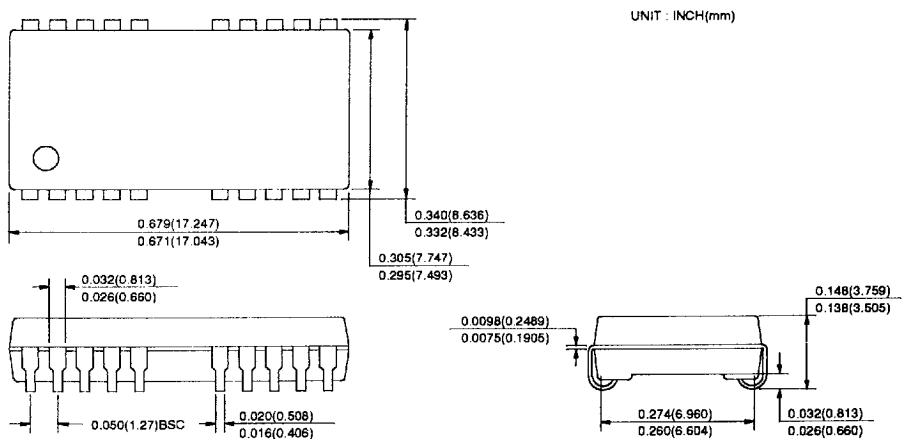
- $t_{WCS}(40)$: Write Command Setup time (from WE rising edge to DQ0-3 becoming valid).
- $t_{WCH}(31)$: Write Command Hold time (from WE falling edge to DQ0-3 becoming invalid).
- $t_{WP}(33)$: Write Pulse width (duration of WE pulse).
- $t_{RWL}(34)$: Write Recovery time (from WE falling edge to OE rising edge).
- $t_{CWL}(35)$: Write Recovery time (from WE falling edge to DQ0-3 becoming high-impedance).
- $t_{RWS}(36)$: Write Recovery time (from WE falling edge to DQ0-3 becoming high-impedance).
- $t_{OE}(37)$: Output Enable delay time (from OE falling edge to DQ0-3 becoming valid).
- $t_{DS}(36)$: Data Setup time (from DQ0-3 becoming valid to WE falling edge).
- $t_{DH}(37)$: Data Hold time (from WE falling edge to DQ0-3 becoming high-impedance).

PACKAGE INFORMATION

300 mil 20 pin Dual In Line Package (S)



300 mil 20/26 pin Thin Small Outline Package (J)



ORDERING INFORMATION

PART NUMBER	SPEED	POWER	PACKAGE
HY534256AS	60/70/80		PDIP
HY534256ALS	60/70/80	L-part	PDIP
HY534256AJ	60/70/80		SOJ
HY534256ALJ	60/70/80	L-part	SOJ