

SIEMENS

T-46-23-17

HYB 514256AL-60/-70 256K x 4-Bit Dynamic RAM

(Low Power Version)

Advance Information

- 262 144 x 4-bit organization
- Fast access and cycle time
60 ns access time
110 ns cycle time (HYB 514256AL-60)
70 ns access time
130 ns cycle time (HYB 514256AL-70)
- Fast page mode cycle time
40 ns (HYB 514256AL-60)
40 ns (HYB 514256AL-70)
- Single +5 V ($\pm 10\%$) supply with a built-in V_{BB} generator
- Output unlatched at cycle end allows two-dimensional chip selection
- Low power dissipation
max. 495 mW (HYB 514256AL-60)
max. 440 mW (HYB 514256AL-70)
max. 1.1 mW standby
- Read-modify-write, $\overline{CAS}$ -before- $\overline{RAS}$ refresh, $\overline{RAS}$ -only refresh, hidden-refresh, and fast page mode capability
- All inputs, outputs and clocks fully TTL-compatible
- 512 refresh cycles/64 ms
- Plastic Packages:
P-DIP-20-T HYB 514256AL,
P-SOJ-26/20 HYB 514256AJL,
P-ZIP-20/19 HYB 514256AZL

The HYB 514256AL-60/-70 is the new generation dynamic RAM organized as 262 144 words by 4-bit. The HYB 514256AL-60/-70 utilizes CMOS silicon gate process technology as well as advanced circuit techniques to provide wide operation margins, both internally and for the system user. Multiplexed address inputs permit the HYB 514256AL-60/-70 to be packaged in a standard 20-pin plastic DIP, 26/20 pin plastic SOJ and 20/19 pin plastic ZIP. This package size provides high system bit densities and is compatible with commonly used automatic testing and insertion equipment. System oriented features include single +5 V ($\pm 10\%$) power supply, direct interfacing with high-performance logic device families such as Schottky TTL. These HYB 514256AL-60/-70 256K x 4 DRAMs are specially selected for battery backup applications.

Ordering Information

T-46-23-17

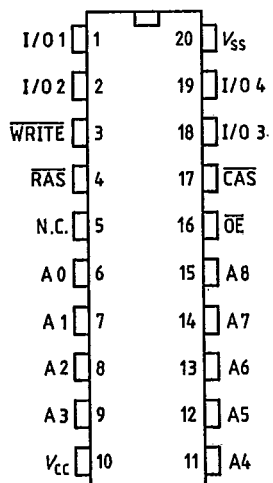
Type	Ordering code	Package	Description
HYB 514256AL-60	Q67100-Q489	P-DIP-20-T	DRAM (access time 60 ns)
HYB 514256AL-70	Q67100-Q490	P-DIP-20-T	DRAM (access time 70 ns)
HYB 514256AJL-60	Q67100-Q491	P-SOJ-26/20	DRAM (access time 60 ns)
HYB 514256AJL-70	Q67100-Q492	P-SOJ-26/20	DRAM (access time 70 ns)
HYB 514256AZL-60	Q67100-Q495	P-ZIP-20/19	DRAM (access time 60 ns)
HYB 514256AZL-70	Q67100-Q496	P-ZIP-20/19	DRAM (access time 70 ns)

Pin Names

A0-A8	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{OE}}$	Output Enable
I/O1-I/O4	Data Input Output
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WRITE}}$	Read/Write Input
V _{cc}	Power Supply (+5 V)
V _{ss}	Ground (0 V)
N.C.	No Connection

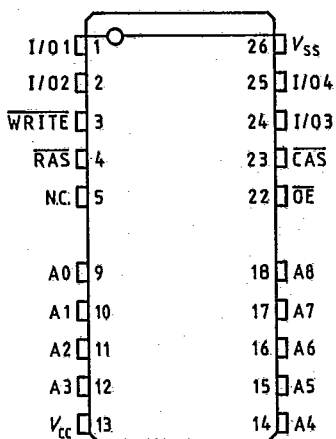
T-46-23-17

Pin Configuration
P-DIP-20-T



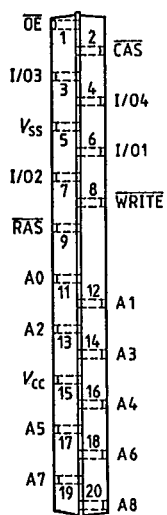
SPP00883

P-SOJ-26/20



SPP00884

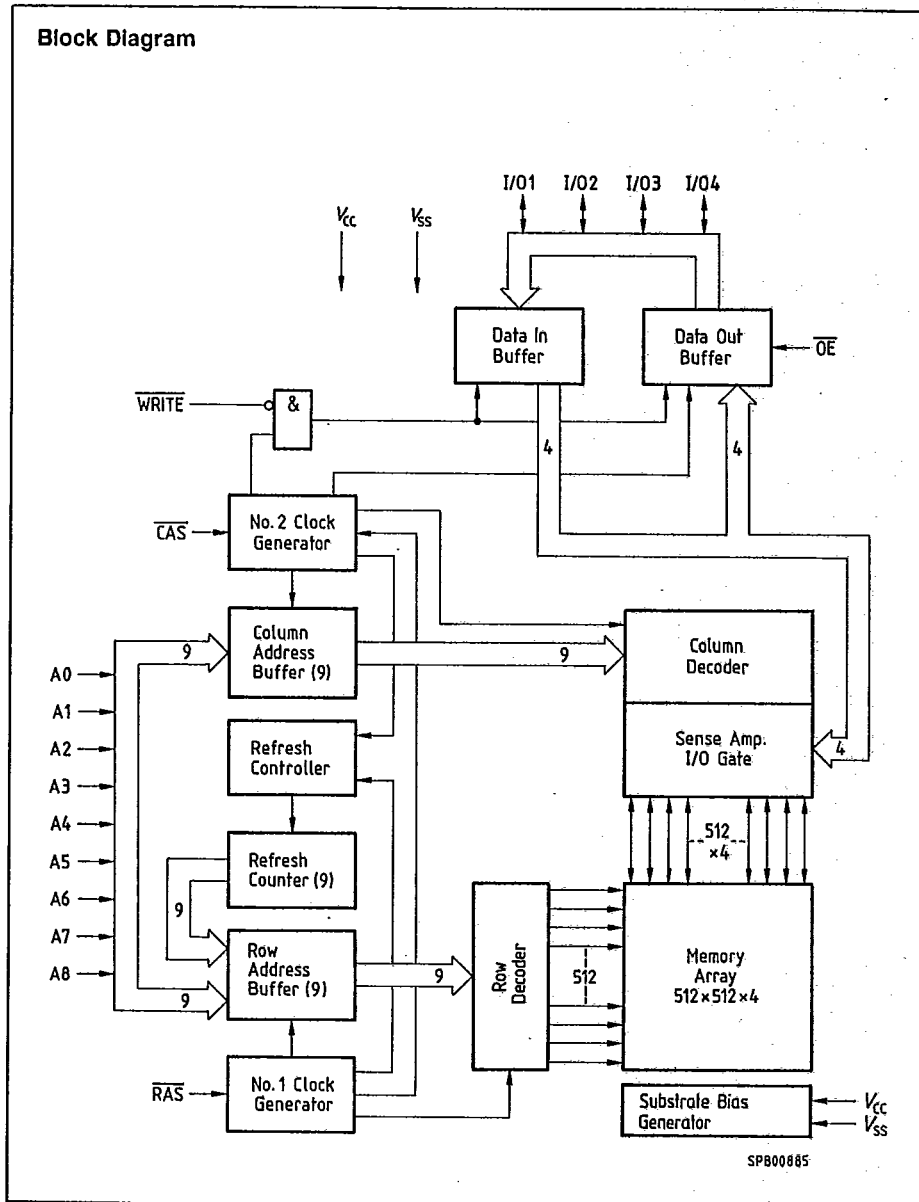
P-ZIP-20/19



SPP00999

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Block Diagram



Absolute Maximum Ratings

Operating temperature range	0 to +70 °C
Storage temperature range	-55 to +150 °C
Soldering temperature	260 °C
Soldering time	10 s
Input/output voltage	-1 to +7 V
Power supply voltage	-1 to +7 V
Power dissipation	0.6 W
Data out current (short circuit)	50 mA

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

$T_A = 0$ to 70 °C, $V_{SS} = 0$ V, $V_{CC} = 5$ V ± 10 %

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input high voltage	V_{IH}	2.4	6.5	-	1)
Input low voltage	V_{IL}	-1.0	0.8	V	1)
Output high voltage ($I_{OUT} = -5$ mA)	V_{OH}	2.4	-	V	-
Output low voltage ($I_{OUT} = 4.2$ mA)	V_{OL}	-	0.4	V	-
Input leakage current, any input (0 V $\leq V_{IN} \leq 6.5$ V, all other pins = 0 V)	$I_{I(L)}$	-10	10	μ A	-
Output leakage current (DO is disabled, 0 V $\leq V_{OUT} \leq 5.5$ V)	$I_{O(L)}$	-10	10	μ A	-
Average V_{CC} supply current: HYB 514256AL-60 HYB 514256AL-70 ($\overline{RAS}$, $\overline{CAS}$, address cycling: $t_{RC} = t_{RC \min.}$)	I_{CC1}	-	90	mA	2) 3)
		-	80	mA	2) 3)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{IH}$)	I_{CC2}	-	2	mA	-

For notes see page 6.

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DC Characteristics (cont'd)

Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Average V_{CC} supply current, during $\overline{RAS}$ only refresh cycles: HYB 514256AL-60 HYB 514256AL-70 ($\overline{RAS}$ cycling, $\overline{CAS} = V_{IH}$, $t_{RC} = t_{RC \min.}$)	I_{CC3}	-	90 80	mA mA	2) 2)
Average V_{CC} supply current, during fast page mode: HYB 514256AL-60 HYB 514256AL-70 ($\overline{RAS} = V_{IL}$, $\overline{CAS}$, address cycling, $t_{PC} = t_{PC \min.}$)	I_{CC4}	-	70 60	mA mA	2) 3) 2) 3)
Standby V_{CC} supply current ($\overline{RAS} = \overline{CAS} = V_{CC} - 0.2 \text{ V}$)	I_{CC5}	-	1	mA	-
Average V_{CC} supply current, during $\overline{CAS}$ -before- $\overline{RAS}$ refresh mode: HYB 514256AL-60 HYB 514256AL-70 ($\overline{RAS}$, $\overline{CAS}$ cycling, $t_{RC} = t_{RC \min.}$)	I_{CC6}	-	90 80	mA mA	2) 2)
Battery backup current average power supply current battery backup mode: ($\overline{CAS} = \overline{CAS}$ before $\overline{RAS}$ cycling or 0.2 V, $\overline{OE} = V_{CC} - 0.2 \text{ V}$, $\overline{WRITE} = V_{CC} - 0.2 \text{ V}$ or 0.2 V, $A0$ to $A8 = V_{CC} - 0.2 \text{ V}$ or 0.2 V, $I/O1$ to $I/O4 = V_{CC} - 0.2 \text{ V}$ or 0.2 V or open, $t_{RC} = 125 \mu\text{s}$, $t_{RAS} = t_{RAS \min.} \sim 1 \mu\text{s}$)	I_{CC7}	-	300	μA	2) 13)

- 1) All voltages are referenced to V_{GS} .
- 2) I_{CC1} , I_{CC3} , I_{CC4} and I_{CC6} depend on cycle rate.
- 3) I_{CC1} and I_{CC4} depend on output loading. Specified values are measured with the output open.
- 13) $t_{RAS} (\text{max.}) = 1 \mu\text{s}$ is only applied to refresh of battery-backup.
 $t_{RAS} (\text{max.}) = 10 \mu\text{s}$ is applied to functional operating.

AC Characteristics ^{4) 5)} $T_A = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $t_T = 5\text{ ns}$

Parameter	Symbol	Limit values				Unit
		HYB 514256AL-60		HYB 514256AL-70		
		min.	max.	min.	max.	
Random read or write cycle time	t_{RC}	110	—	130	—	ns
Read modify write cycle time	t_{RMW}	165	—	185	—	ns
Fast page mode cycle time	t_{PC}	40	—	40	—	ns
Fast page mode RMW cycle time	t_{PRMW}	90	—	95	—	ns
Access time from $\overline{RAS}$ 6) 11)	t_{RAC}	—	60	—	70	ns
Access time from $\overline{CAS}$ 6) 11)	t_{CAC}	—	20	—	20	ns
Access time from column address 6) 12)	t_{AA}	—	30	—	35	ns
Access time from $\overline{CAS}$ precharge 6) 12)	t_{CPA}	—	30	—	35	ns
$\overline{CAS}$ to output in low-Z 4)	t_{CLZ}	0	—	0	—	ns
Output buffer turn-off delay 7)	t_{OFF}	0	20	0	20	ns
Transition time (rise and fall) 5)	T_T	3	50	3	50	ns
$\overline{RAS}$ precharge time	t_{RP}	40	—	50	—	ns
$\overline{RAS}$ pulse width	t_{RAS}	60	10000	70	10000	ns
$\overline{RAS}$ pulse width (fast page mode)	t_{RASP}	60	100000	70	100000	ns
$\overline{RAS}$ hold time	t_{RSH}	20	—	20	—	ns
$\overline{CAS}$ hold time	t_{CSH}	60	—	70	—	ns
$\overline{CAS}$ pulse width	t_{CAS}	20	10000	20	10000	ns
$\overline{RAS}$ to $\overline{CAS}$ delay time 11)	t_{ROD}	20	40	20	50	ns
$\overline{RAS}$ to column address delay time 12)	t_{RAD}	15	30	15	35	ns
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns
$\overline{CAS}$ precharge time	t_{CPN}	10	—	10	—	ns
$\overline{CAS}$ precharge time (fast page mode)	t_{CP}	10	—	10	—	ns
Row address setup time	t_{ASR}	0	—	0	—	ns
Row address hold time	t_{RAH}	10	—	10	—	ns
Column address setup time	t_{ASC}	0	—	0	—	ns
Column address hold time	t_{CAH}	15	—	15	—	ns
Column address hold time referenced to $\overline{RAS}$	t_{AR}	50	—	55	—	ns

For notes see page 9.

AC Characteristics (cont'd) ^{4) 5)}

Parameter	Symbol	Limit values				Unit
		HYB 514256AL-60		HYB 514256AL-70		
		min.	max.	min.	max.	
Column address to $\overline{\text{RAS}}$ lead time	t_{RAL}	30	—	35	—	ns
Read command setup time	t_{RCS}	0	—	0	—	ns
Read command hold time 8)	t_{RCH}	0	—	0	—	ns
Read command hold time referenced to $\overline{\text{RAS}}$ 8)	t_{RRH}	0	—	0	—	ns
Write command hold time	t_{WCH}	15	—	15	—	ns
Write command hold time referenced to $\overline{\text{RAS}}$	t_{WCR}	50	—	55	—	ns
Write command pulse width	t_{WP}	15	—	15	—	ns
Write command to $\overline{\text{RAS}}$ lead time	t_{RWL}	20	—	20	—	ns
Write command to $\overline{\text{CAS}}$ lead time	t_{CWL}	20	—	20	—	ns
Data setup time 9)	t_{DS}	0	—	0	—	ns
Data hold time 9)	t_{DH}	15	—	15	—	ns
Data hold time referenced to $\overline{\text{RAS}}$	t_{DHR}	50	—	55	—	ns
Refresh period	t_{REF}	—	64	—	64	ms
Write command setup time 10)	t_{WCS}	0	—	0	—	ns
$\overline{\text{CAS}}$ to $\overline{\text{WRITE}}$ delay time 10)	t_{CWD}	50	—	50	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{WRITE}}$ delay time 10)	t_{RWD}	90	—	100	—	ns
Column address to $\overline{\text{WRITE}}$ delay time 10)	t_{AWD}	60	—	65	—	ns
$\overline{\text{CAS}}$ setup time (CBR cycle)	t_{CSR}	10	—	10	—	ns
$\overline{\text{CAS}}$ hold time (CBR cycle)	t_{CHR}	30	—	30	—	ns
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ precharge time	t_{RPC}	0	—	0	—	ns
$\overline{\text{CAS}}$ precharge time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ counter test cycle)	t_{CPT}	40	—	40	—	ns
$\overline{\text{RAS}}$ hold time referenced to $\overline{\text{OE}}$	t_{ROH}	10	—	10	—	ns
$\overline{\text{OE}}$ access time	t_{OEA}	—	20	—	20	ns
$\overline{\text{OE}}$ to data delay	t_{OED}	20	—	20	—	ns
Output buffer turn-off delay time from $\overline{\text{OE}}$	t_{OEZ}	0	20	0	20	ns
$\overline{\text{OE}}$ command hold time	t_{OEH}	20	—	20	—	ns

For notes see page 9.

Capacitance $T_A = 0$ to 70°C , $V_{CC} = 5\text{ V} \pm 10\%$, $f = 1\text{ MHz}$

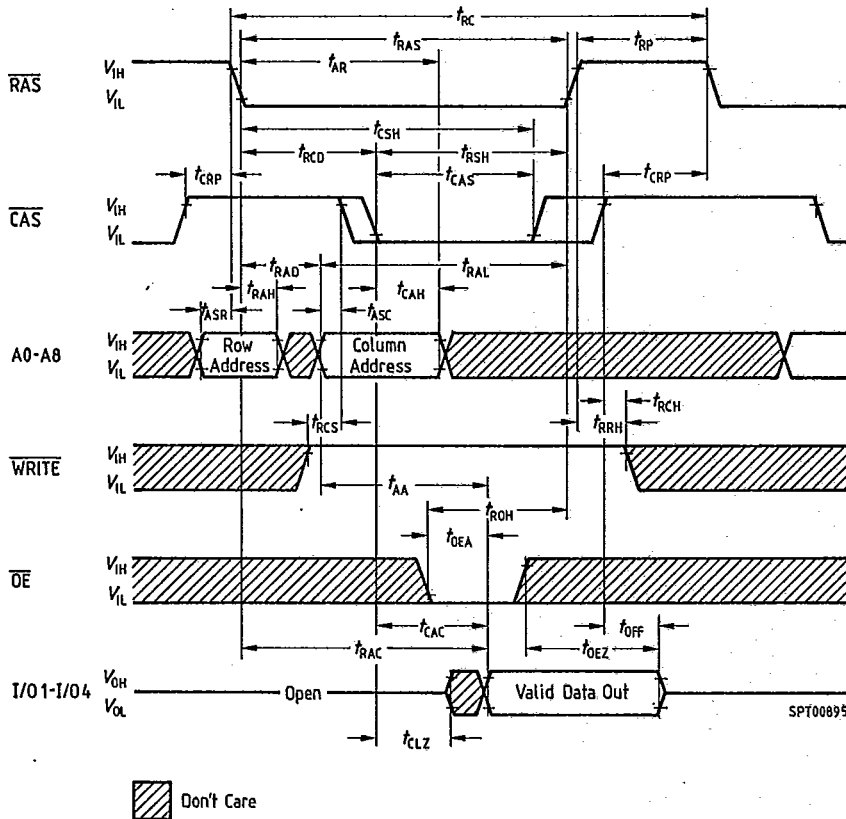
Parameter	Symbol	Limit values		Unit	Test condition
		min.	max.		
Input capacitance (A0 to A8, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	C_{i1}	—	6	pF	—
I/O capacitance	C_{iO}	—	7	pF	—

Notes for pages 7 and 8

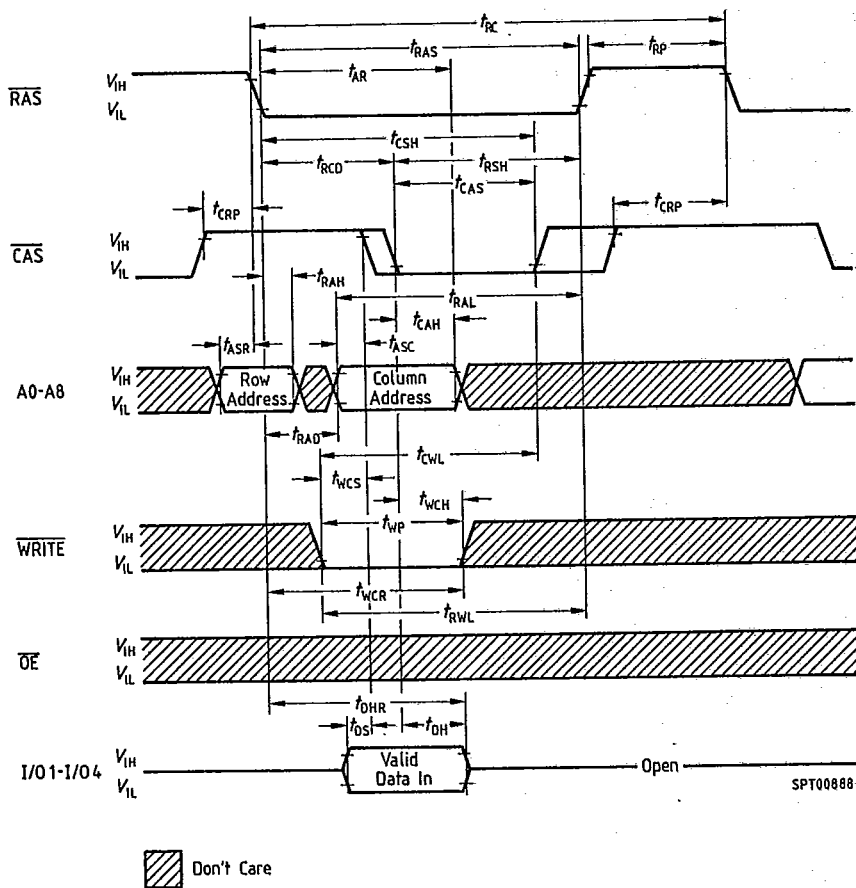
- 4) An initial pause of 200 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ initialization cycles instead of 8 $\overline{\text{RAS}}$ cycles are required.
- 5) V_{IH} (min.) and V_{IL} (max.) are reference levels for measuring timing of input signals. Transition times are also measured between V_{IH} and V_{IL} .
- 6) Measured with a load equivalent of 2 TTL loads and 100 pF.
- 7) t_{OFF} (max.) defines the time at which the output achieves the open-circuit conditions and is not referenced to output voltage levels.
- 8) Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
- 9) These parameters are referenced to the $\overline{\text{CAS}}$ leading edge in early write cycles and the $\overline{\text{WRITE}}$ leading edge in read-write cycles.
- 10) t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restricted operation parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$ the cycle is an early write cycle and data out pin will remain open-circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, and $t_{AWD} \geq t_{AWD}(\text{min.})$ the cycle is a read-modify-write cycle and data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of data out (at access time) is indeterminate.
- 11) Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
- 12) Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .

Waveforms

Read Cycle

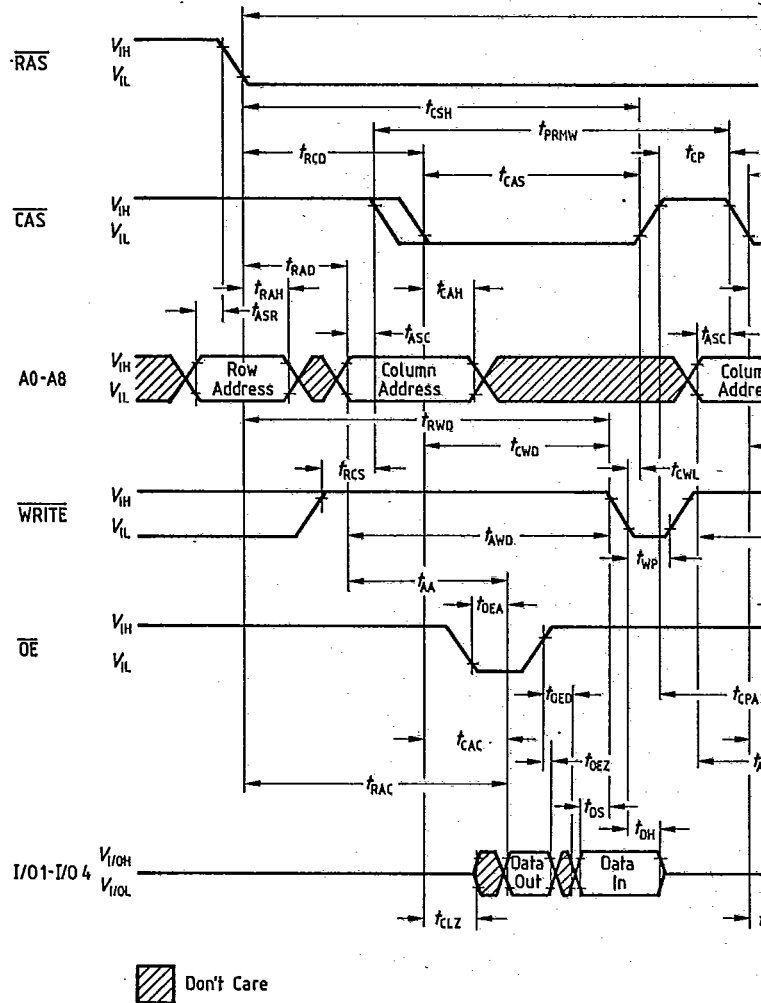


Write Cycle (early write)



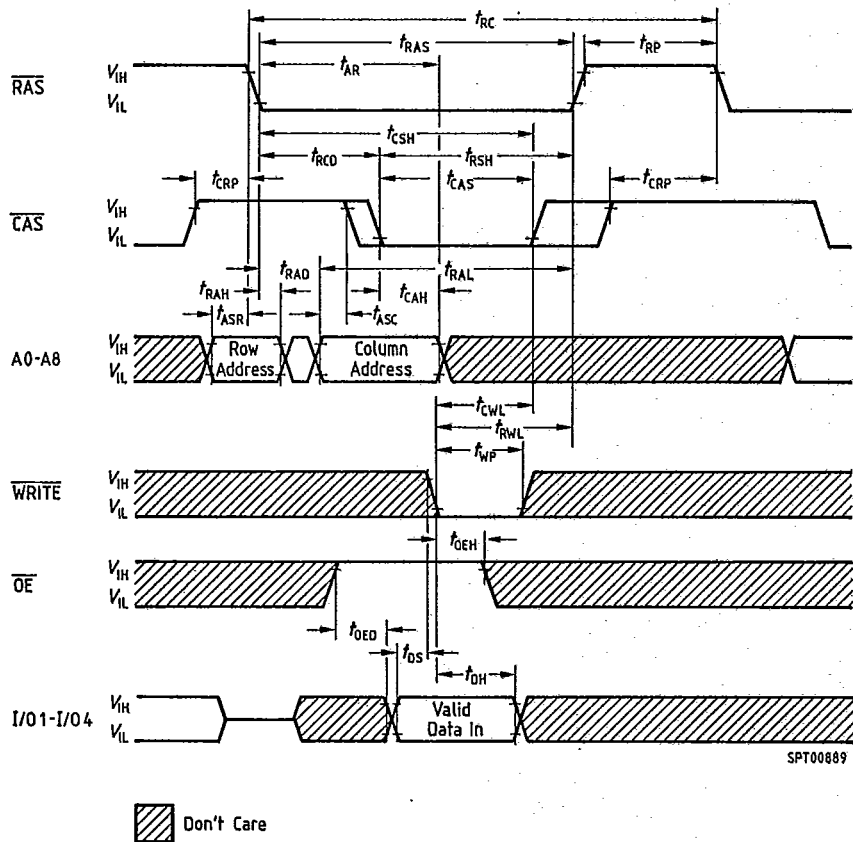
SPT00888

Fast Page Mode Read-Modify-Write Cycle



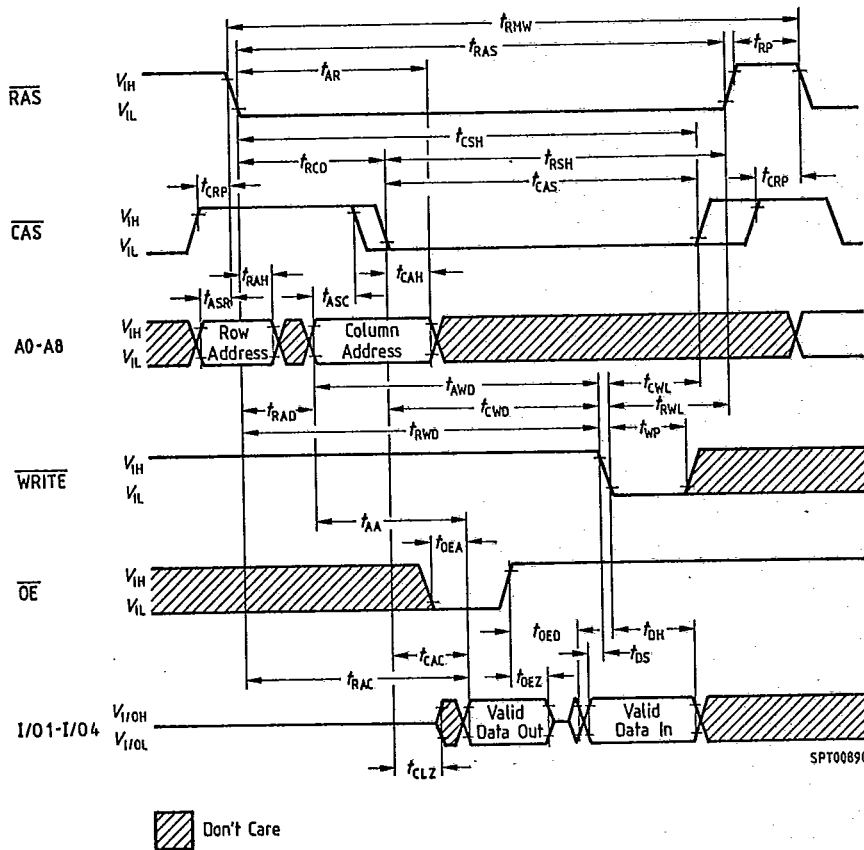


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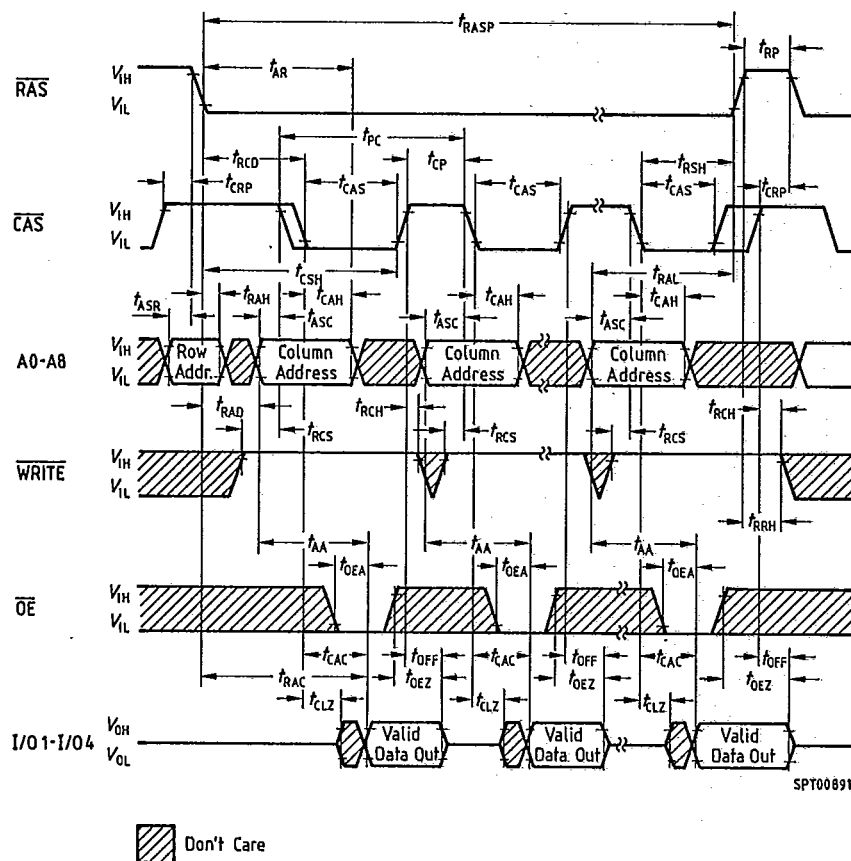
Write Cycle ($\overline{OE}$ controlled write)

SPT00889

Read-Write (read-modify-write) Cycle

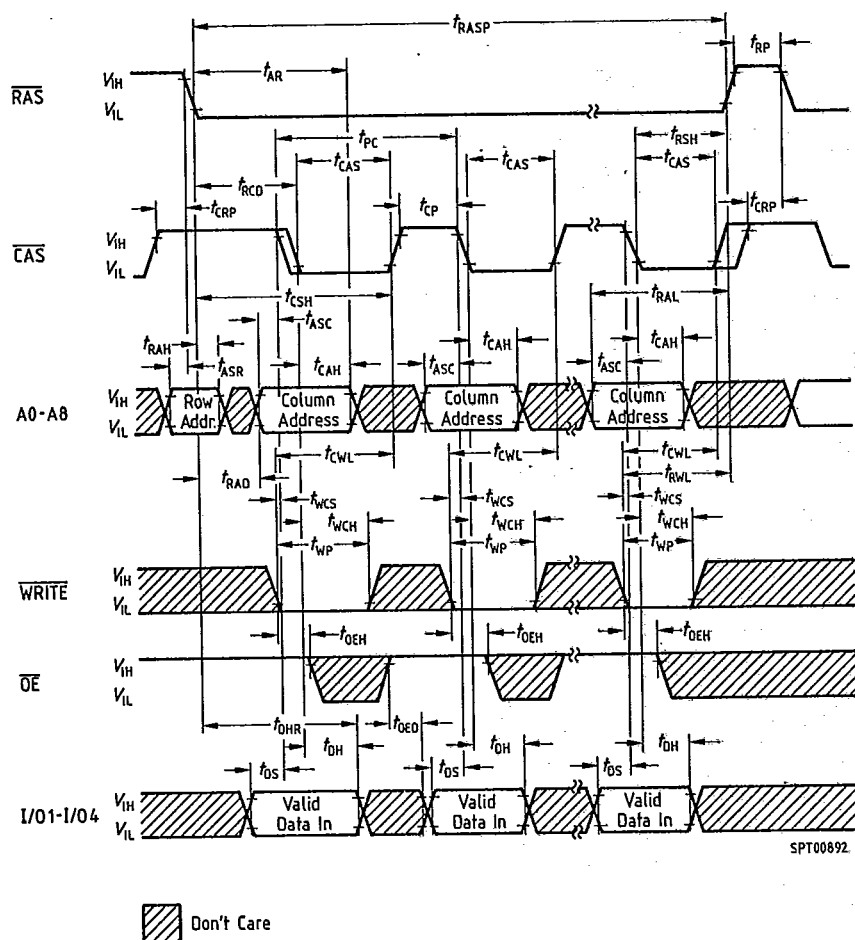


Fast Page Mode Read Cycle



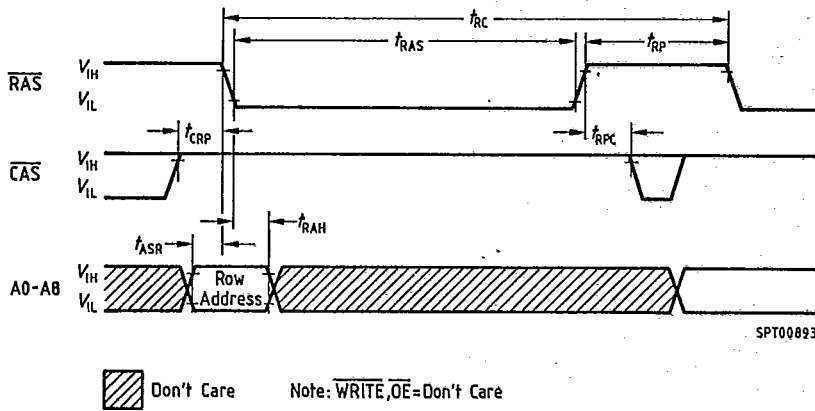
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Fast Page Mode Write Cycle



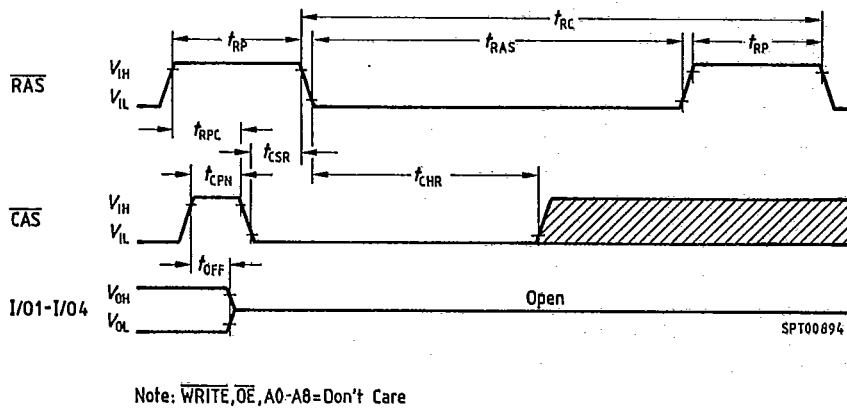
SPT00892

RAS-Only Refresh Cycle



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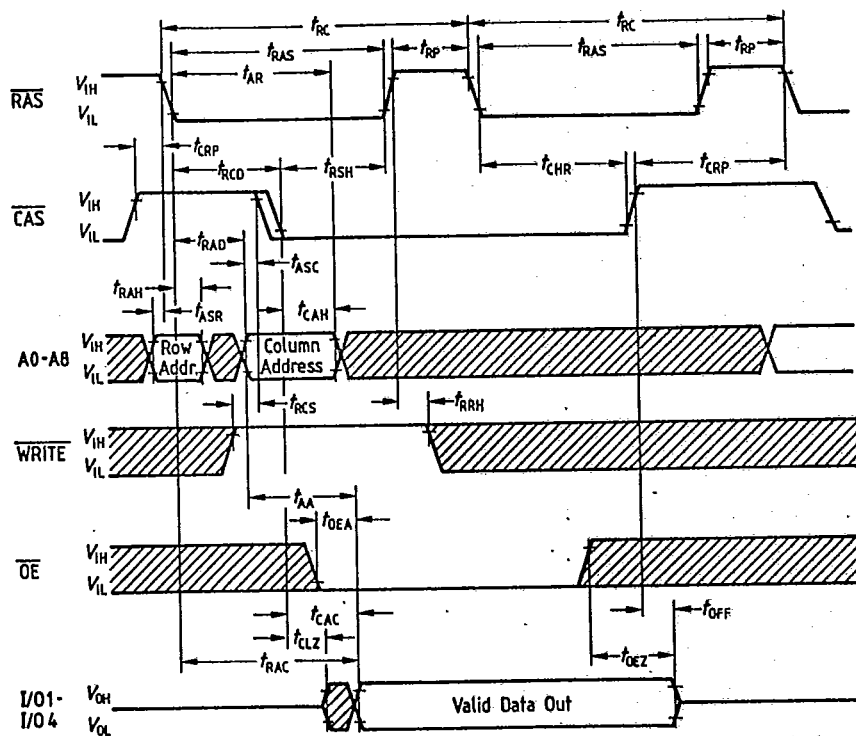
CAS-Before-RAS Refresh Cycle



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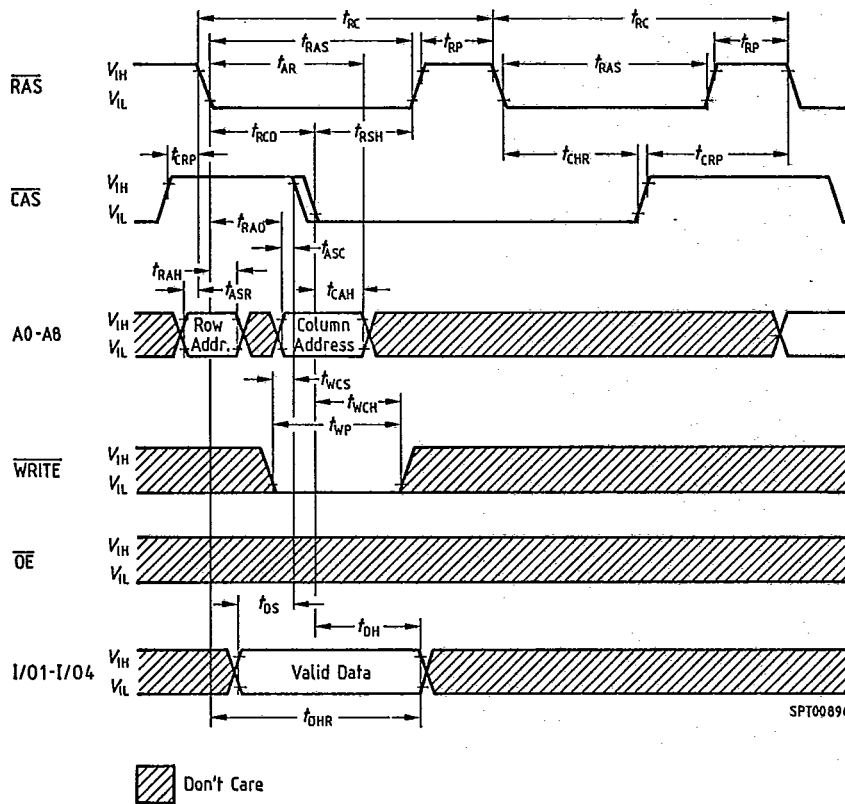
Hidden Refresh Cycle (read)



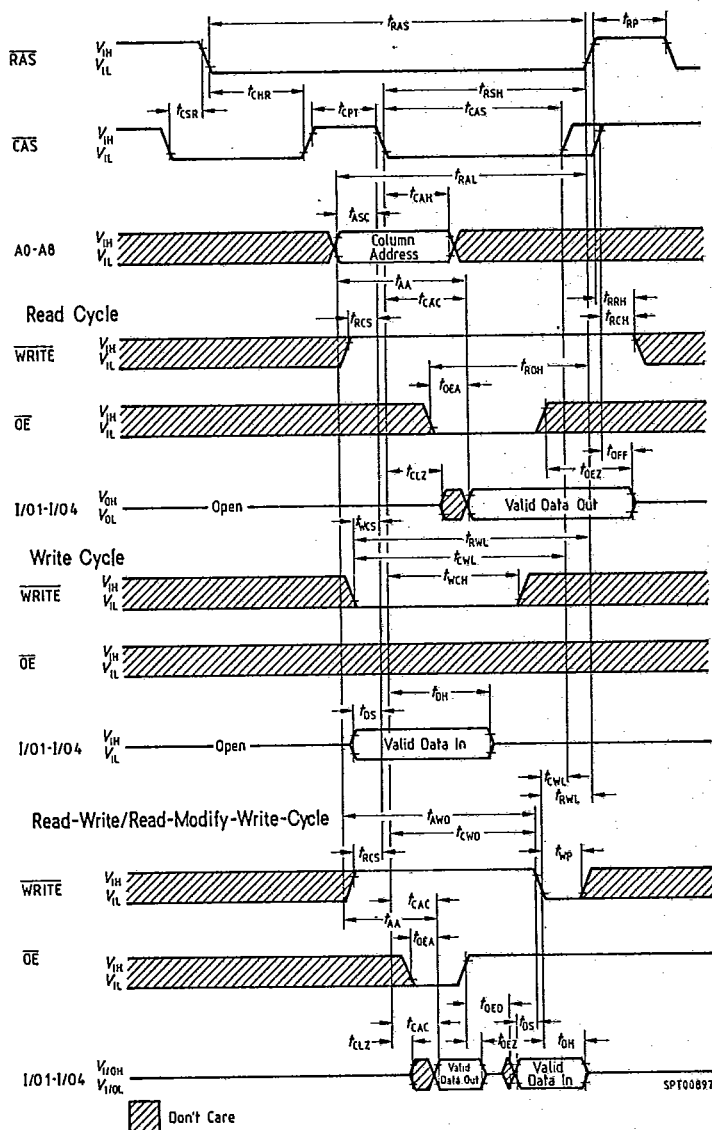
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Don't Care

Hidden Refresh Cycle (write)



CAS-Before-RAS Refresh Counter Test Cycle

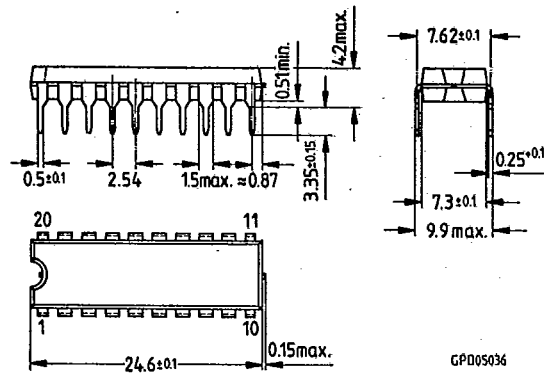


Package Outlines

Plastic Package, P-DIP-20-T

(dual-in-line-package)

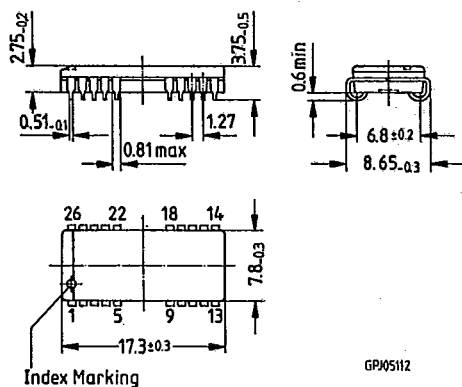
20A20DIN41870 T9



Dimensions in mm

Plastic Package, P-SOJ-26/20

(Plastic small outline J-lead) - SMD

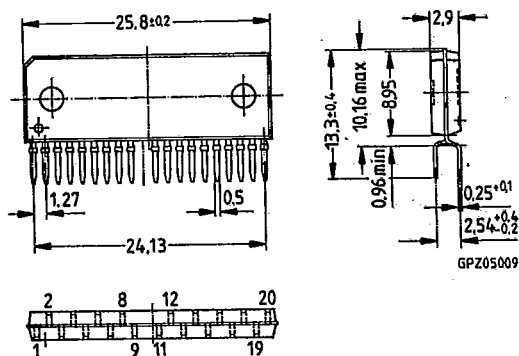


Dimensions in mm

T-46-23-17

Package Outlines (cont'd)

Plastic Package, P-ZIP-20/19
 (JEDEC-MO-072-AA)



Dimensions in mm