

3.3 V 168-pin Registered SDRAM Modules

PC133 128 MByte Module

PC133 256 MByte module

PC133 512 MByte Module

PC133 1 GByte Module

PC133 2 GByte Module

- 168-pin Registered 8 Byte Dual-In-Line SDRAM Module for PC and Server main memory applications
- One bank 16M × 72, 32M × 72, 64M × 72 and 128M × 72, two bank 128M × 72 and 256M × 72 organization
- Optimized for ECC applications with very low input capacitances
- JEDEC standard Synchronous DRAMs (SDRAM) Programmable $\overline{\text{CAS}}$ Latency, Burst Length and Wrap Sequence (Sequential & Interleave)
- Single + 3.3 V (± 0.3 V) power supply
- Auto Refresh (CBR) and Self Refresh
- Performance:
- Programmable $\overline{\text{CAS}}$ Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- All inputs and outputs are LVTTTL compatible
- Serial Presence Detect with E²PROM
- Utilizes SDRAMs in TSOPII-54 packages with registers and PLL.
- Card Size: 133.35 mm × 38.10 / 43.18 mm with Gold contact pads (JEDEC MO-161)
- These modules all fully compatible with the current industry standard PC133 and PC100 specifications

speed grade		-7	-7.5	Unit
f_{CK}	Clock Frequency (max.) @ CL = 3	133	133	MHz
t_{CK}	Clock Cycle Time (min.) @ CL = 3	7.5	7.5	ns
t_{AC}	Clock Access Time (min.) @ CL= 3	5.4	5.4	ns
f_{CK}	Clock Frequency (max.) @ CL = 2	133	100	MHz
t_{CK}	Clock Cycle Time (min.) @ CL = 2	7.5	10	ns
t_{AC}	Clock Access Time (min.) @ CL= 2	5.4	6	ns

Description

The HYS 72Vxx3xxGR-7 and -7.5 are industry standard 168-pin 8-byte Dual in-line Memory Modules (DIMMs) organized as 16M × 72, 32M × 72, 64M × 72, 128M × 72 and 256M × 72 high speed memory arrays designed with Synchronous DRAMs (SDRAMs) for ECC applications. All control and address signals are registered on-DIMM and the design incorporates a PLL circuit for the Clock inputs. Use of an on-board register reduces capacitive loading on the input signals but are delayed by one cycle in arriving at the SDRAM devices. Decoupling capacitors are mounted on the PC board. The DIMMs use a serial presence detects scheme implemented via a serial E²PROM using the 2-pin I²C protocol. The first 128 bytes are utilized by the DIMM manufacturer and the second 128 bytes are available to the end user. All Infineon 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 133.35 mm long footprint.

Ordering Information

Type	Compliance Code	Description	SDRAM Technology
PC133-333:			
HYS 72V16300GR-7.5-C HYS 72V16300GR-7.5-E	PC133R-333-542-B2	one bank 128 MB Reg. DIMM	64 MBit (x4)
HYS 72V16301GR-7.5-C2	PC133R-333-542-B2	one bank 128 MB Reg. DIMM	128 MBit (x8)
HYS 72V32301GR-7.5-C2	PC133R-333-542-B2	one bank 256 MB Reg. DIMM	128 Mbit (x4)
HYS 72V32300GR-7.5-C2 HYS 72V32300GR-7.5-D	PC133R-333-542-AA	one bank 256 MB Reg. DIMM	256 Mbit (x8)
HYS 72V64300GR-7.5-C2 HYS 72V64300GR-7.5-D	PC133R-333-542-B2	one bank 512 MB Reg. DIMM	256 MBit (x4)
HYS 72V128320GR-7.5-C2 HYS 72V128320GR-7.5-D	PC133R-333-542-B2	two banks 1 GByte Reg. DIMM	256 MBit(x4, stacked)
HYS 72V128300GR-7.5-A	PC133R-333-542-B2	one bank 1 GByte Reg. DIMM	512 MBit (x4)
HYS 72V256320GR-7.5-A	PC133R-333-542-B2	two banks 2 GByte Reg. DIMM	512 MBit(x4, stacked)
PC133-222:			
HYS 72V16300GR-7-E	PC133R-222-542-B2	one bank 128 MB Reg. DIMM	64 MBit (x4)
HYS 72V16301GR-7-C2	PC133R-222-542-B2	one bank 128 MB Reg. DIMM	128 MBit (x8)
HYS 72V32301GR-7-C2	PC133R-222-542-B2	one bank 256 MB Reg. DIMM	128 Mbit (x4)
HYS 72V32300GR-7-D	PC133R-222-542-AA	one bank 256 MB Reg. DIMM	256 Mbit (x8)
HYS 72V64300GR-7-D	PC133R-222-542-B2	one bank 512 MB Reg. DIMM	256 MBit (x4)
HYS 72V128320GR-7-D	PC133R-222-542-B2	two banks 1 GByte Reg. DIMM	256 MBit (x4, stacked)
HYS 72V128300GR-7-A	PC133R-222-542-B2	one bank 1 GByte Reg. DIMM	512 MBit (x4)
HYS 72V256320GR-7-A	PC133R-222-542-B2	two banks 2 GByte Reg. DIMM	512 MBit (x4, stacked)

Note: All part numbers end with a place code (not shown), designating the die revision. Consult factory for current revision. Example: HYS 64V32300GR-7.5-D, indicating Rev.D dies are used for SDRAM components.

Pin Definitions and Functions

A0 - A11, A12	Address Inputs (A12 is used for 256Mbit based modules only)	DQMB0 - DQMB7	Data Mask
BA0, BA1	Bank Selects	$\overline{CS0} - \overline{CS3}$	Chip Select
DQ0 - DQ63	Data Input/Output	REGE*)	Register Enable "H" or N.C = registered mode "L" = buffered mode
CB0 - CB7	Check Bits	V_{DD}	Power (+ 3.3 V)
$\overline{RAS}$	Row Address Strobe	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	SCL	Clock for Presence Detect
$\overline{WE}$	Read/Write Input	SDA	Serial Data Out
CKE0	Clock Enable	N.C.	No Connection
CLK0 - CLK3	Clock Input	—	—

Note: To confirm to this specification, motherboards must pull this pin to high state or no connect

Address Format

Density	Organization	Memory Banks	SDRAMs	# of SDRAMs	# of row/bank/ columns bits	Refresh	Period	Interval
128 MB	16M × 72	1	16M × 4	18	12/2/10	4k	64 ms	15.6 μs
128 MB	16M × 72	1	16M × 8	9	12/2/10	4k	64 ms	15.6 μs
256 MB	32M × 72	1	32M × 4	18	12/2/11	4k	64 ms	15.6 μs
256 MB	32M × 72	1	32M × 8	9	13/2/10	8k	64 ms	7.8 μs
512 MB	64M × 72	1	64M × 4	18	13/2/11	8k	64 ms	7.8 μs
1 GB	128M × 72	2	64M × 4	36	13/2/11	8k	64 ms	7.8 μs
1 GB	128M × 72	1	128M × 4	18	13/2/12	8k	64ms	7.8 μs
2 GB	256M × 72	2	128M × 4	36	13/2/12	8k	64ms	7.8 μs

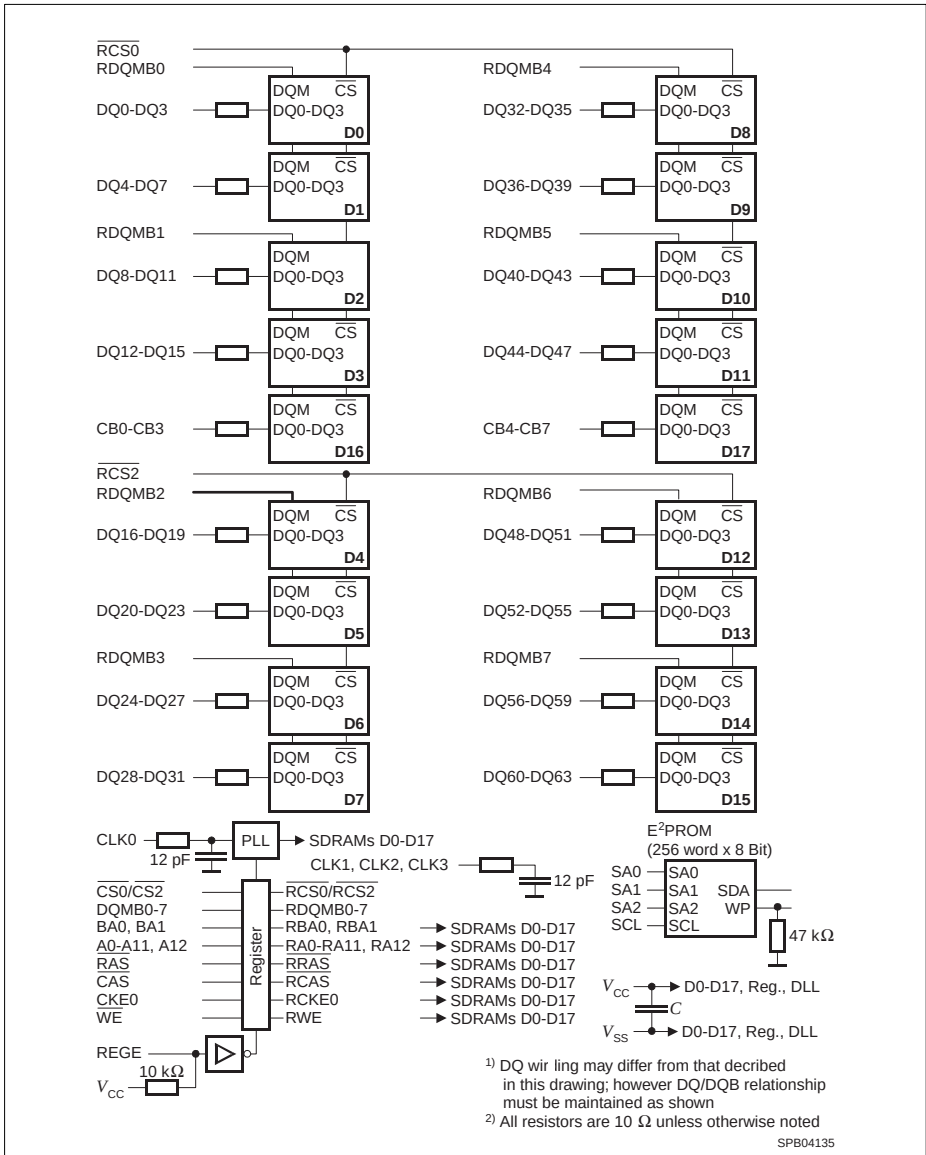
Pin Configuration

PIN#	Symbol
1	V _{SS}
2	DQ0
3	DQ1
4	DQ2
5	DQ3
6	V _{DD}
7	DQ4
8	DQ5
9	DQ6
10	DQ7
11	DQ8
12	V _{SS}
13	DQ9
14	DQ10
15	DQ11
16	DQ12
17	DQ13
18	V _{DD}
19	DQ14
20	DQ15
21	CB0
22	CB1
23	V _{SS}
24	N.C.
25	N.C.
26	V _{DD}
27	WE
28	DQMB0
29	DQMB1
30	CS0
31	DU
32	V _{SS}
33	A0
34	A2
35	A4
36	A6
37	A8
38	A10 (AP)
39	BA1
40	V _{DD}
41	V _{DD}
42	CLK0

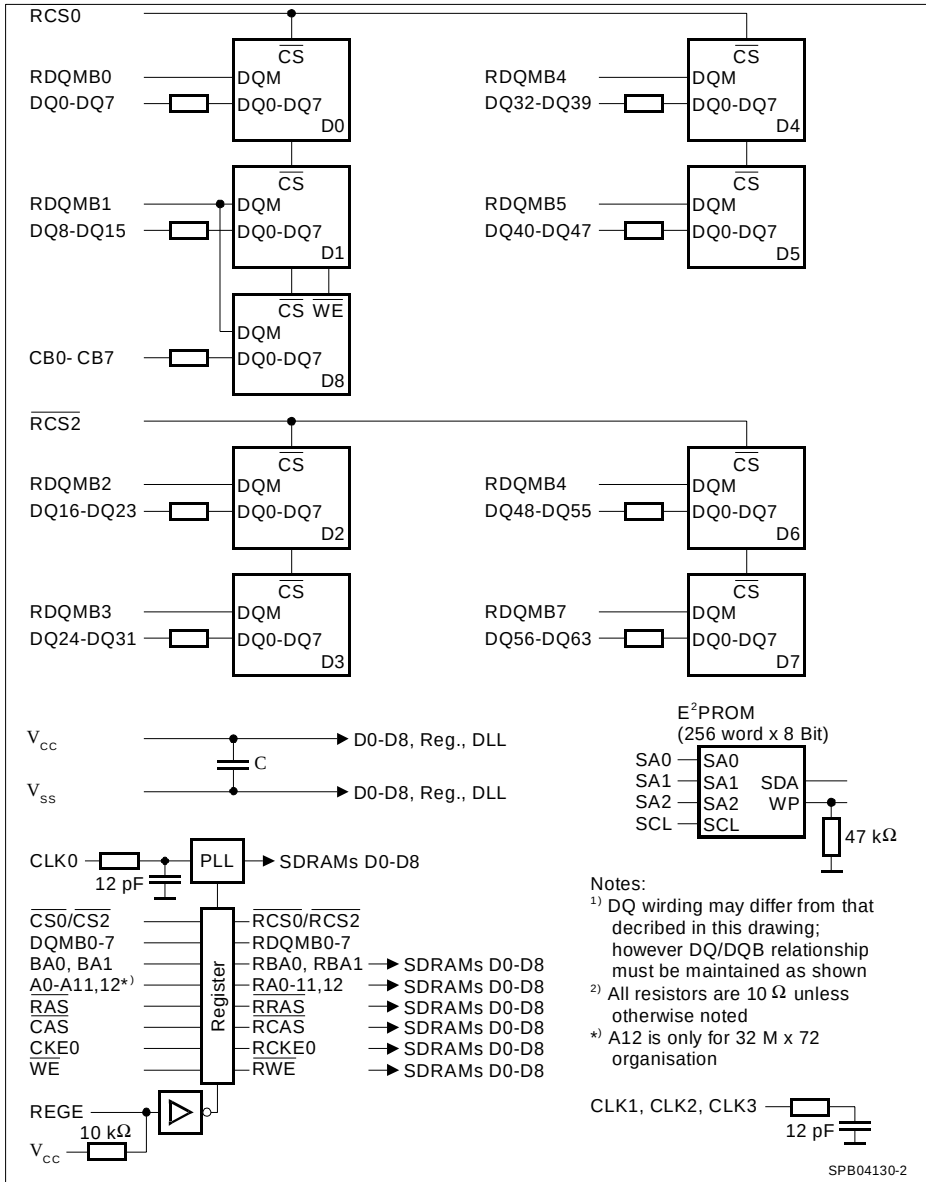
PIN#	Symbol
43	V _{SS}
44	DU
45	CS2
46	DQMB2
47	DQMB3
48	DU
49	V _{DD}
50	N.C.
51	N.C.
52	CB2
53	CB3
54	V _{SS}
55	DQ16
56	DQ17
57	DQ18
58	DQ19
59	V _{DD}
60	DQ20
61	N.C.
62	DU
63	N.C.
64	V _{SS}
65	DQ21
66	DQ22
67	DQ23
68	V _{SS}
69	DQ24
70	DQ25
71	DQ26
72	DQ27
73	V _{DD}
74	DQ28
75	DQ29
76	DQ30
77	DQ31
78	V _{SS}
79	CLK2
80	N.C.
81	WP
82	SDA
83	SCL
84	V _{DD}

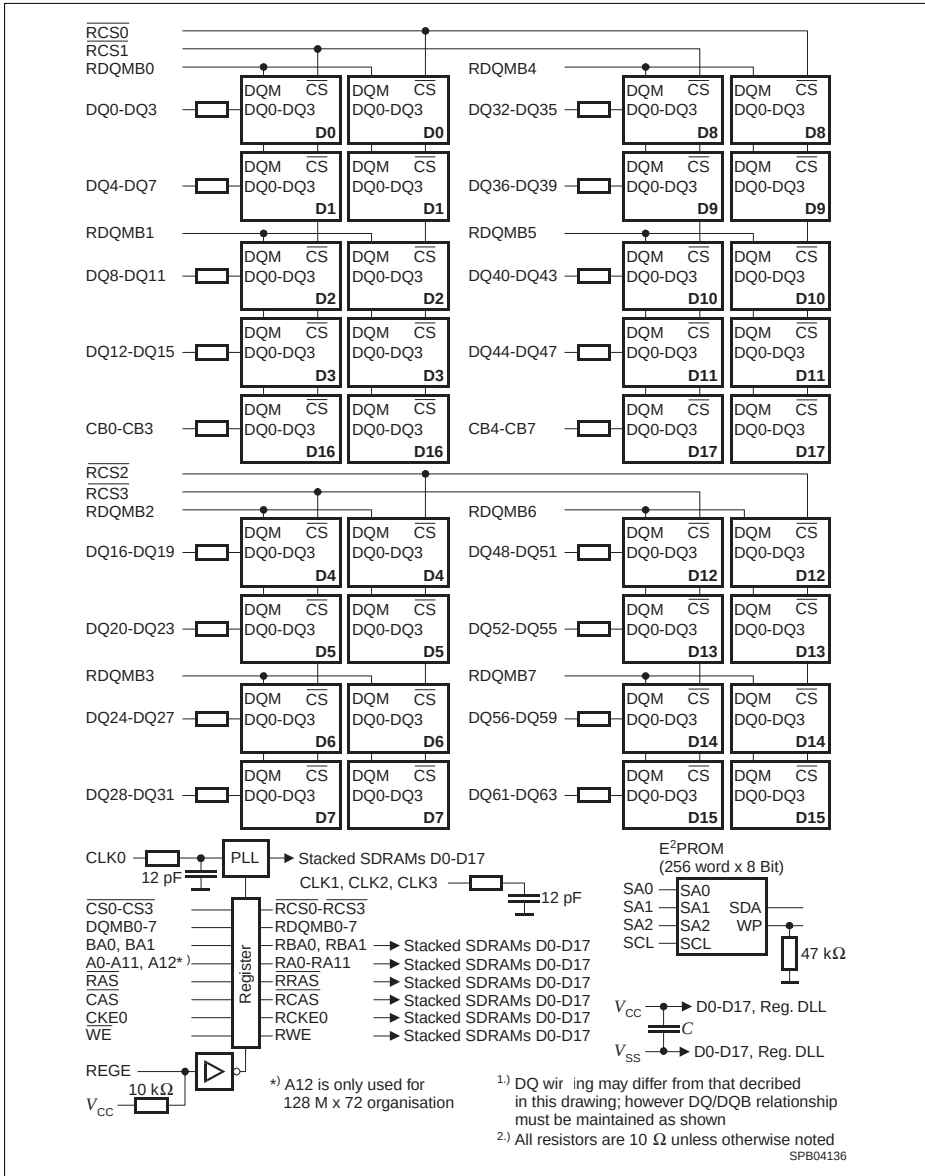
PIN#	Symbol
85	V _{SS}
86	DQ32
87	DQ33
88	DQ34
89	DQ35
90	V _{DD}
91	DQ36
92	DQ37
93	DQ38
94	DQ39
95	DQ40
96	V _{SS}
97	DQ41
98	DQ42
99	DQ43
100	DQ44
101	DQ45
102	V _{DD}
103	DQ46
104	DQ47
105	CB4
106	CB5
107	V _{SS}
108	N.C.
109	N.C.
110	V _{DD}
111	CAS
112	DQMB4
113	DQMB5
114	CS1
115	RAS
116	V _{SS}
117	A1
118	A3
119	A5
120	A7
121	A9
122	BA0
123	A11
124	V _{DD}
125	CLK1
126	A12

PIN#	Symbol
127	V _{SS}
128	CKE0
129	CS3
130	DQMB6
131	DQMB7
132	N.C.
133	V _{DD}
134	N.C.
135	N.C.
136	CB6
137	CB7
138	V _{SS}
139	DQ48
140	DQ49
141	DQ50
142	DQ51
143	V _{DD}
144	DQ52
145	N.C.
146	DU
147	REGE
148	V _{SS}
149	DQ53
150	DQ54
151	DQ55
152	V _{SS}
153	DQ56
154	DQ57
155	DQ58
156	DQ59
157	V _{DD}
158	DQ60
159	DQ61
160	DQ62
161	DQ63
162	V _{SS}
163	CLK3
164	N.C.
165	SA0
166	SA1
167	SA2
168	V _{DD}



Block Diagram: One Bank 16M x 72, 32M x 72, 64M x 72 and 128M x 72 SDRAM DIMM Modules HYS72V16300GR, HYS72V32301GR, HYS72V64300GR and HYS72V128320GR using x4 organized SDRAMs





Block Diagram: Two Bank 128M x 72 and 256M x 72 SDRAM DIMM Modules
HYS 72V128320GR and HYS 72V256320GR Using Stacked x4 Organized SDRAMs

Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	- 1.0	4.6	V
Power supply voltage on V_{DD}	V_{DD}	- 1.0	4.6	V
Storage temperature range	T_{STG}	-55	+150	°C
Power dissipation (per SDRAM component)	P_D	—	1	W
Data out current (short circuit)	I_{OS}	—	50	mA

Permanent device damage may occur if "Absolute Maximum Ratings" are exceeded.
Functional operation should be restricted to recommended operation conditions.
Exposure to higher than recommended voltage for extended periods of time affect device reliability

DC Characteristics

$T_A = 0$ to 70 °C ¹⁾; $V_{SS} = 0$ V; $V_{DD} = 3.3$ V $\pm$ 0.3 V

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input High Voltage	V_{IH}	2.0	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	- 0.5	0.8	V
Output High Voltage ($I_{OUT} = - 4.0$ mA)	V_{OH}	2.4	—	V
Output Low Voltage ($I_{OUT} = 4.0$ mA)	V_{OL}	—	0.4	V
Input Leakage Current, any input (0 V < V_{IN} < 3.6 V, all other inputs = 0 V)	$I_{I(L)}$	- 10	10	µA
Output Leakage Current (DQ is disabled, 0 V < V_{OUT} < V_{DD})	$I_{O(L)}$	- 10	10	µA

Capacitance

$T_A = 0$ to 70 °C ¹⁾; $V_{DD} = 3.3$ V $\pm$ 0.3 V, $f = 1$ MHz

Parameter	Symbol	Limit Values		Unit
		One Bank Modules	Two Bank Modules	
Input Capacitance (all inputs except CLK and CKE)	C_{IN}	10	20	pF
Input Capacitance (CLK)	C_{CLK}	30	30	pF
Input Capacitance (CKE)	C_{CKE}	17	30	pF
Input/Output Capacitance(DQ0 - DQ63, CB0 - CB7)	C_{IO}	10	17	pF
Input Capacitance (SCL, SA0 - 2)	C_{SC}	8	8	pF
Input/Output Capacitance (SDA)	C_{SD}	8	8	pF

Operating Currents per SDRAM Component

$T_A = 0$ to $70\text{ }^{\circ}\text{C}^{1)}$, $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$

Parameter	Test Condition	Symbol	64 Mb	128 Mb	256 Mb	512 Mb	Unit	Note
			max.					
Operating current $t_{RC} = t_{RC(MIN.)}$, $t_{CK} = t_{CK(MIN.)}$ Outputs open, Burst Length = 4, CL = 3. All banks operated in random access, all banks operated in ping-pong manner to maximize gapless data access	—	I_{CC1}	110	160	270	tbd.	mA	2)
Precharge stand-by current in Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, $CKE \leq V_{IL(MAX.)}$	$t_{CK} = \text{min.}$	I_{CC2P}	2	1.5	2	tbd.	mA	2)
Precharge Stand-by Current in Non-Power Down Mode $\overline{CS} = V_{IH(MIN.)}$, $CKE \geq V_{IH(MIN.)}$	$t_{CK} = \text{min.}$	I_{CC2N}	40	40	25	tbd.	mA	2)
No operating current $t_{CK} = \text{min.}$, $\overline{CS} = V_{IH(MIN.)}$, active state (max. 4 banks)	$CKE \geq V_{IH(MIN.)}$	I_{CC3N}	50	50	50	tbd.	mA	2)
	$CKE \leq V_{IL(MAX.)}$	I_{CC3P}	8	10	10	tbd.	mA	2)
Burst operating current $t_{CK} = \text{min.}$, Read command cycling	—	I_{CC4}	70	100	170	tbd.	mA	2), 3)
Auto refresh current $t_{CK} = \text{min.}$, Auto Refresh command cycling	—	I_{CC5}	140	230	240	tbd.	mA	2)
Self refresh current Self Refresh Mode, $CKE = 0.2\text{ V}$	—	I_{CC6}	1	1.5	2.5	tbd.	mA	2)

AC Characteristics (SDRAM Device Specification) ^{4), 5)}

$T_A = 0 \text{ to } 70 \text{ }^{\circ}\text{C}^1$; $V_{SS} = 0 \text{ V}$; $V_{DD} = 3.3 \text{ V} \pm 0.3 \text{ V}$; $t_T = 1 \text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-7 PC133-222		-7.5 PC133-333			
		min.	max.	min.	max.		

Clock and Access Time

Clock Cycle Time	t_{CK}						
		$\overline{CAS}$ Latency = 3	7.5	–	7.5	–	ns
		$\overline{CAS}$ Latency = 2	7.5	–	10	–	ns
Clock Frequency	f_{CK}						
		$\overline{CAS}$ Latency = 3	–	133	–	133	MHz
		$\overline{CAS}$ Latency = 2	–	133	–	100	MHz
Access Time from Clock	t_{AC}						
		$\overline{CAS}$ Latency = 3	–	5.4	–	5.4	ns
		$\overline{CAS}$ Latency = 2	–	5.4	–	6	ns
Clock High Pulse Width	t_{CH}		2.5	–	2.5	–	ns
Clock Low Pulse Width	t_{CL}		2.5	–	2.5	–	ns
Transition Time	t_T		0.5	7.5	0.5	10	ns

Setup and Hold Parameters

Input Setup Time	t_{IS}	1.5	–	1.5	–	ns	–
Input Hold Time	t_{IH}	0.8	–	0.8	–	ns	–
Power Down Mode Entry Time	t_{SB}	–	1	–	1	CLK	–
Power Down Mode Exit Setup Time	t_{PDE}	1	–	1	–	CLK	–
Mode Register Setup Time	t_{RCS}	2	–	2	–	CLK	–

Common Parameters

Row to Column Delay Time	t_{RCD}	15	–	20	–	ns	–
Row Precharge Time	t_{RP}	15	–	20	–	ns	–
Row Active Time	t_{RAS}	37	–	45	100k	ns	–
Row Cycle Time	t_{RC}	60	–	67.5	–	ns	–
Activate (a) to Activate (b) Command Period	t_{RRD}	2	–	2	–	CLK	–
$\overline{CAS}$ (a) to $\overline{CAS}$ (b) Command Period	t_{CCD}	1	–	1	–	CLK	–

AC Characteristics (SDRAM Device Specification) (cont'd) ^{4), 5)}

$T_A = 0$ to $70\text{ }^{\circ}\text{C}$ ¹⁾; $V_{SS} = 0\text{ V}$; $V_{DD} = 3.3\text{ V} \pm 0.3\text{ V}$; $t_T = 1\text{ ns}$

Parameter	Symbol	Limit Values				Unit	Note
		-7 PC133-222		-7.5 PC133-333			
		min.	max.	min.	max.		

Refresh Cycle

Refresh Period	t_{REF}	—	15.6	—	15.6	μs	—
64&128MBit SDRAM Based Modules		—	7.8	—	7.8	μs	
256&512MBit SDRAM Based Modules							
Self Refresh Exit Time	t_{SREX}	1	—	1	—	CLK	⁶⁾

Read Cycle

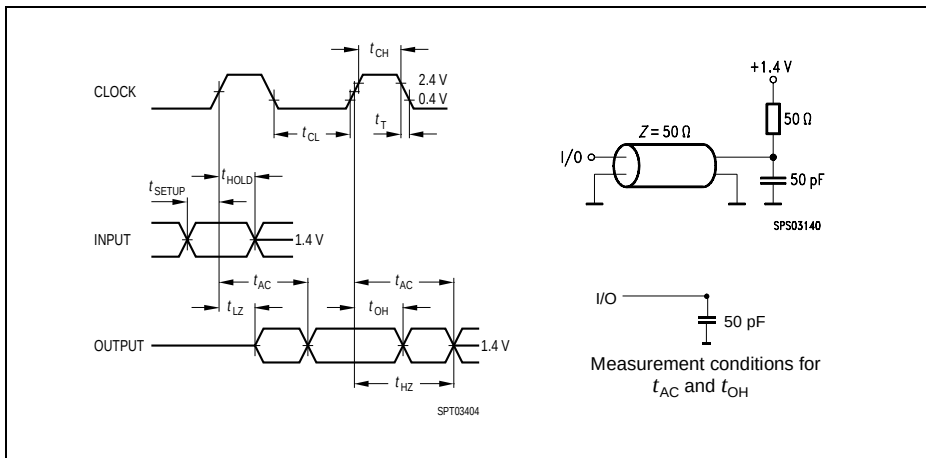
Data Out Hold Time	t_{OH}	3	—	3	—	ns	—
Data Out to Low Impedance Time	t_{LZ}	0	—	0	—	ns	⁷⁾
Data Out to High Impedance Time	t_{HZ}	3	7	3	7	ns	⁷⁾
DQM Data Out Disable Latency	t_{DQZ}	—	2	—	2	CLK	—

Write Cycle

Data Input to Precharge (write recovery)	t_{WR}	2	—	2	—	CLK	—
DQM Write Mask Latency	t_{DQW}	0	—	0	—	CLK	—

Notes

1. The registered DIMM modules are designed to operate under system operating conditions between 0-55 deg C ambient, maximum sustained bandwidth and 0 LFM airflow.
2. These parameters depend on the cycle rate. All values are measured at 133 MHz operation frequency. Input signals are changed once during tck excepts for Icc6 and for standby currents when tck = infinity.
3. These parameters are measured with continous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the data-out current is excluded.
4. An initial pause of 100 μ s is required after power-up. Then a Precharge All Banks command must be given followed by eight Auto Refresh (CBR) cycles before the Mode Register Set Operation can begin. Also the on-DIMM PLL must be given enough clock cycles to stabilize (t_{STAB}) before any operation can be guaranteed.
5. AC timing tests have $V_{IL} = 0.8$ V and $V_{IH} = 2.0$ V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL} . All AC measurements assume $t_T = 1$ ns with the AC output load circuit shown. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with a input signal of 1 V/ns edge rate between 0.8 V and 2.0 V.
6. Self Refresh Exit is a synchronous operation and begins on the second positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied after the Self Refresh Exit command is registered.
7. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.



A serial presence detect storage device - E²PROM 34C02 - is assembled onto the module. Information about the module configuration, speed, etc. is written into the E²PROM device during module production using a serial presence detect protocol (I²C synchronous 2-wire bus).

SPD-Table for -7.5 Registered DIMM Modules

Byte#	Description	SPD Entry Value	Hex							
			128 MB 1 Bank 1)	128 MB 1 Bank 2)	256 MB 1 Bank*)	256 MB 1 Bank**)	512 MB 1 Bank	1 GB 2 Banks	1 GB 1 Bank	2 GB 2 Banks
0	Number of SPD Bytes	128	80							
1	Total Bytes in Serial PD	256	08							
2	Memory Type	SDRAM	04							
3	Number of Row Addresses	12/13	0C	0C	0C	0D	0D	0D	0D	0D
4	Number of Column Addresses	10/11/12	0A	0A	0B	0A	0B	0B	0C	0C
5	Number of DIMM Banks	1/2	01	01	01	01	01	02	01	02
6	Module Data Width	72	48							
7	Module Data Width (cont'd)	0	00							
8	Module Interface Levels	LVTTTL	01							
9	Cycle Time at CL = 3	7.5 ns	75							
10	Access Time from Clock at CL = 3	5.4 ns	54							
11	DIMM Config (Error Det/Corr.)	ECC	02							
12	Refresh Rate/Type	15.6/7.8 μ s	80	80	80	82	82	82	82	82
13	SDRAM Width, Primary	x4 / x8	04	08	04	08	04	04	04	04
14	Error Checking SDRAM Data Width	x4 / x8	04	08	04	08	04	04	04	04
15	Minimum t_{CCD}	1 CLK	01							
16	Burst Length Supported	1, 2, 4, 8 & (full page)	8F	0F	0F	0F	0F	0F	0F	0F
17	Number of SDRAM Banks	4	04							
18	SDRAM Supported CAS Latencies	2 & 3	06							
19	SDRAM CS Latencies	0	01							
20	SDRAM WE Latencies	0	01							
21	SDRAM DIMM Module Attributes	with PLL	1F							
22	SDRAM Device Attributes	V_{DD} tol +/- 10%	0E							
23	Min. Clock Cycle Time at CL = 2	10 ns	A0							
24	Max. Data Access Time from Clock for CL = 2	6.0 ns	60							
25	Min. Clock Cycle Time at CL = 1	not supported	00							
26	Max. Data Access Time from Clock at CL = 1	not supp.	00							
27	SDRAM Minimum t_{RP}	20 ns	14							
28	SDRAM Minimum t_{RRD}	15 ns	0F							
29	SDRAM Minimum t_{RCD}	20 ns	14							
30	SDRAM Minimum t_{RAS}	45 ns	2D							
31	Module Bank Density (per bank)	128 MByte 256 Mbyte 512 MByte 1 GByte	20	20	40	40	80	80	01	01

SPD-Table for -7.5 Registered DIMM Modules (cont'd)

Byte#	Description	SPD Entry Value	Hex							
			128 MB 1 Bank 1)	128 MB 1 Bank 2)	256 MB 1 Bank*)	256 MB 1 Bank**)	512 MB 1 Bank	1 GB 2 Banks	1 GB 1 Bank	2 GB 2 Banks
32	SDRAM Input Setup Time	1.5 ns	15							
33	SDRAM Input Hold Time	0.8 ns	08							
34	SDRAM Data Input Setup Time	1.5 ns	15							
35	SDRAM Data Input Hold Time	0.8 ns	08							
36-61	Superset Information (may be used in future)	–	00							
62	SPD Revision	JEDEC 2	02							
63	Checksum for Bytes 0 - 62	–	C8	50	69	73	AC	AD	2E	2F
64-125	Manufacturer's Information	–								
126	Frequency Specification	–	64							
127	Details of Clocks	–	8F							
128+	Unused Storage Locations	–	FF							

1) HYS72V16300GR-7.5

2) HYS72V16301GR-7.5

*) HYS72V32301GR-7.5

**) HYS72V32300GR-7.5

SPD-Table for -7 Registered DIMM Modules

Byte#	Description	SPD Entry Value	Hex		256 MB 1 Bank*)	256 MB 1 Bank**)	512 MB 1 Bank	1 GB 2 Banks	1 GB 1 Bank	2 GB 2 Banks
			128 MB 1 Bank 1)	128 MB 1 Bank 2)						
0	Number of SPD Bytes	128	80							
1	Total Bytes in Serial PD	256	08							
2	Memory Type	SDRAM	04							
3	Number of Row Addresses	12/13	0C	0C	0C	0D	0D	0D	0D	0D
4	Number of Column Addresses	10/11/12	0A	0A	0B	0A	0B	0B	0C	0C
5	Number of DIMM Banks	1/2	01	01	01	01	01	02	01	02
6	Module Data Width	72	48							
7	Module Data Width (cont'd)	0	00							
8	Module Interface Levels	LVTTTL	01							
9	Cycle Time at CL = 3	7.5 ns	75							
10	Access Time from Clock at CL = 3	5.4 ns	54							
11	DIMM Config (Error Det/Corr.)	ECC	02							
12	Refresh Rate/Type	15.6/7.8 μs	80	80	80	82	82	82	82	82
13	SDRAM Width, Primary	x4 / x8	04	08	04	08	04	04	04	04
14	Error Checking SDRAM Data Width	x4 / x8	04	08	04	08	04	04	04	04
15	Minimum t _{CCD}	1 CLK	01							
16	Burst Length Supported	1, 2, 4, 8 & (full page)	8F	0F	0F	0F	0F	0F	0F	0F
17	Number of SDRAM Banks	4	04							
18	SDRAM Supported CAS Latencies	2 & 3	06							
19	SDRAM CS Latencies	0	01							
20	SDRAM WE Latencies	0	01							
21	SDRAM DIMM Module Attributes	with PLL	1F							
22	SDRAM Device Attributes	V _{DD} tol +/- 10%	0E							
23	Min. Clock Cycle Time at CL = 2	7.5 ns	75							
24	Max. Data Access Time from Clock for CL = 2	5.6 ns	54							
25	Min. Clock Cycle Time at CL = 1	not supported	00							
26	Max. Data Access Time from Clock at CL = 1	not supp.	00							
27	SDRAM Minimum t _{RP}	15 ns	0F							
28	SDRAM Minimum t _{RRD}	14 ns	0E							
29	SDRAM Minimum t _{RCD}	15 ns	0F							
30	SDRAM Minimum t _{RAS}	37 ns	25							

Byte#	Description	SPD Entry Value	Hex							
			128 MB 1 Bank 1)	128 MB 1 Bank 2)						
31	Module Bank Density (per bank)	128 MByte 256 Mbyte 512 MByte 1024 MByte	20	20	40	40	80	80	01	01
32	SDRAM Input Setup Time	1.5 ns	15							
33	SDRAM Input Hold Time	0.8 ns	08							
34	SDRAM Data Input Setup Time	1.5 ns	15							
35	SDRAM Data Input Hold Time	0.8 ns	08							
36-61	Superset Information (may be used in future)	–	00							
62	SPD Revision	JEDEC 2	02							
63	Checksum for Bytes 0 - 62	–	7E	06	1F	29	62	63	E4	E5
64-125	Manufacturer's Information	–								
126	Frequency Specification	–	64							
127	Details of Clocks	–	8F							
128+	Unused Storage Locations	–	FF							

1) HYS72V16300GR-7

2) HYS72V16301GR-7

*) HYS72V32301GR-7

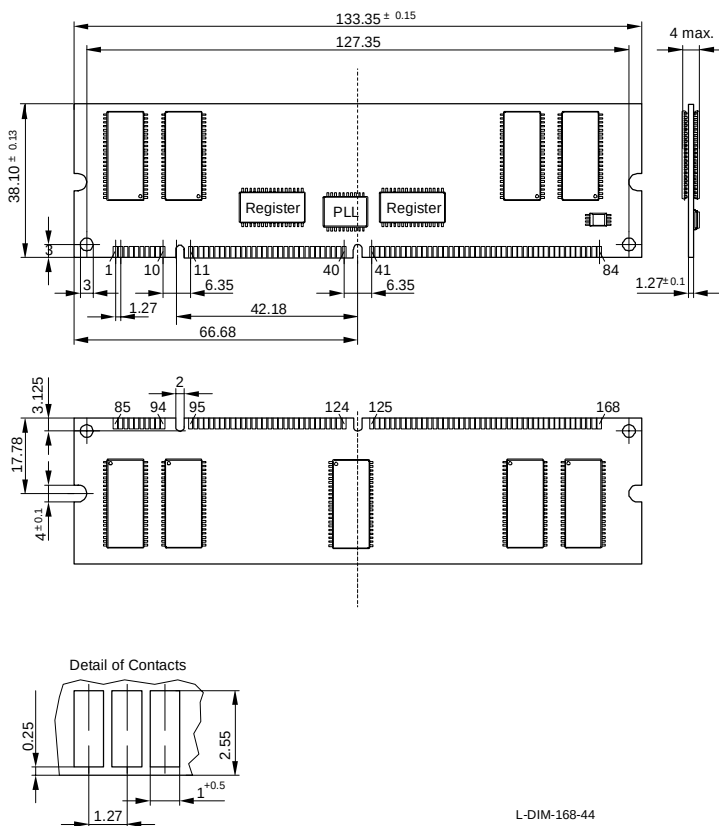
**) HYS72V32300GR-7

Package Outlines for Raw Card AA

Module Package

JEDEC MO-161

Registered DIMM Modules Raw Card AA L-DIM168-44



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

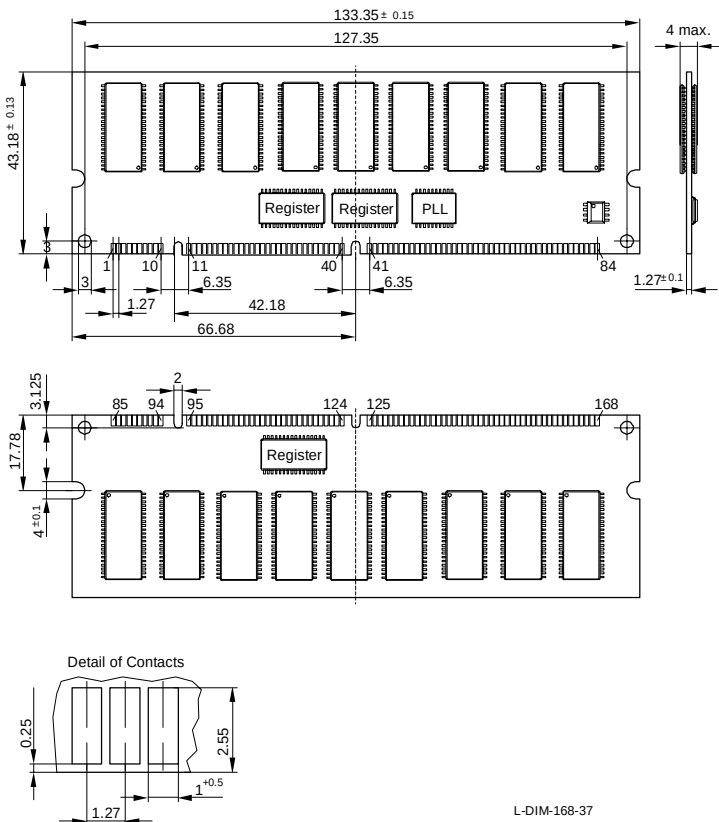
Package Outlines for Raw Card B

Module Package

JEDEC MO-161

Registered DIMM Modules Raw Card B L-DIM168-37

128MB, 256MB, 512MB & 1GB modules based on
x4 SDRAM components



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

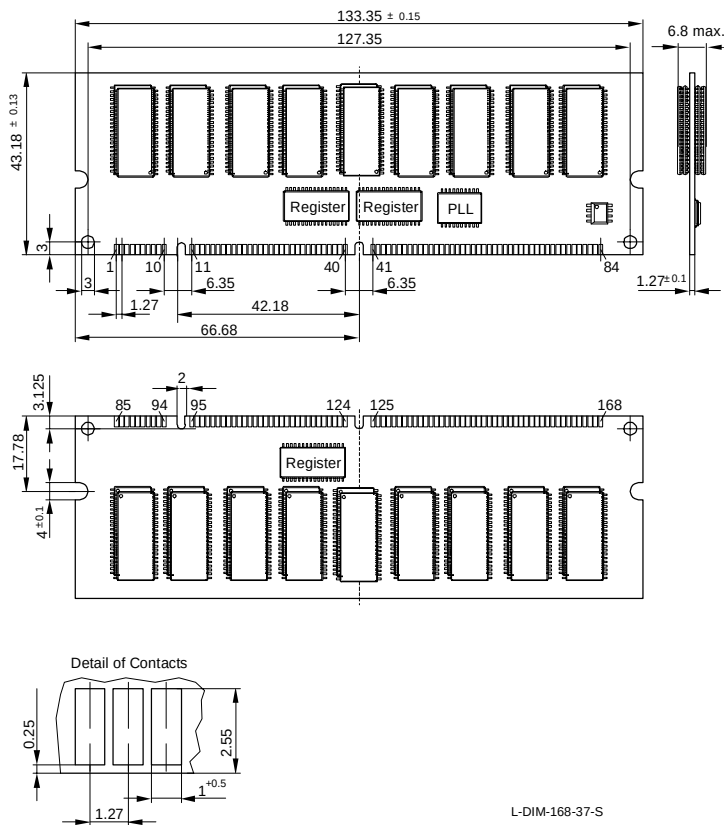
Package Outlines for Raw Card B (with stacked components)

Module Package

JEDEC MO-161

Registered DIMM Modules Raw Card B L-DIM168-37

1 GByte and 2 GByte modules



note: all outline dimensions and tolerances are in accordance with the JEDEC standard

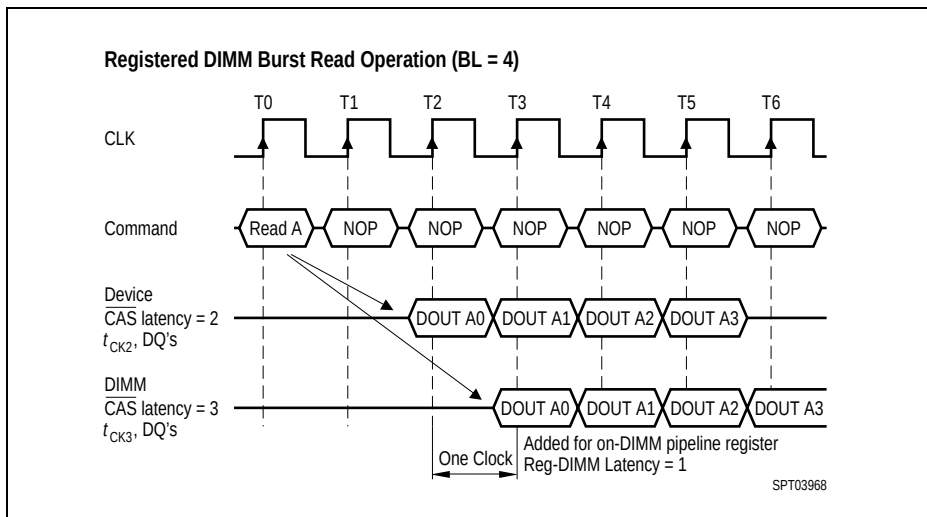
Functional Description

All these PC133 168-pin Registered DIMMs conform to a compatible set of timing and operation characteristics intended to comply with the 133 MHz standards. The Registered DIMMs achieve high speed data transfer rate up to 133 MHz, when in "registered mode". The "registered mode" is achieved when the REGE input signal is in "high" state or the pin is not connected. Operation in "buffered mode" (REGE = "low") needs careful system design to compensate all input signals for the extra delay time of the register components when in "buffered mode". "Buffered mode" is limited to 66 Mhz maximum operation frequency.

Registered Mode:

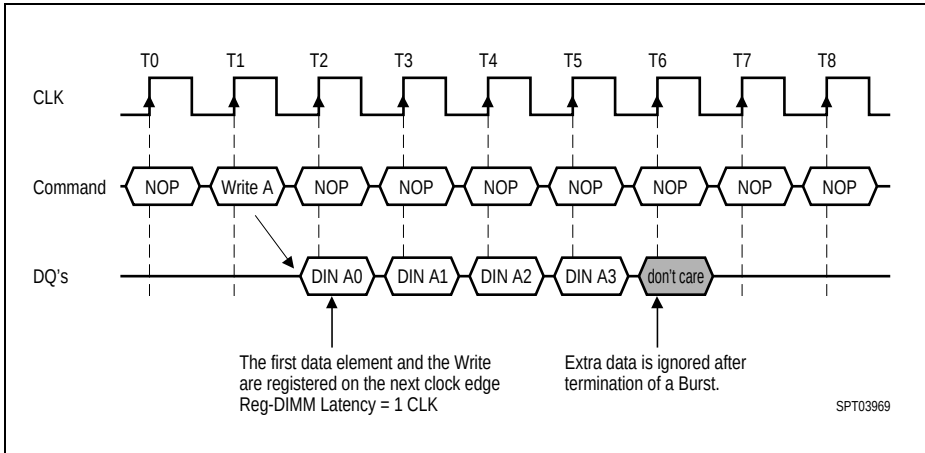
All control and address signals are synchronized with the positive edge of externally supplied clocks and are registered on-DIMM and hence delayed by one clock cycle in arriving at the SDRAM devices. The use of the on-board register reduces the capacitive loading of the DIMM on input control and address signals. The SDRAM device data lines (DQ) are connected directly to the DIMM tabs through 10 Ohm series resistors. All the following timing diagrams and explanations show DIMM operation at the tabs, not SDRAM operation.

The picture below depicts an overview of the effect of the Registered Mode on the data outputs (DQs) for a Read operation. Without the registers, the data is delayed according to the device $\overline{\text{CAS}}$ latency, in the case two clocks. With the register, the data is delayed according to the device $\overline{\text{CAS}}$ latency plus an additional clock cycle. This is known as the DIMM CAS latency, and in this example is four three. The data path can be thought of as a pipeline in which the register effectively lengthens the pipe by one clock cycle.



In case of a Burst Write Command the data-in is delayed one clock due the op-DIMM pipeline register also. Therefore, data for the first Burst Write cycle must be applied on the DQ pins on the next clock cycle after the Write command is issued. the remaining data inputs must be supplied on

each subsequent rising clock edge until the burst length is completed. When the burst has finished, any additional data supplied to the DQ pins will be ignored.



Registered DIMM Burst Write Operation (BL = 4)