

Synchronizing cascaded dual positive edge-triggered D-type flip-flop

74F50728

FEATURES

- Metastable immune characteristics
- Output skew less than 1.5ns
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50109 for synchronizing dual J-K positive edge-triggered flip-flop
- See 74F50729 for synchronizing dual dual D-type flip-flop with edge-triggered set and reset
- Industrial temperature range available (-40°C to $+85^{\circ}\text{C}$)

DESCRIPTION

The 74F50728 is a cascaded dual positive edge-triggered D-type featuring individual data, clock, set and reset inputs; also true and complementary outputs.

Set ($\overline{\text{SDn}}$) and reset ($\overline{\text{RDn}}$) are asynchronous active low inputs and operate independently of the clock (CPn) input. They set and reset both flip-flops of a cascaded pair simultaneously. Data must be stable just one setup time prior to the low-to-high transition of the clock for guaranteed propagation delays.

Clock triggering occurs at a voltage level and is not directly related to the transition time of the positive-going pulse. Following the hold time interval, data at the Dn input may be changed without affecting the levels of the output. Data entering the 74F50728 requires two clock cycles to arrive at the outputs.

The 74F50728 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50728 are: $\tau \approx 135\text{ps}$ and $T_0 \approx 9.8 \times 10^6 \text{ sec}$ where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

| TYPE | TYPICAL f_{max} | TYPICAL SUPPLY CURRENT (TOTAL) |
|----------|--------------------------|--------------------------------|
| 74F50728 | 145 MHz | 23mA |

ORDERING INFORMATION

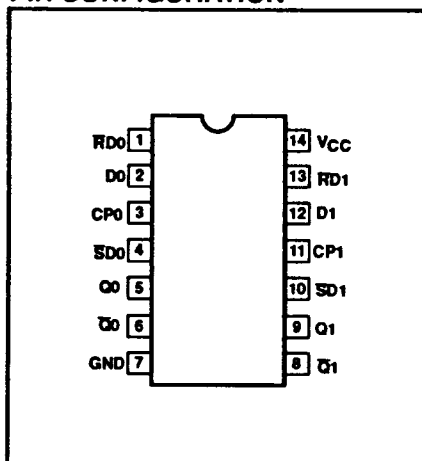
| DESCRIPTION | ORDER CODE | |
|--------------------|---|---|
| | COMMERCIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$, $T_{\text{amb}} = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$ | INDUSTRIAL RANGE $V_{\text{CC}} = 5\text{V} \pm 10\%$, $T_{\text{amb}} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ |
| 14-pin plastic DIP | N74F50728N | I74F50728N |
| 14-pin plastic SO | N74F50728D | I74F50728D |

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

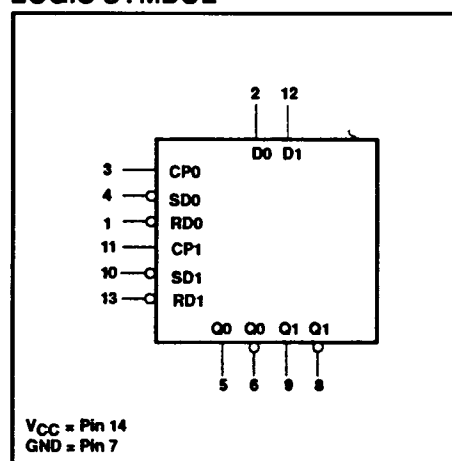
| PINS | DESCRIPTION | 74F (U.L.) HIGH/LOW | LOAD VALUE HIGH/LOW |
|---|-----------------------------------|---------------------|-------------------------------------|
| D0, D1 | Data inputs | 1.0/0.417 | 20 μA /250 μA |
| CP0, CP1 | Clock inputs (active rising edge) | 1.0/1.0 | 20 μA /20 μA |
| $\overline{\text{SD0}}$, $\overline{\text{SD1}}$ | Set inputs (active low) | 1.0/1.0 | 20 μA /20 μA |
| $\overline{\text{RD0}}$, $\overline{\text{RD1}}$ | Reset inputs (active low) | 1.0/1.0 | 20 μA /20 μA |
| Q0, Q1, $\overline{\text{Q0}}$, $\overline{\text{Q1}}$ | Data outputs | 50/33 | 1.0mA/20mA |

NOTE: One (1.0) FAST unit load is defined as: 20 μA in the high state and 0.6mA in the low state.

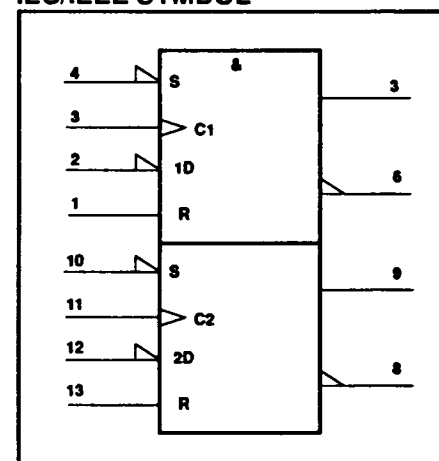
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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SYNCHRONIZING SOLUTIONS

Synchronizing incoming signals to a system clock has proven to be costly, either in terms of time delays or hardware. The reason for this is that in order to synchronize the signals a flip-flop must be used to "capture" the incoming signal. While this is perhaps the only way to synchronize a signal, to this point, there have been problems with this method. Whenever the flop's setup or hold times are violated the flop can enter a metastable state causing the outputs in turn to glitch, oscillate, enter an intermediate state or change state in some abnormal fashion. Any of these conditions could be responsible for causing a system crash. To minimize this risk, flip-flops are often cascaded so that the input signal is captured on the first clock pulse and released on the second clock pulse (see Fig. 1). This gives the first flop about one clock period minus the flop delay and minus the second flop's clock-to-Q setup time to resolve any metastable condition. This method greatly reduces the probability of the outputs of the synchronizing device displaying an abnormal state but the trade-off is that one clock cycle is lost to synchronize the incoming data and two separate flip-flops are required to produce the cascaded flop circuit. In order to assist the designer of

synchronizing circuits Philips Components—Signetics is offering the 74F50728.

The 50728 consists of two pair of cascaded D-type flip-flops with metastable immune features and is pin compatible with the 74F74. Because the flops are cascaded on a single part the metastability characteristics are greatly improved over using two separate flops that are cascaded. The pin compatibility with the 74F74 allows for plug-in retrofitting of previously designed systems.

Because the probability of failure of the 74F50728 is so remote, the metastability characteristics of the part were empirically determined based on the characteristics of its sister part, the 74F5074. The table below shows the 74F5074 metastability characteristics.

Having determined the T_0 and τ of the flop, calculating the mean time between failures (MTBF) for the 74F50728 is simple. It is, however, somewhat different than calculating MTBF for a typical part because data requires two clock pulses to transit from the input to the output. Also, in this case a failure is considered of the output beyond the normal propagation delay.

Suppose a designer wants to use the flop for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), and is using a clock frequency of 50MHz. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/T_0)} f_c f_i$$

In this formula, f_c is the frequency of the clock, f_i is the average input event frequency, and t' is the period of the clock input (20 nanoseconds). In this situation the f_i will be twice the data frequency of 20 MHz because input events consist of both of low and high data transitions. From Fig. 2 it is clear that the MTBF is greater than 10^{41} seconds. Using the above formula the actual MTBF is 2.23×10^{42} seconds or about 7×10^{34} years.

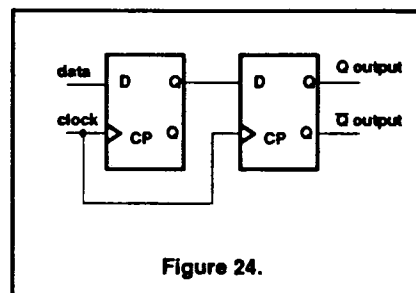


Figure 24.

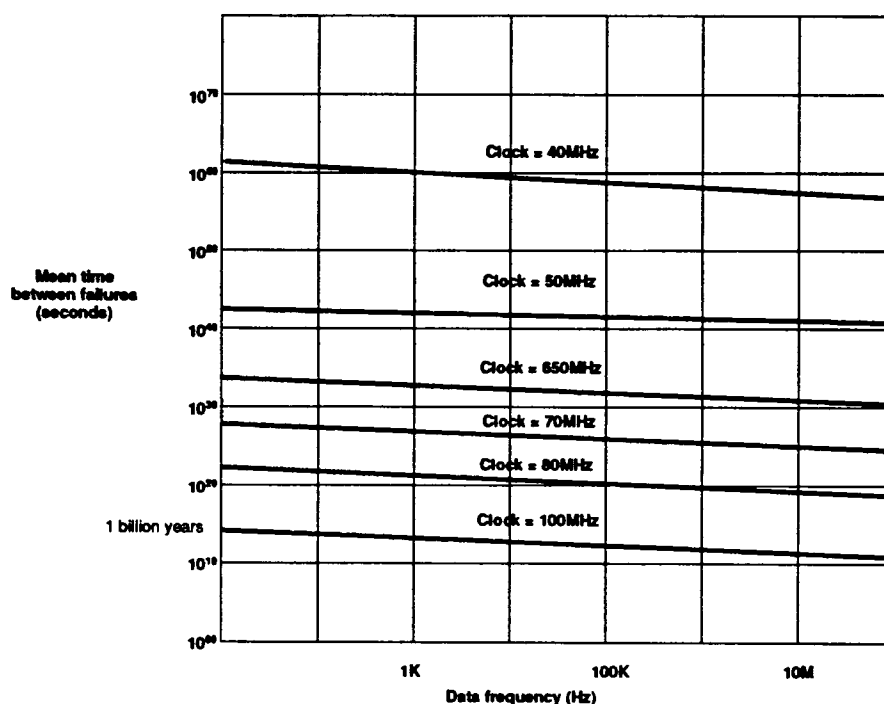
TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC} S AND TEMPERATURES

| | $T_{amb} = 0^\circ C$ | | $T_{amb} = 25^\circ C$ | | $T_{amb} = 70^\circ C$ | |
|-----------------|-----------------------|--------------------------|------------------------|-----------------------|------------------------|-----------------------|
| | τ | T_0 | τ | T_0 | τ | T_0 |
| $V_{CC} = 5.5V$ | 125ps | 1.0×10^9 sec | 138ps | 5.4×10^6 sec | 160ps | 1.7×10^5 sec |
| $V_{CC} = 5.0V$ | 115ps | 1.3×10^{10} sec | 135ps | 9.8×10^6 sec | 167ps | 3.9×10^4 sec |
| $V_{CC} = 4.5V$ | 115ps | 3.4×10^{13} sec | 132ps | 5.1×10^8 sec | 175ps | 7.3×10^4 sec |

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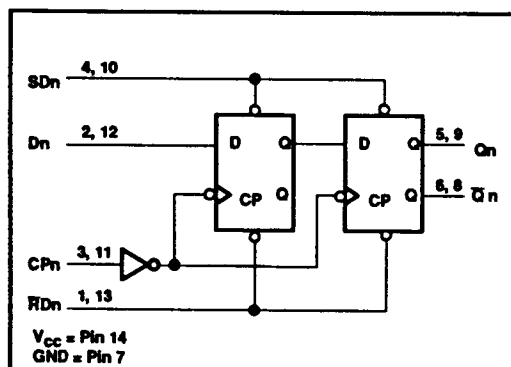
MEAN TIME BETWEEN FAILURES VERSUS DATA FREQUENCY AT VARIOUS CLOCK FREQUENCY



NOTE: $V_{CC} = 5V$, $T_{AMB} = 25^{\circ}C$, $T = 135^{\circ}PS$, $T_O = 9.8 \times 10^8 SEC$

Figure 25.

LOGIC DIAGRAM



NOTE: Data entering the flip-flop requires two clock cycles to arrive at the output.

FUNCTION TABLE

| INPUTS | | | | INTERNAL REGISTER | OUTPUTS | | OPERATING MODE |
|--------|-----|-----|----|-------------------|---------|-------------|--------------------|
| SDn | RDn | CPn | Dn | Q | Qn | \bar{Q}_n | |
| L | H | X | X | H | H | L | Asynchronous set |
| H | L | X | X | L | L | H | Asynchronous reset |
| L | L | X | X | X | H | H | Undetermined* |
| H | H | ↑ | h | h | H | L | Load "1" |
| H | H | ↑ | l | l | L | H | Load "0" |
| H | H | L | X | NC | NC | NC | Hold |

NOTES:

1. H = High voltage level
2. h = High voltage level one setup time prior to low-to-high clock transition
3. L = Low voltage level
4. l = Low voltage level one setup time prior to low-to-high clock transition
5. NC = No change from the previous setup
6. X = Don't care
7. * = This setup is unstable and will change when either set or reset return to the high-level
8. ↑ = Low-to-high clock transition.
9. ** = Data entering the flip-flop requires two clock cycles to arrive at the output (see logic diagram)

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ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

| SYMBOL | PARAMETER | | RATING | UNIT |
|-----------|--|------------------|------------------|------|
| V_{CC} | Supply voltage | | -0.5 to +7.0 | V |
| V_{IN} | Input voltage | | -0.5 to +7.0 | V |
| I_{IN} | Input current | | -30 to +5 | mA |
| V_{OUT} | Voltage applied to output in high output state | | -0.5 to V_{CC} | V |
| I_{OUT} | Current applied to output in low output state | | 40 | mA |
| T_{amb} | Operating free air temperature range | Commercial range | 0 to +70 | °C |
| | | Industrial range | -40 to +85 | °C |
| T_{stg} | Storage temperature range | | -65 to +150 | °C |

RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|-----------|--------------------------------------|------------------|--------|-----|-----|------|
| | | | MIN | NOM | MAX | |
| V_{CC} | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| V_{IH} | High-level input voltage | | 2.4 | | | V |
| V_{IL} | Low-level input voltage | | | | 0.8 | V |
| I_{IK} | Input clamp current | | | | -18 | mA |
| I_{OH} | High-level output current | | | | -3 | mA |
| I_{OL} | Low-level output current | | | | 20 | mA |
| T_{amb} | Operating free air temperature range | Commercial range | 0 | | +70 | °C |
| | | Industrial range | -40 | | +85 | °C |

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

| SYMBOL | PARAMETER | | TEST CONDITIONS ¹ | | | LIMITS | | | UNIT |
|-----------------|---|---------------|--|-----------------------|---------------------|--------|------------------|------|------|
| | | | | | | MIN | TY, ² | MAX | |
| V _{OH} | High-level output voltage | | V _{CC} = MIN, V _{IH} = MIN V _{IL} = MAX, | I _{OH} = MAX | ±10%V _{CC} | 2.5 | | | V |
| | | | | | ±5%V _{CC} | 2.7 | 3.4 | | V |
| V _{OL} | Low-level output voltage | | V _{CC} = MIN, V _{IL} = MAX, V _{IH} = MIN | I _{OL} = MAX | ±10%V _{CC} | | 0.30 | 0.50 | V |
| | | | | | ±5%V _{CC} | | 0.30 | 0.50 | V |
| V _{IK} | Input clamp voltage | | V _{CC} = MIN, I _I = I _{IK} | | | | -0.73 | -1.2 | V |
| I _I | Input current at maximum input voltage | | V _{CC} = MAX, V _I = 7.0V | | | | | 100 | μA |
| I _{IH} | High-level input current | | V _{CC} = MAX, V _I = 2.7V | | | | | 20 | μA |
| I _{IL} | Low-level input current | Dn | V _{CC} = MAX, V _I = 0.5V | | | | | -250 | μA |
| | | CPn, SDn, RDn | | | | | | -20 | μA |
| I _{OS} | Short-circuit output current ³ | | V _{CC} = MAX, V _O = 2.25V | | | -60 | | -150 | mA |
| I _{CC} | Supply current ⁴ (total) | | V _{CC} = MAX | | | | 23 | 34 | mA |

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at $V_{CC} = 5\text{V}$, $T_{amb} = 25^\circ\text{C}$.
- Not more than one output should be shorted at a time. For testing I_{OS} , the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
- Measure I_{CC} with the clock input grounded and all outputs open, then with Q and \bar{Q} outputs high in turn.

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AC ELECTRICAL CHARACTERISTICS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | | | UNIT |
|------------------------|--|-------------------|--|------------|------------|---|------------|---|--------------|----|------|
| | | | $T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | | |
| f_{max} | Maximum clock frequency | Waveform 1 | 100 | 145 | | 85 | | 70 | | ns | |
| t_{PLH} t_{PHL} | Propagation delay CPn to Qn or Qn | Waveform 1 | 2.0 2.0 | 3.8 3.8 | 6.0 6.0 | 1.5 2.0 | 6.5 6.5 | 1.5 2.0 | 7.5 7.0 | ns | |
| t_{PLH} t_{PHL} | Propagation delay SDn RDn to Qn or Qn | Waveform 2 | 3.5 3.5 | 5.0 5.0 | 8.0 8.0 | 3.0 3.0 | 9.0 8.5 | 3.0 3.0 | 10.5 10.0 | ns | |
| $t_{sk(o)}$ | Output skew ^{1, 2} | Waveform 4 | | | 1.5 | | 1.5 | | 1.5 | ns | |

NOTES TO AC ELECTRICAL CHARACTERISTICS

1. $|t_{PLH} \text{ actual} - t_{PHL} \text{ actual}|$ for any one output compare to any other output where N and M are either LH or HL.
2. Skew lines are valid only under same conditions (temperature, V_{CC} , loading, etc.).

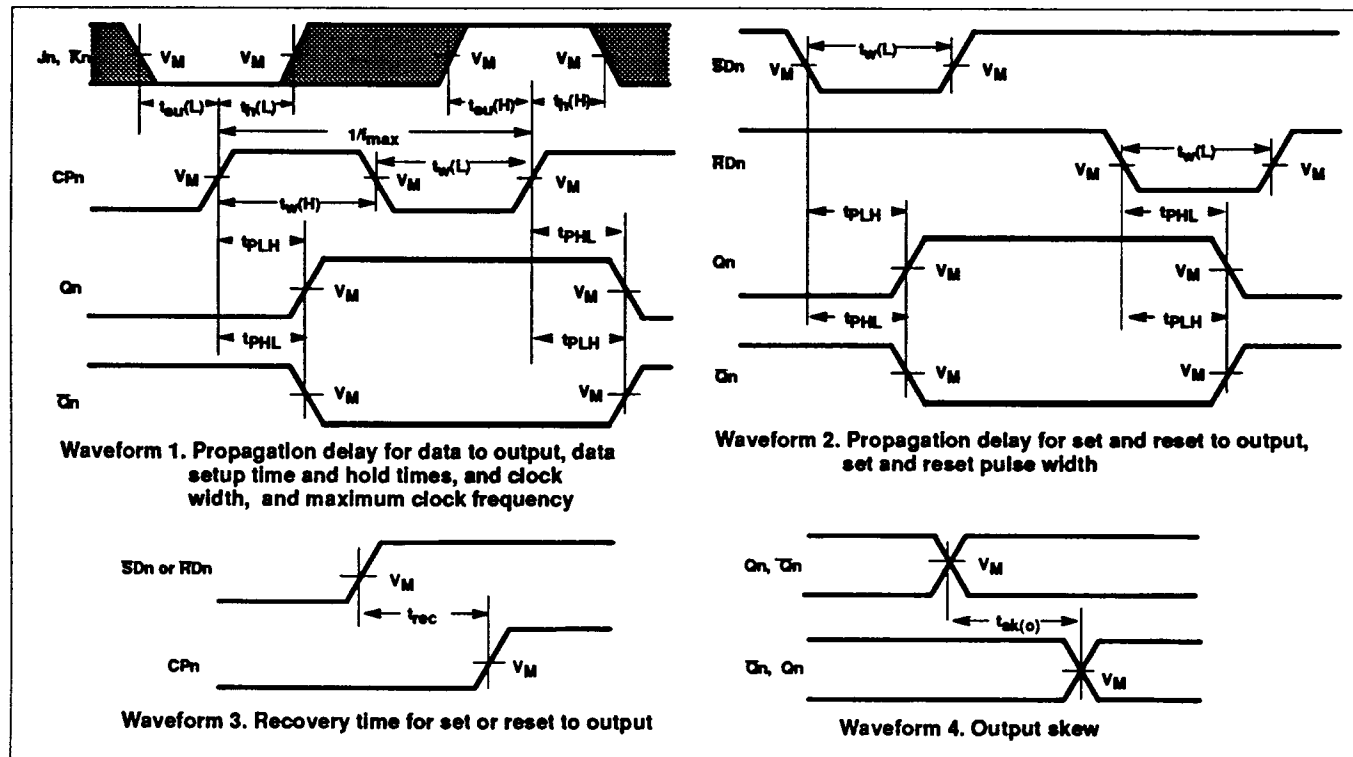
AC SETUP REQUIREMENTS

| SYMBOL | PARAMETER | TEST CONDITION | LIMITS | | | | | | UNIT | |
|--|--------------------------------------|-------------------|--|-----|-----|---|-----|---|------|-----|
| | | | $T_{amb} = +25^{\circ}\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | | $T_{amb} = 0^{\circ}\text{C to } +70^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | $T_{amb} = -40^{\circ}\text{C to } +85^{\circ}\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{pF}$ $R_L = 500\Omega$ | | |
| | | | MIN | TYP | MAX | MIN | MAX | MIN | | MAX |
| $t_{su}(\text{H})$ $t_{su}(\text{L})$ | Setup time, high or low Dn to CPn | Waveform 1 | 1.5 1.5 | | | 2.0 2.0 | | 2.0 2.0 | | ns |
| $t_h(\text{H})$ $t_h(\text{L})$ | Hold time, high or low Dn to CPn | Waveform 1 | 0.0 0.0 | | | 1.5 1.5 | | 1.5 1.5 | | ns |
| $t_w(\text{H})$ $t_w(\text{L})$ | CPn pulse width, high or low | Waveform 2 | 3.0 4.0 | | | 3.5 5.0 | | 4.0 5.5 | | ns |
| $t_w(\text{L})$ | SDn, RDn pulse width, low | Waveform 2 | 4.5 | | | 4.0 | | 4.5 | | ns |
| t_{rec} | Recovery time SDn, RDn to CPn | Waveform 3 | 3.5 | | | 3.5 | | 3.5 | | ns |

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AC WAVEFORMS



NOTES:

- For all waveforms, $V_M = 1.5V$.
- The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS

