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# IA-D1 TURBOSENSOR™

T-41-55

## IA-D1 Series Area Image Sensor Arrays

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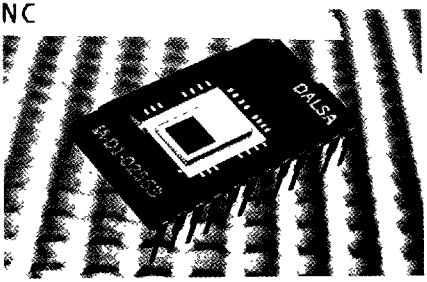
### FEATURES

- **Up to 10,000 frames / second**
- **32x32, 64x64, 128x128, 256x256 Elements**
- **16 MHz Output Data Rate**
- **TURBOSENSOR™ technology**
- **16μm (H) x 16μm (V) Pixel Size**
- **3,000:1 Dynamic Range**
- **2 Phase BCCDs for Simple Operation**




### DESCRIPTION

The IA-D1 series of area array image sensors use DALSA's TURBOSENSOR™ technology to provide high output data rates of 16 MHz. The series is ideally suited for applications requiring maximum operating speed and medium resolution, and employs two phase buried channel CCD shift registers to maximize output speed and reduce noise. The IA-D1 sensors use square pixels and a square imaging area in sizes of 32x32, 64x64, 128x128, and 256x256. The dynamic range of the photoelements exceeds 3,000:1 and provides an output which is linear for all light levels.

All sensors in the IA-D1 series are functionally equivalent and can be easily interchanged in systems with only a few minor adjustments.

### APPLICATIONS

The IA-D1 series sensors are ideally suited for applications requiring maximum operating speed, medium resolution and high sensitivity.

DALSA also offers the CA-D1 camera series which uses the IA-D1 series of image sensors for:

- **image processing**
- **machine vision**
- **surveillance**

For mechanical information regarding package size and tolerance, refer to package #50-01-24002 in **Optical and Mechanical Considerations of Sensors** on pp. 101-104 of this databook.

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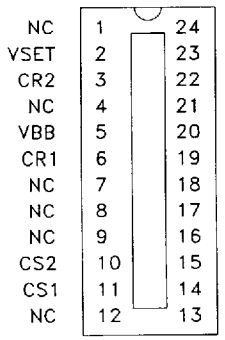
## IA-D1 PIN FUNCTIONAL DESCRIPTION

| PIN | SYMBOL | NAME |
|---|---|---|
| 1,4,7,8,9 | NC | No Connection |
| 2 | VSET | Output Node Set Voltage |
| 3 | CR2 | Readout Clock, Phase 2 |
| 5 | VBB | Substrate Bias Voltage |
| 6 | CR1 | Readout Clock, Phase 1 |
| 10 | CS2 | Storage Region Clock, Phase 2 |
| 11 | CS1 | Storage Region Clock, Phase 1 |
| 12,16,21 | NC | No connection |
| 13 | VSS | Ground Reference |
| 14 | CI1 | Image Region Clock, Phase 1 |
| 15 | CI2 | Image Region Clock, Phase 2 |
| 17 | TOP | Not Used; Do not connect |
| 18 | TCK | Storage to Readout Transfer Clk |
| 19 | RST | Output Node Reset Clock |
| 20 | VOD | Output Node Drain Bias |
| 22 | VDD | Amplifier Supply Voltage |
| 23 | OS | Output Signal |
| 24 | VSS | Ground Reference |




**NOTE:** Pinout shown here applies to Rev. C and Rev. D pinouts only.





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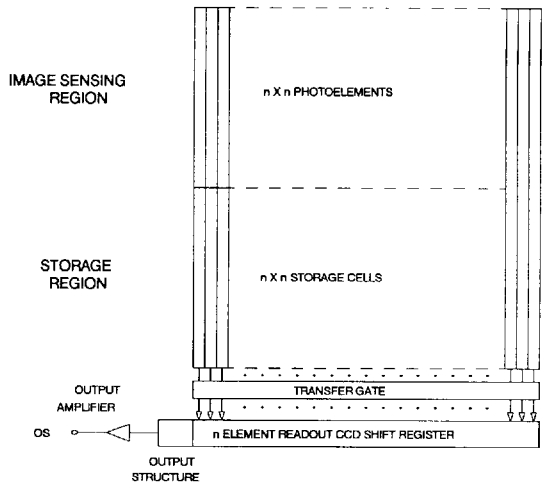
## IA-D1 IMAGE SENSOR BLOCK DIAGRAM

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## FUNCTIONAL DESCRIPTION

*ORGANIZATION*

This series of area array image sensors employ a frame transfer organization with photogate photoelements. During exposure, signal is collected under phase 1 of the imaging region CCD. At the end of the exposure time, the entire frame is transferred at high speed into the storage region CCD. During this time invalid data is transferred out of the readout CCD. Exposure then starts for the next frame; during this time the data from the storage region is transferred line by line to the readout shift register and then to the output.

*PHOTOELEMENTS*

The area array consists of a square matrix of 32, 64, 128 or 256 photoelements for imaging, plus an additional square matrix of the same size for frame storage. Each pixel has a photosensitive area of 256 square micrometers and center to center spacing of 16 micrometers in both directions.

The photoelements (in the imaging region) are controlled by the image region clocks CI1 and CI2 and are organized to allow parallel transfer into the storage region, which is controlled by CS1 and CS2. Specifically, CI1 transfers into CS2.

The TURBOSENSOR™ photogate photoelement offers ultra high speed operation and responds linearly with respect to input light intensity.

*TRANSFER GATE*

This gate controls the flow of light generated signal charge from the storage region CCD (CS1 and CS2) into the readout CCD shift register (CR1 and CR2). Specifically, TCK interfaces between CS1 of the storage region and CR1 of the readout shift register.

Electrons from the storage region are transferred when a high potential (equal to the high clock voltage) is applied to the transfer gate.

*OUTPUT STRUCTURE*

The signal charge packets from the readout shift register are transferred serially, over the SET gate, to a floating sensing diffusion. As the signal charge is received, the corresponding potential on the diffusion is applied to the input of a two stage low noise amplifier structure, producing an output signal voltage (OS). The floating sensing diffusion is cleared of signal charge by the reset gate, driven by the reset clock (RST) in preparation for the subsequent signal charge packet.

The output data stream includes invalid data which is transferred out during the high speed transfer from imaging to storage region.

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## RECOMMENDED DC OPERATION

*SIGNAL NAMES*

The signal names assigned to the package pins describe both the function of the pin as well as the sense of input signals. DC (unclocked) bias and supply voltages are designated with signal names beginning with "V". Clocked signals begin with any other letter and are representative of the function of the pin.

*SUPPLY VOLTAGES*

VDD provides operating current to the on chip output amplifier and hence should be well regulated. The substrate, or bulk bias voltage, VBB, is negative with respect to ground in some applications. This low current bias should be well regulated. Since protection diodes are provided between many clock lines and the substrate, no clocks can be permitted to go below VBB. In most cases, VBB can be maintained at 0 volts (equal to VSS), although a negative VBB can reduce charge injection.

*OUTPUT BIAS*

A very low current DC gate bias, VSET, controls transfer of signal charge onto the output sensing diffusion. This voltage should be adjusted with a resistive divider to optimize output structure operation. If VSET is not optimized, single bright pixels will appear to "bleed" into adjacent pixels and could be mistaken for very poor CTE or crosstalk.

The shift register output drain voltage, VOD, is a bias provided to the output structure to discharge signal electrons after sensing. It should be well filtered to reduce output noise.

*GROUND REFERENCE*

VSS is provided as the ground reference for the output amplifier. All other bias, supply and clock voltages are specified relative to VSS.

*OUTPUT SIGNAL*

The output signal is an AC waveform on a DC offset. It is recommended that the video signal be buffered for current gain. It is also recommended that the video signal be AC coupled.

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### IA-D1 DC OPERATING CONDITIONS

**Recommended Operating Conditions at Tp = 25°C. (See notes)**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| VDD | Amplifier supply voltage | 12.0 | 15.0 | 16.0 | V |
| VBB | Substrate voltage | -3.0 | 0.0 | 0.0 | V |
| VOD | Shift register drain voltage | 10.0 | 13.0 | 16.0 | V |
| VSET | Set Voltage | 3.0 | 5.0 | 8.0 | V |

**NOTES:**

1. Voltages with respect to ground (VSS).
2. Tp is defined as the package temperature.

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## RECOMMENDED CLOCK OPERATION

*PHOTOELEMENTS (IMAGE CLOCKS)*

The two phase image clocks are the photosensitive elements in this device. These clocks, CI1 and CI2, control exposure and transfer signal charge from the image region to the storage region.

Signal charge electrons are photogenerated during the exposure period, which is set by the time CI1 is maintained high and CI2 is maintained low.

Following exposure, CI1 and CI2 are clocked at high speed (approximately 1/4 the readout frequency of CR1 and CR2) to move the signal charge in parallel into the storage region. Charge transfers from CI1 into CS2. During this time CI1 and CI2 can be operated at 50% duty cycle and are complementary.

*STORAGE CLOCKS*

During integration or exposure, the storage clocks (CS1 and CS2) transfer signal data from the storage region, through the transfer gate (controlled by TCK), to the readout shift register. CS1 transfers over TCK into CR1. During this time CS2 is the same as TCK, and CS1 is the inverse of CS2.

High speed transfer follows integration. During this time CS1 is driven by the same signal as CI1 and CS2 is driven by the same signal as CI1. Invalid data is transferred from the storage region into the readout shift register and to the output at this time.

*TRANSFER CLOCK*

The transfer gate is controlled by the TCK signal. When TCK is pulsed high the pixel data is transferred into the first phase (CR1) of the CCD readout shift register.

During integration, TCK pulses occur once per line, and transfer each line of the previous frame into the readout shift register.

During high speed transfer, TCK and CS2 should be driven by the same signal in order to transfer invalid data out of the storage region.

*READOUT CLOCKS*

Two phase transport clocks (CR1, CR2) are used to transfer data to the output structure. The clocks can be operated at 50% duly cycle continuously and are complementary, non-overlapping.

*OUTPUT CONTROL CLOCKS*

One output structure clock (RST) is required to clear the output node after sensing. This clock should go to a high voltage equal to the transport clock (CR) high voltages, and to a low of VSS. During RST high, the output will go to a reset level as shown in the clock diagrams.

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## IA-D1 CLOCK CHARACTERISTICS

**Recommended Operating Conditions at Tp = 25°C.**

| SYMBOL | DESCRIPTION | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{H(C)}$ | Transport clock 1 HIGH | 4.0 | 7.0 | 16.0 | V |
| $V_{L(C)}$ | Transport clock 1 LOW | 0.0 | 0.0 | 0.5 | V |
| $V_{H(TCK)}$ | Transfer clock HIGH | 4.0 | 7.0 | 16.0 | V |
| $V_{L(TCK)}$ | Transfer clock LOW | 0.0 | 0.0 | 0.5 | V |
| $V_{H(RST)}$ | Reset clock HIGH | 4.0 | 8.0 | 16.0 | V |
| $V_{L(RST)}$ | Reset clock LOW | 0.0 | 0.0 | 0.5 | V |
| $f_{(RST)}$ | Reset frequency | | 15 | 20 | MHz |
| $f_{(DATA)}$ | Data freq. (effective data rate) | | 15 | 20 | MHz |

**NOTE:**

1. Transport clocks include CI1, CI2, CS1, CS2, CR1, and CR2.



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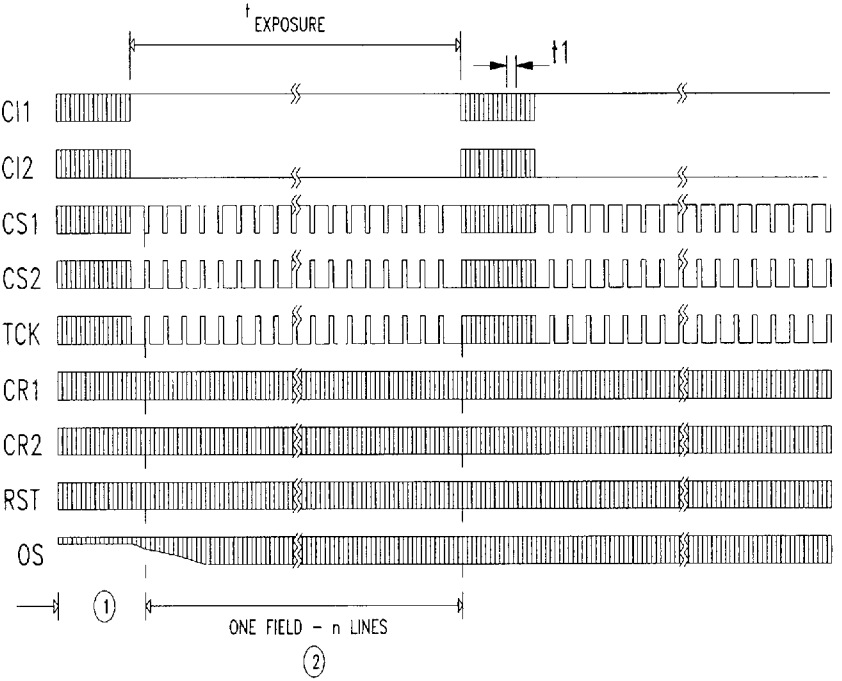
## IA-D1 DEVICE CLOCKING




11: $f_{CI,CS} \leq 5$ MHz

1. High speed transfer from the imaging area to the storage area. The number of CI pulses is equal to the number of rows in the array.

2 Readout of entire storage region. The number of CS pulses is equal to the number of rows in the array. For each CS pulse, a string of CR pulses greater than the number of columns in the array must occur.



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# IA-D1
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## IA-D1 TIMING

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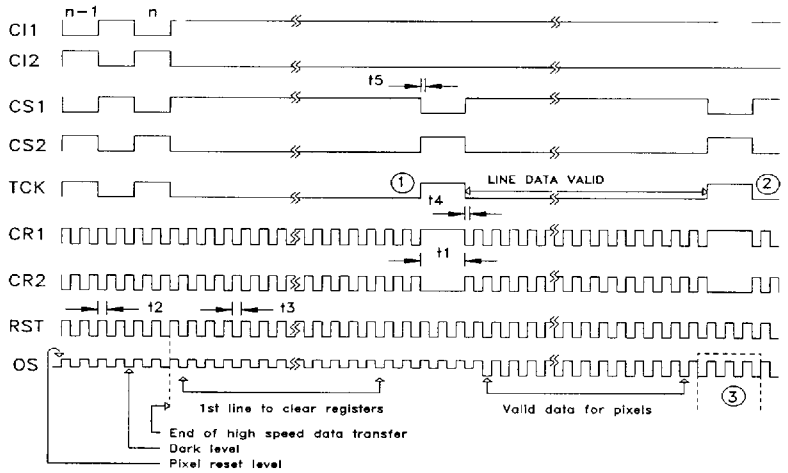


1. Transfer of last line into O/P CCD shift register
2. Transfer of second to last line into O/P CCD S.R. pixel. Data for each line is read out to the output during the line data valid time.
3. Not valid data

t1: TCK, CR1 high and CS1 low ≥ 100 ns
t2: RST high ≥ 15 ns
t3: RST falling edge ≥ 0 ns before CR1 Falling edge
t4: TCK falling edge ≥ 20 ns before CR1 falling edge.
t5: TCK rising edge ≥ 100 ns after CS1 falling edge

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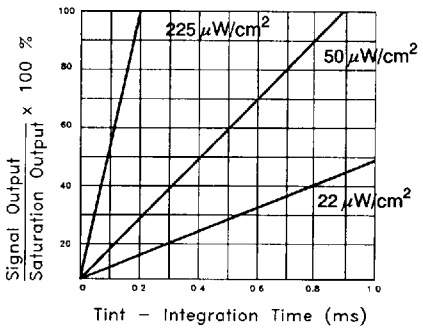
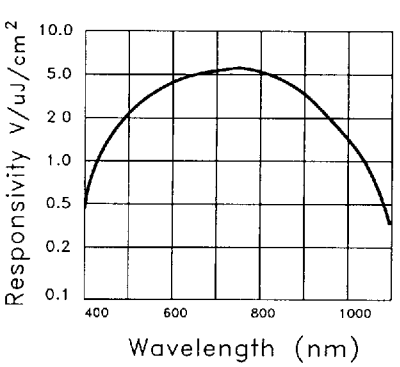
## IA-D1 PERFORMANCE MEASUREMENTS




**Output vs. Integration Time**




**Spectral Response**





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## IA-D1 PERFORMANCE CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| **Recommended Operating Conditions at Tp = 25°C. (See notes).** | | | | |
| Dynamic range[1] | | 3,000:1 | | |
| Noise Equivalent Exposure (NEE) | | 15 | | pJ/cm$^2$ |
| Saturation Equivalent Exposure (SEE)[2] | | 45 | | nJ/cm$^2$ |
| Responsivity[2] | | 6.6 | | V/$\mu$J/cm$^2$ |
| Saturation Output Amplitude ($V_{SAT}$)[3] | | 300 | | mV |
| $V_{NOISE}$[4] | | | | |
| Peak-Peak | | 0.50 | | mV |
| RMS | | 0.10 | | mV |
| FPN | | 10.0 | | mV |
| PRNU[5] | | 10 | | % $V_{SAT}$ |
| CTE[6] | 0.9999 | 0.99999 | 0.999999 | |
| DC Output Offset | | 8 | | V |
| Storage Temperature ($T_P$)[7] | −70 | | +125 | °C |
| Operating Temperature ($T_P$)[7] | −60 | | +90 | °C |

**Notes:**
1. Ratio of $V_{SAT}$ to RMS Noise with reset noise eliminated through correlated double sampling (CDS)
2. Responsivity at peak Quantum Efficiency (near 700 nm).
3. Output amplitude with respect to dark reference level.
4. Amplifier noise measured with reset noise eliminated through correlated double sampling (CDS).
5. PRNU is measured at approximately 50% $V_{SAT}$ and is the difference between the pixels with the lowest and highest outputs, expressed as a percentage of $V_{SAT}$.
6. CTE is the measurement for a one stage transfer, measured at $f_{RST}$ = 3.75 MHz
7. $T_P$ is package temperature
8. See cosmetic specifications for this device.

**Test Conditions:**
1. All tests are done at $f_{RST}$ = 3.75 MHz
2. Light Source QTH lamp with WBHM, unless otherwise noted
3. VDD, VOD = 15 V, VBB = 0 V; Clock high voltage 12 V, low voltage 0 V, (includes CRx, Clx, CSx, TCK, RST as applicable); VSET as required for maximum $V_{SAT}$ and CTE
4. All measurements exclude first and last 2 rows and columns of frame

## IA-D1 ELECTRICAL CHARACTERISTICS

| PARAMETER | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|
| **Recommended Operating Conditions at Tp = 25°C.** | | | | |
| Output impedance | | 200 | | Ω |
| Amplifier supply current | | 15 | | mA |
| DC Bias Currents (VOD, VSET, VBB) | | | 1 | mA |
| Amplifier power dissipation | 150 | 225 | 300 | mW |
| Resistance to VBB | | | | |
| Transport gate (CRx) | | 5 | | MΩ |
| Transfer gate | | 5 | | MΩ |
| Reset, Set gate | | 5 | | MΩ |
| Capacitance to VBB | | | | |
| Transport clocks (CRx)[1] | | 75 | | pF |
| Transfer clocks (TCK)[1] | | 8 | | pF |
| Imaging and Storage clocks (CSx, Clx) | | 500 | | pF |
| Reset (RST), Set (VSET) gate | | 12 | | pF |

**Notes:**
1 Capacitance given for 128x128 element array For other sensors in this series, apply the following factors: 32 element (0.3), 64 element (0.6), 256 element (1.8).

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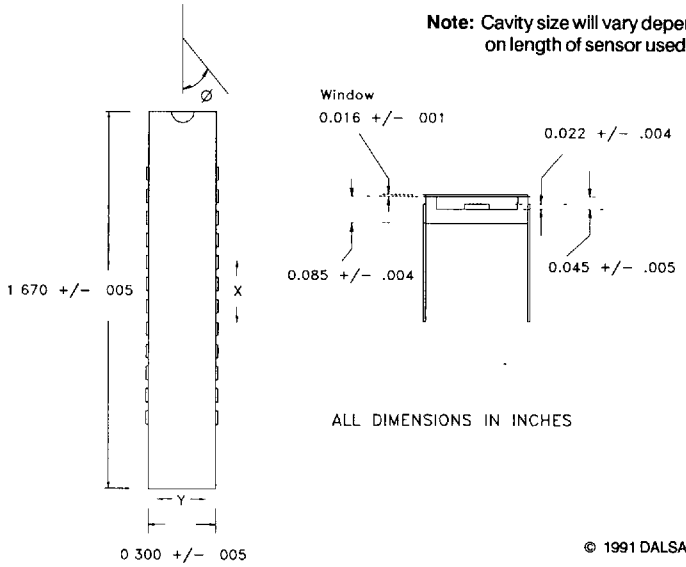
# Optical and Mechanical Considerations of Sensors

## Optical and Mechanical Considerations of DALSA CCD Image Sensors

DALSA INC T-90-20

This applications note provides packaging information for the sensors listed in this databook. Please refer to the tables on the following pages for the critical dimensions of each image sensor series. For more information on a particular image sensor, please refer to the specific datasheet.

### FIGURE 1. DIMENSIONS OF PACKAGE # 50-01-24005






### TABLE 1. PACKAGE # 50-01-24005 TYPICAL DIMENSIONS

| Package # | Part | X | Y | Ø |
|---|---|---|---|---|
| 50-01-24005 | IL-C3-0128 | 0.55 ± .09 | 0.15 ± .02 | $0^{o} \pm 3.0^{o}$ |
| 50-01-24005 | IL-C3-0256 | 0.55 ± .08 | 0.15 ± .02 | $0^{o} \pm 2.5^{o}$ |
| 50-01-24005 | IL-C3-0512 | 0.55 ± .07 | 0.15 ± .02 | $0^{o} \pm 2.0^{o}$ |
| 50-01-24005 | IL-C2-0512 | 0.55 ± .07 | 0.15 ± .02 | $0^{o} \pm 2.0^{o}$ |
| 50-01-24005 | IL-C9-0512 | 0.55 ± .07 | 0.15 ± .02 | $0^{o} \pm 2.0^{o}$ |
| 50-01-24005 | IL-C4-1024 | 0.55 ± .05 | 0.15 ± .02 | $0^{o} \pm 1.5^{o}$ |
| 50-01-24005 | IL-C4-2048 | 0.55 ± .04 | 0.15 ± .02 | $0^{o} \pm 1.0^{o}$ |
| 50-01-24005 | IL-C5-2048 | 0.55 ± .05 | 0.15 ± .02 | $0^{o} \pm 1.5^{o}$ |
| 50-01-24005 | IL-C5-4096 | 0.55 ± .04 | 0.15 ± .02 | $0^{o} \pm 1.0^{o}$ |
| 50-01-24005 | IL-C6-2048 | 0.55 ± .04 | 0.15 ± .02 | $0^{o} \pm 1.0^{o}$ |
| 50-01-24005 | IL-E1-0512 | 0.55 ± .07 | 0.15 ± .02 | $0^{o} \pm 2.0^{o}$ |
| 50-01-24005 | IL-E1-1024 | 0.55 ± .05 | 0.15 ± .02 | $0^{o} \pm 1.5^{o}$ |
| 50-01-24005 | IL-E1-2048 | 0.55 ± .04 | 0.15 ± .02 | $0^{o} \pm 1.0^{o}$ |
| 50-01-24005 | IL-F2-0512 | 0.55 ± .07 | 0.15 ± .02 | $0^{o} \pm 2.0^{o}$ |
| 50-01-24005 | IL-F2-1024 | 0.55 ± .05 | 0.15 ± .02 | $0^{o} \pm 1.5^{o}$ |
| 50-01-24005 | IL-F2-2048 | 0.55 ± .04 | 0 15 ± .02 | $0^{o} \pm 1.0^{o}$ |

**Note:** X = center imaging area to center pin 1 along package Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

# Optical and Mechanical Considerations of Sensors

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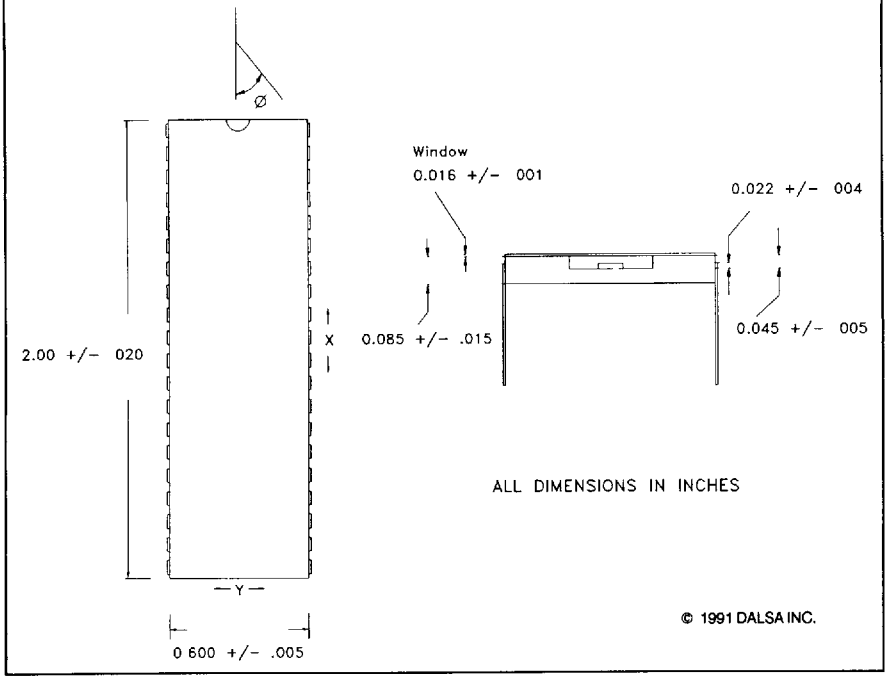
## FIGURE 2. DIMENSIONS OF PACKAGE # 50-01-40003




## TABLE 2. PACKAGE # 50-01-40003 TYPICAL DIMENSIONS

| Package # | Part | X | Y | Ø |
|---|---|---|---|---|
| 50-01-40003 | IT-C5-2048 | 0.95 ± 0.1 | 0.3 ± 0.05 | $0^{o} \pm 2.5^{o}$ |
| 50-01-40003 | IT-C5-4096 | 0.95 ± 0.08 | 0.3 ± 0.03 | $0^{o} \pm 1.5^{o}$ |
| 50-01-40003 | IT-E1-1536 | 0.95 ± 0.08 | 0.3 ± 0 05 | $0^{o} \pm 2.0^{o}$ |
| 50-01-40003 | IT-E1-2048 | 0.95 ± 0.06 | 0.3 ± 0.05 | $0^{o} \pm 1.5^{o}$ |
| 50-01-40003 | IT-F2-2048 | 0.95 ± 0.06 | 0.3 ± 0.03 | $0^{o} \pm 1.5^{o}$ |

**Note:** X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package
Ø = off-axis rotation.

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# Optical and Mechanical Considerations of Sensors

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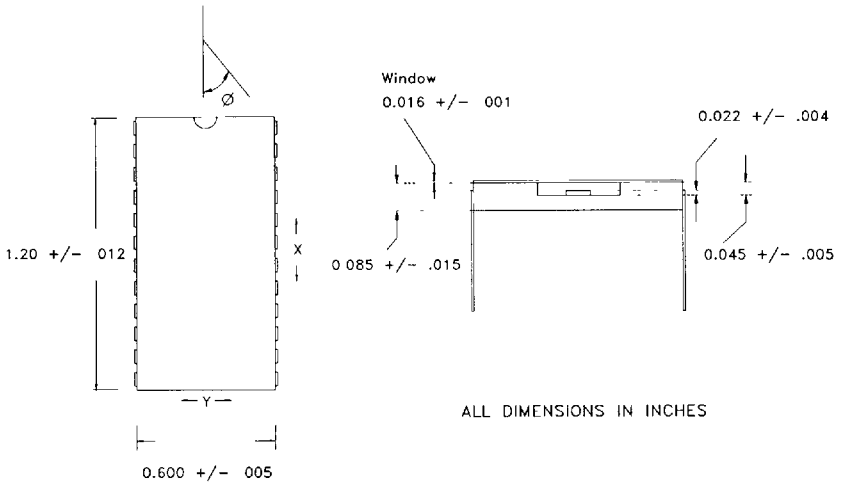
## FIGURE 3. DIMENSIONS OF PACKAGE # 50-01-24002






## TABLE 3. PACKAGE # 50-01-40002 TYPICAL DIMENSIONS

| Package # | Part | X | Y | Ø |
|---|---|---|---|---|
| 50-01-40002 | IA-D1-0032 | 0.56 ± 0.12 | 0.3 ± 0.05 | $0^{o} \pm 5.0^{o}$ |
| 50-01-40002 | IA-D1-0064 | 0.57 ± 0.09 | 0.3 ± 0.04 | $0^{o} \pm 4.0^{o}$ |
| 50-01-40002 | IA-D1-0128 | 0.59 ± 0.12 | 0.3 ± 0.03 | $0^{o} \pm 2.5^{o}$ |
| 50-01-40002 | IA-D1-0256 | 0.71 ± 0.10 | 0.3 ± 0.03 | $0^{o} \pm 1.5^{o}$ |

**Note:** X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation

# Optical and Mechanical Considerations of Sensors



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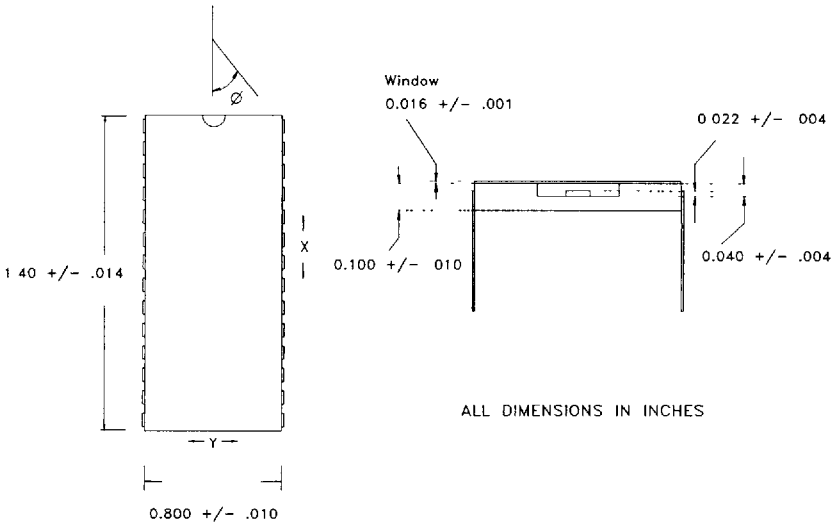
## FIGURE 4. DIMENSIONS OF PACKAGE # 50-01-28004






## TABLE 4. PACKAGE # 50-01-28004 TYPICAL DIMENSIONS

| Package # | Part | X | Y | Ø |
|---|---|---|---|---|
| 50-01-28004 | IA-D2-0512 | 0.65 ± 0.08 | 0.4 ± 0.04 | $0^{o} \pm 3.0^{o}$ |

**Note:** X = center imaging area to center pin 1 along package. Y = center imaging area to center pin 1 across package.
Ø = off-axis rotation



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