



IBM0116165 IBM0116165M
IBM0116165B IBM0116165P

1M x 16 12/8 EDO DRAM

Features

- 1,048,576 word by 16 bit organization
- Single 3.3V $\pm$ 0.3V or 5.0V $\pm$ 0.5V power supply
- Standard Power (SP) and Low Power (LP)
- 4096 Refresh Cycles
 - 64 ms Refresh Rate (SP version)
 - 256 ms Refresh Rate (LP version)
- High Performance:
- Low Power Dissipation
 - Active (max) - 85 mA / 75 mA / 65 mA
 - Standby: TTL Inputs (max) - 1.0 mA
 - Standby: CMOS Inputs (max)
 - 1.0 mA (SP version)
 - 0.2 mA (LP version)
 - Self Refresh (LP version only)
 - 200 μ A (3.3 Volt)
 - 300 μ A (5.0 Volt)

		-50	-60	-6R	-70	Units
t _{RAC}	RAS Access Time	50	60	60	70	ns
t _{CAC}	CAS Access Time	13	15	17	20	ns
t _{AA}	Column Address Access Time	25	30	30	35	ns
t _{RC}	Cycle Time	84	104	104	124	ns
t _{HPC}	EDO (Hyper Page) Mode Cycle Time	20	25	25	30	ns

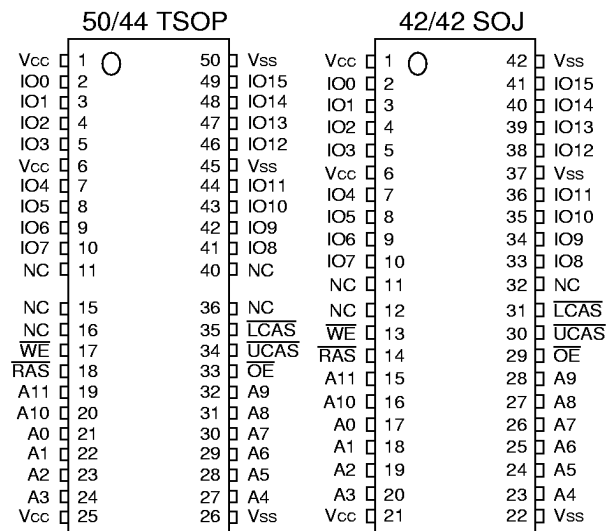
- Extended Data Out (Hyper Page) Mode
- Dual $\overline{\text{CAS}}$ Byte Read/Write
- Read-Modify-Write
- $\overline{\text{RAS}}$ Only and $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
- Hidden Refresh
- Package: TSOP-II 50/44 (400milx825mil)
SOJ 42/42 (400mil)

Description

The IBM0116165 is a dynamic RAM organized 1,048,576 words by 16 bits, which has a very low "sleep mode" power consumption option. These devices are fabricated in IBM's advanced 0.5 μ m CMOS silicon gate process technology. The circuit and process have been carefully designed to pro-

vide high performance, low power dissipation, and high reliability. The devices operate with a single 3.3V $\pm$ 0.3V or 5.0V $\pm$ 0.5V power supply. The 20 addresses required to access any bit of data are multiplexed (12 are strobed with $\overline{\text{RAS}}$, 8 are strobed with $\overline{\text{CAS}}$).

Pin Assignments (Top View)



Pin Description

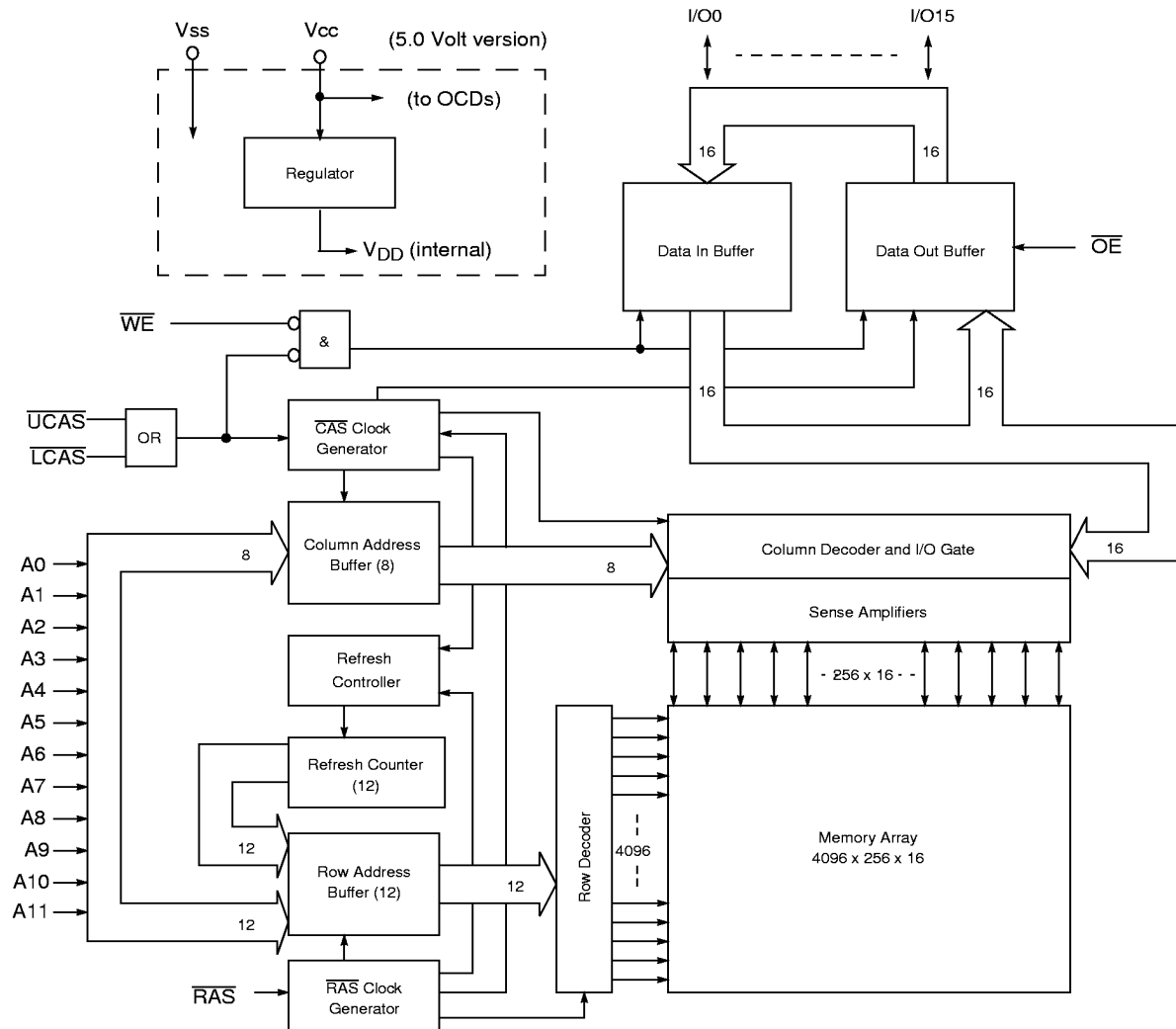
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{LCAS}} / \overline{\text{UCAS}}$	L/U Column Address Strobe
$\overline{\text{WE}}$	Read/Write Input
A0 - A11	Address Inputs
$\overline{\text{OE}}$	Output Enable
I/O0 - I/O15	Data Input/Output
V _{CC}	Power (+3.3V or +5.0V)
V _{SS}	Ground

Ordering Information

Part Number	SP / LP	Self Refresh	Power Supply	Speed	Package	Notes
IBM0116165T3 -50	SP	No	5.0V	50ns	400mil TSOP-II 50/44	1
IBM0116165T3 -60	SP	No	5.0V	60ns	400mil TSOP-II 50/44	1
IBM0116165T3 -70	SP	No	5.0V	70ns	400mil TSOP-II 50/44	1
IBM0116165BT3 -50	SP	No	3.3V	50ns	400mil TSOP-II 50/44	1
IBM0116165BT3 -60	SP	No	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0116165BT3 -6R	SP	No	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0116165BT3 -70	SP	No	3.3V	70ns	400mil TSOP-II 50/44	1
IBM0116165J3 -50	SP	No	5.0V	50ns	400mil SOJ 42/42	1
IBM0116165J3 -60	SP	No	5.0V	60ns	400mil SOJ 42/42	1
IBM0116165J3 -70	SP	No	5.0V	70ns	400mil SOJ 42/42	1
IBM0116165BJ3 -50	SP	No	3.3V	50ns	400mil SOJ 42/42	1
IBM0116165BJ3 -60	SP	No	3.3V	60ns	400mil SOJ 42/42	1
IBM0116165BJ3 -70	SP	No	3.3V	70ns	400mil SOJ 42/42	1
IBM0116165MT --50	LP	Yes	5.0V	50ns	400mil TSOP-II 50/44	1
IBM0116165MT3 -60	LP	Yes	5.0V	60ns	400mil TSOP-II 50/44	1
IBM0116165MT3 -70	LP	Yes	5.0V	70ns	400mil TSOP-II 50/44	1
IBM0116165PT3 -50	LP	Yes	3.3V	50ns	400mil TSOP-II 50/44	1
IBM0116165PT3 -60	LP	Yes	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0116165PT3 -6R	LP	Yes	3.3V	60ns	400mil TSOP-II 50/44	1
IBM0116165PT3 -70	LP	Yes	3.3V	70ns	400mil TSOP-II 50/44	1
IBM0116165MJ3 -50	LP	Yes	5.0V	50ns	400mil SOJ 42/42	1
IBM0116165MJ3 -60	LP	Yes	5.0V	60ns	400mil SOJ 42/42	1
IBM0116165MJ3 -70	LP	Yes	5.0V	70ns	400mil SOJ 42/42	1
IBM0116165PJ3 -50	LP	Yes	3.3V	50ns	400mil SOJ 42/42	1
IBM0116165PJ3 -60	LP	Yes	3.3V	60ns	400mil SOJ 42/42	1
IBM0116165PJ3 -70	LP	Yes	3.3V	70ns	400mil SOJ 42/42	1

1. SP = Standard Power version (IBM0116165 and IBM0116165B); LP = Low Power version (IBM0116165M and IBM00116165P)

Block Diagram



Truth Table

Function		$\overline{\text{RAS}}$	$\overline{\text{LCAS}}$	$\overline{\text{UCAS}}$	$\overline{\text{WE}}$	$\overline{\text{OE}}$	Row Address	Column Address	I/O0 - I/O15
Standby		H	H→X	H→X	X	X	X	X	High Impedance
Read: Word		L	L	L	H	L	Row	Col	Data Out
Read: Lower Byte		L	L	H	H	L	Row	Col	Lower Byte: Data Out Upper Byte: High-Z
Read: Upper Byte		L	H	L	H	L	Row	Col	Lower Byte: High-Z Upper Byte: Data Out
Write: Word Early-Write		L	L	L	L	X	Row	Col	Data In
Write: Lower Byte Early-Write		L	L	H	L	X	Row	Col	Lower Byte: Data In Upper Byte: High-Z
Write: Upper Byte Early-Write		L	H	L	L	X	Row	Col	Lower Byte: High-Z Upper Byte: Data In
Read-Modify-Write		L	L	L	H→L	L→H	Row	Col	Data Out, Data In
EDO (Hyper Page) Mode Read	1st Cycle	L	H→L	H→L	H	L	Row	Col	Data Out
	2nd Cycle	L	H→L	H→L	H	L	N/A	Col	Data Out
EDO (Hyper Page) Mode Write	1st Cycle	L	H→L	H→L	L	X	Row	Col	Data In
	2nd Cycle	L	H→L	H→L	L	X	N/A	Col	Data In
EDO (Hyper Page) Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	H→L	L→H	Row	Col	Data Out, Data In
	2nd Cycle	L	H→L	H→L	H→L	L→H	N/A	Col	Data Out, Data In
$\overline{\text{RAS}}$ -Only Refresh		L	H	H	X	X	Row	N/A	High Impedance
CAS-Before-RAS Refresh		H→L	L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	L	H	X	Row	Col	Data In
Self Refresh (LP version only)		H→L	L	L	H	X	X	X	High Impedance

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt Device	5.0 Volt Device		
V_{CC}	Power Supply Voltage	-0.5 to +4.6	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min ($V_{CC}+0.5$, 4.6)	-0.5 to min ($V_{CC}+0.5$, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min ($V_{CC}+0.5$, 4.6)	-0.5 to min ($V_{CC}+0.5$, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

Symbol	Parameter	3.3 Volt Device			5.0 Volt Device			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	$V_{CC} + 0.5$	2.4	—	$V_{CC} + 0.5$	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS} .
2. V_{IH} may overshoot to $V_{CC} + 1.2\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ with 3.3 Volt, or $V_{CC} + 2.0\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ (or $V_{CC} + 1.0\text{V}$ for $\leq 8.0\text{ns}$) with 5.0 Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths $\leq 4.0\text{ns}$ with 3.3 Volt, or to -2.0V for pulse widths $\leq 4.0\text{ns}$ (or -1.0V for $\leq 8.0\text{ns}$) with 5.0 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance ($T_A = 25^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$)	—	7	pF	1
C_O	Output Capacitance (I/O0 - I/O15)	—	7	pF	1

1. Input capacitance measurements made with rise time shift method with $\overline{\text{CAS}}$ & $\overline{\text{RAS}} = V_{IH}$ to disable output.

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3V ± 0.3V or V_{CC} = 5.0V ± 0.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
I _{CC1}	Operating Current Average Power Supply Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: t _{RC} = t _{RC} min.)	-50	—	85	mA 1, 2, 3
		-60 / -6R	—	75	
		-70	—	65	
I _{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V _{IH})	—	2	mA	
I _{CC3}	$\overline{\text{RAS}}$ Only Refresh Current Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}}$ = V _{IH} ; t _{RC} = t _{RC} min)	-50	—	85	mA 1, 3
		-60 / -6R	—	75	
		-70	—	65	
I _{CC4}	EDO (Hyper Page) Mode Current Average Power Supply Current ($\overline{\text{RAS}}$ = V _{IL} , $\overline{\text{CAS}}$, Address Cycling: t _{PC} = t _{PC} min)	-50	—	75	mA 1, 2, 3
		-60 / -6R	—	65	
		-70	—	55	
I _{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{\text{RAS}}$ = $\overline{\text{CAS}}$ = V _{CC} - 0.2V)	SP version	—	1	mA
		LP version	—	0.2	
I _{CC6}	$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Cycling: t _{RC} = t _{RC} min)	-50	—	85	mA 1, 3
		-60 / -6R	—	75	
		-70	—	65	
I _{CC7}	Self Refresh Current, LP version only Average Power Supply Current during Self Refresh CBR cycle with $\overline{\text{RAS}} \geq t_{\text{RASS}}$ (min); $\overline{\text{CAS}}$ held low; WE = V _{CC} - 0.2V; Addresses and D _{IN} = V _{CC} - 0.2V or 0.2V.	3.3V	—	200	μA
		5.0V	—	300	
I _{I(L)}	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V _{IN} ≤ (V _{CC} + 0.3V)), All Other Pins Not Under Test = 0V	-10	+10	μA	
I _{O(L)}	Output Leakage Current (D _{OUT} is disabled, 0.0 ≤ V _{OUT} ≤ V _{CC})	-10	+10	μA	
V _{OH}	Output Level (TTL) Output "H" Level Voltage (I _{OUT} = -2.0mA for 3.3V, or I _{OUT} = -5mA for 5.0V)	2.4	V _{CC}	V	
V _{OL}	Output Level (TTL) Output "L" Level Voltage (I _{OUT} = +2.0mA for 3.3V, or I _{OUT} = +4.2mA for 5.0V)	0.0	0.4	V	
1. I _{CC1} , I _{CC3} , I _{CC4} and I _{CC6} depend on cycle rate. 2. I _{CC1} and I _{CC4} depend on output loading. Specified values are obtained with the output open. 3. Address can be changed once or less while $\overline{\text{RAS}}$ = V _{IL} . In the case of I _{CC4} , it can be changed once or less when $\overline{\text{CAS}}$ = V _{IH} .					

AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$)

1. An initial pause of $200\mu\text{s}$ is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
2. AC measurements assume $t_T = 2\text{ns}$.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Valid column addresses A0 through A7.
5. When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same Read/Write cycle.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	89	—	104	—	104	—	124	—	ns	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	35	—	40	—	40	—	50	—	ns	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time	8	—	10	—	10	—	10	—	ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	50	10K	60	10K	60	10K	70	10K	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	8	10K	10	10K	10	10K	12	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	8	—	10	—	10	—	10	—	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	14	37	14	45	14	43	14	50	ns	1
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	12	25	12	30	12	30	12	35	ns	2
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	8	—	10	—	10	—	12	—	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	45	—	50	—	50	—	55	—	ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	5	—	5	—	ns	
t_{OED}	$\overline{\text{OE}}$ to D_{IN} Delay Time	13	—	15	—	15	—	15	—	ns	3
t_{DZO}	$\overline{\text{OE}}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	4
t_{DZC}	$\overline{\text{CAS}}$ Delay Time from D_{IN}	0	—	0	—	0	—	0	—	ns	4
t_T	Transition Time (Rise and Fall)	2	30	2	30	2	30	2	30	ns	5

1. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
2. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
3. Either t_{CDD} or t_{OED} must be satisfied.
4. Either t_{DZC} or t_{DZO} must be satisfied.
5. AC measurements assume $t_T = 2\text{ns}$.

Write Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	7	—	10	—	12	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	12	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	7	—	10	—	12	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	7	—	10	—	12	—	ns	
t_{DS}	D_{IN} Setup Time	0	—	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	7	—	10	—	12	—	ns	2

1. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
2. These parameters are referenced to $\overline{LCAS}$ or $\overline{UCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

Read Cycle

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	—	60	—	70	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	—	17	—	20	ns	1, 3
t_{AA}	Access Time from Address	—	25	—	30	—	30	—	35	ns	2, 3
t_{OEA}	Access Time from $\overline{OE}$	—	13	—	15	—	17	—	20	ns	3
t_{RCS}	Read Command Setup Time	0	—	0	—	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	0	—	0	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	0	—	0	—	ns	3
t_{OFF}	Output Buffer Turn-Off Delay	—	13	—	15	—	15	—	15	ns	5, 6
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	15	—	15	—	ns	7
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	—	13	—	15	—	15	—	15	ns	5
t_{OES}	$\overline{OE}$ Setup Time Prior to $\overline{CAS}$	5	—	5	—	5	—	5	—	ns	
t_{ORD}	$\overline{OE}$ Setup Time Prior to $\overline{RAS}$ (Hidden Refresh)	0	—	0	—	0	—	0	—	ns	

1. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
2. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
3. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. t_{OFF} is referenced from the rising edge of $\overline{RAS}$ or $\overline{CAS}$, which ever is last.
7. Either t_{CDD} or t_{OED} must be satisfied.

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		-6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	115	—	135	—	135	—	162	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	67	—	79	—	79	—	94	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	30	—	34	—	36	—	44	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	42	—	49	—	49	—	59	—	ns	1
t_{OEh}	$\overline{OE}$ Command Hold Time	7	—	10	—	10	—	12	—	ns	

1. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Extended Data Out (Hyper Page) Mode Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{HCAS}	EDO (Hyper Page) Mode $\overline{CAS}$ Pulse Width	8	10K	10	10K	12	10K	ns	
t_{HPC}	EDO (Hyper Page) Mode Cycle Time (Read/Write)	20	—	25	—	30	—	ns	
t_{HPRWC}	EDO (Hyper Page) Mode Read Modify Write Cycle Time	51	—	60	—	72	—	ns	
t_{DOH}	Data-out Hold Time from $\overline{CAS}$	5	—	5	—	5	—	ns	
t_{WHZ}	Output buffer Turn-Off Delay from $\overline{WE}$	0	10	0	10	0	15	ns	
t_{WPZ}	$\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High	7	—	10	—	10	—	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	30	—	35	—	40	ns	1
t_{RASP}	EDO (Hyper Page) Mode $\overline{RAS}$ Pulse Width	50	125K	60	125K	70	125K	ns	
t_{OEP}	$\overline{OE}$ High Pulse Width	10	—	10	—	10	—	ns	
t_{OEHC}	$\overline{OE}$ High Hold Time from $\overline{CAS}$ High	10	—	10	—	10	—	ns	

1. Measured with the specified current load and 100pF at $V_{OL} = 0.8V$ and $V_{OH} = 2.0V$.



Refresh Cycle

Symbol	Parameter	-50		-60 / -6R		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CSR}	CAS Setup Time (CAS before RAS Refresh Cycle)	5	—	5	—	5	—	ns	
t_{CHR}	CAS Hold Time (CAS before RAS Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRP}	WE Setup Time (CAS before RAS Refresh Cycle)	10	—	10	—	10	—	ns	
t_{WRH}	WE Hold Time (CAS before RAS Cycle)	10	—	10	—	10	—	ns	
t_{RPC}	RAS Precharge to CAS Hold Time	5	—	5	—	5	—	ns	

Self Refresh Cycle - Low Power version only

Symbol	Parameter	-50		-60		-70		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RASS}	RAS Pulse Width During Self Refresh Cycle	100	—	100	—	100	—	μ s	1
t_{RPS}	RAS Precharge Time During Self Refresh Cycle	89	—	104	—	124	—	ns	1
t_{CHS}	CAS Hold Time From RAS Rising During Self Refresh Cycle	-50	—	-50	—	-50	—	ns	1, 2
t_{CHD}	CAS Hold Time From RAS Falling During Self Refresh Cycle	350	—	350	—	350	—	μ s	1, 2

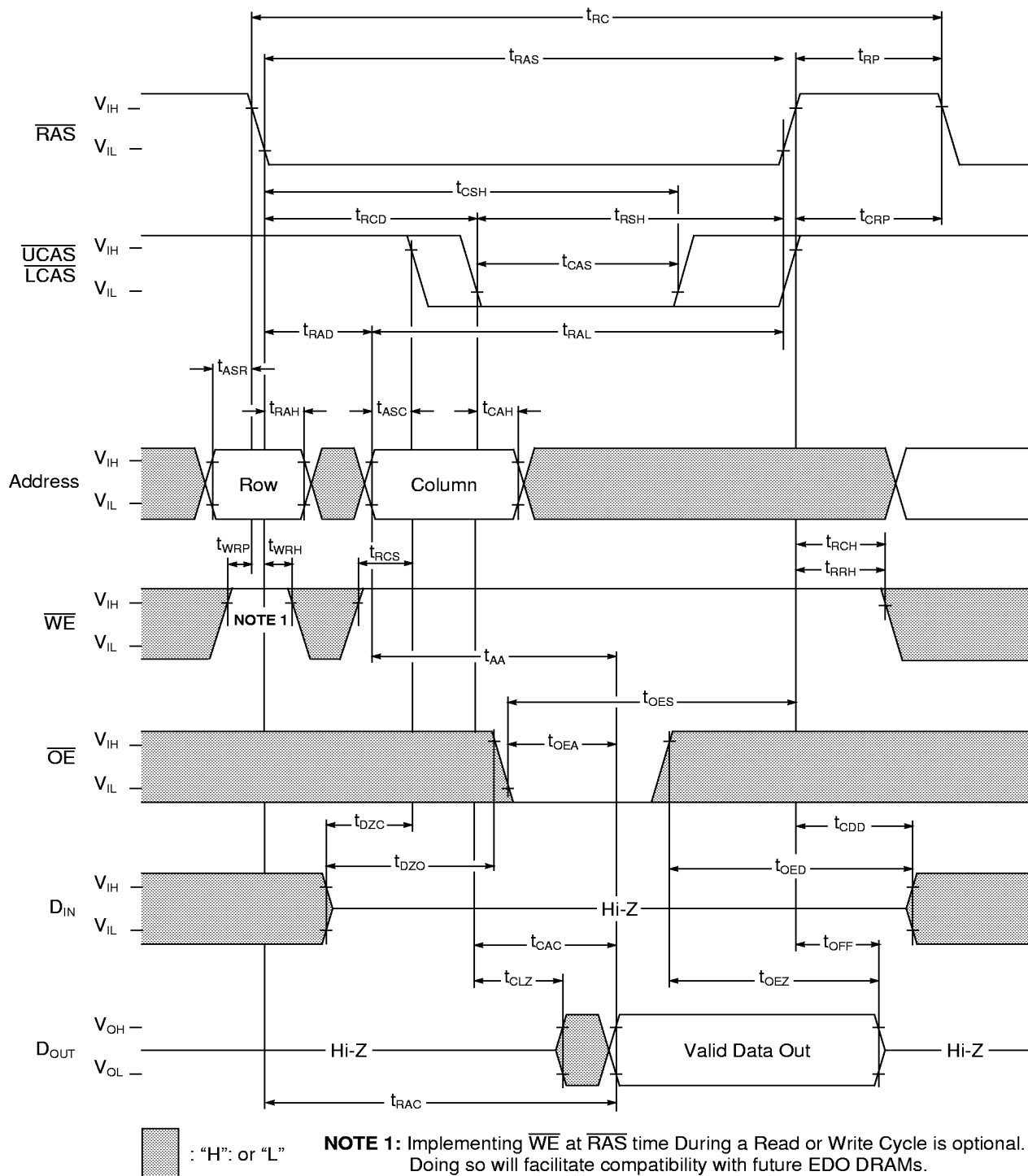
1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation:
If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh.
If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.
2. If $t_{RASS} > t_{CHD}$ (min) then t_{CHD} applies. If $t_{RASS} \leq t_{CHD}$ (min) then t_{CHS} applies.

Refresh

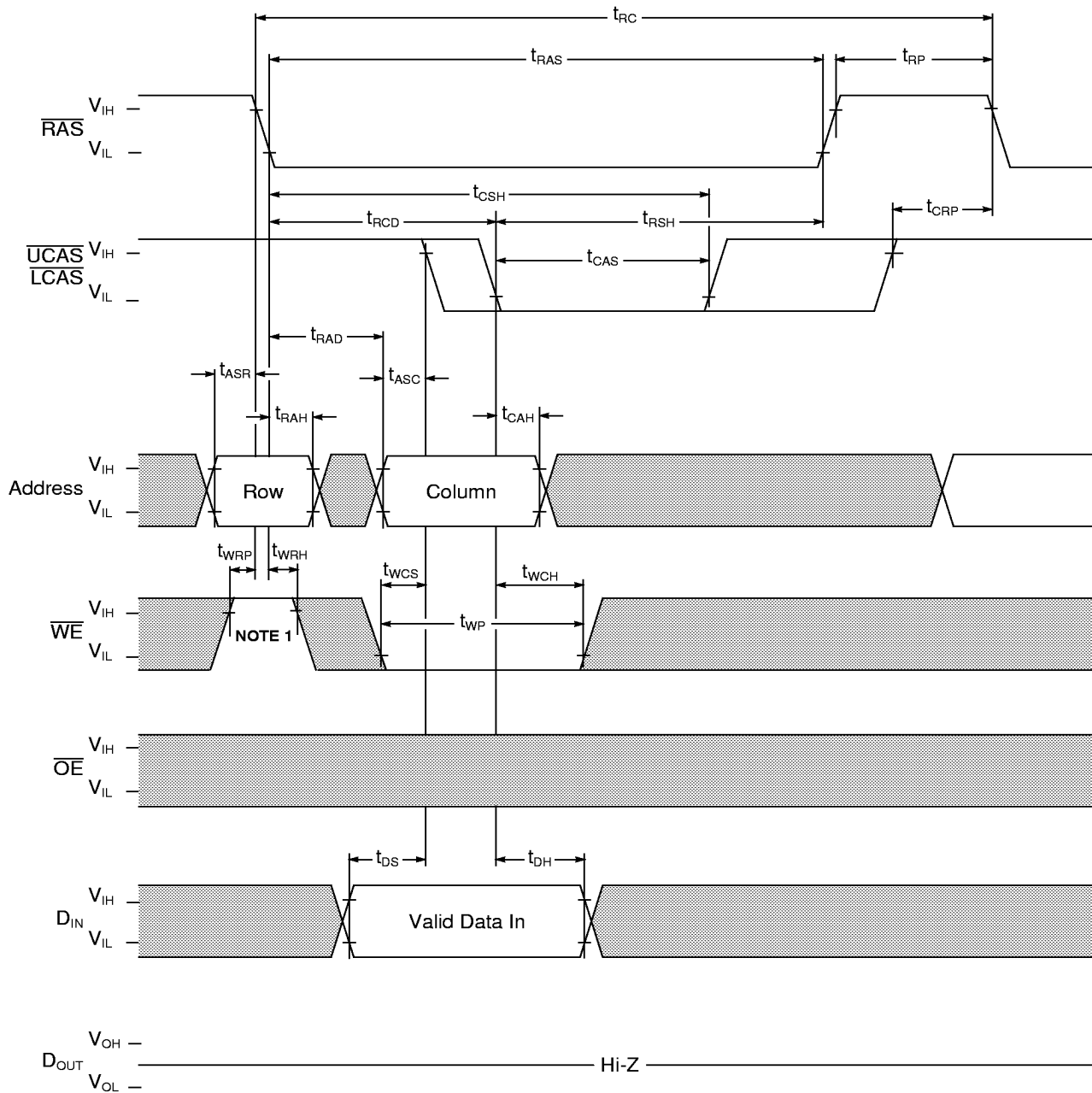
SYMBOL	Parameter		-50		-60 / -6R		-70		Units	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{REF}	Refresh Period	SP version	—	64	—	64	—	64	ms	1
		LP version	—	256	—	256	—	256		

1. 4096 cycles.

Read Cycle



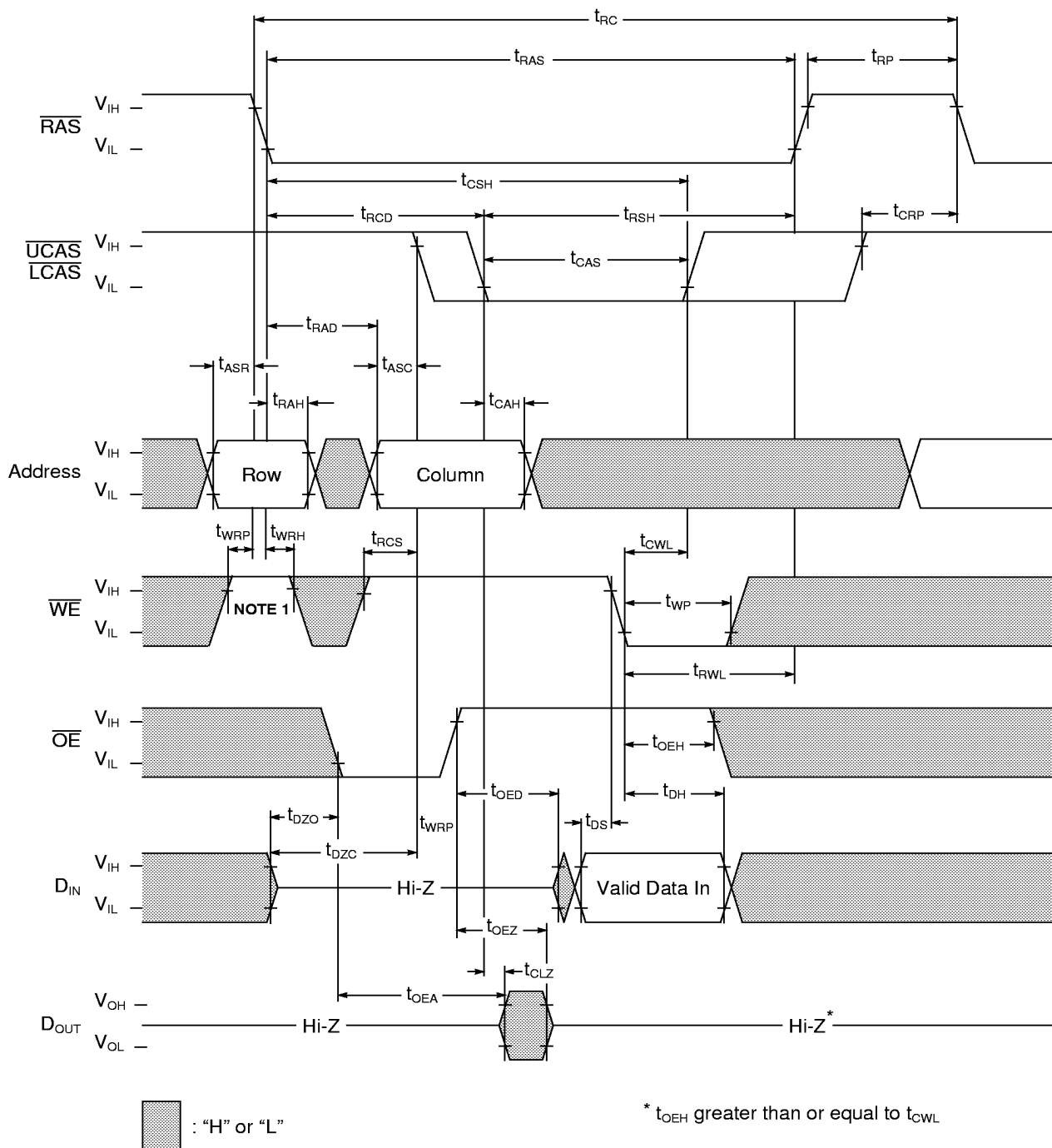
Write Cycle (Early Write)



: "H" or "L"

NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

Write Cycle (Delayed Write)



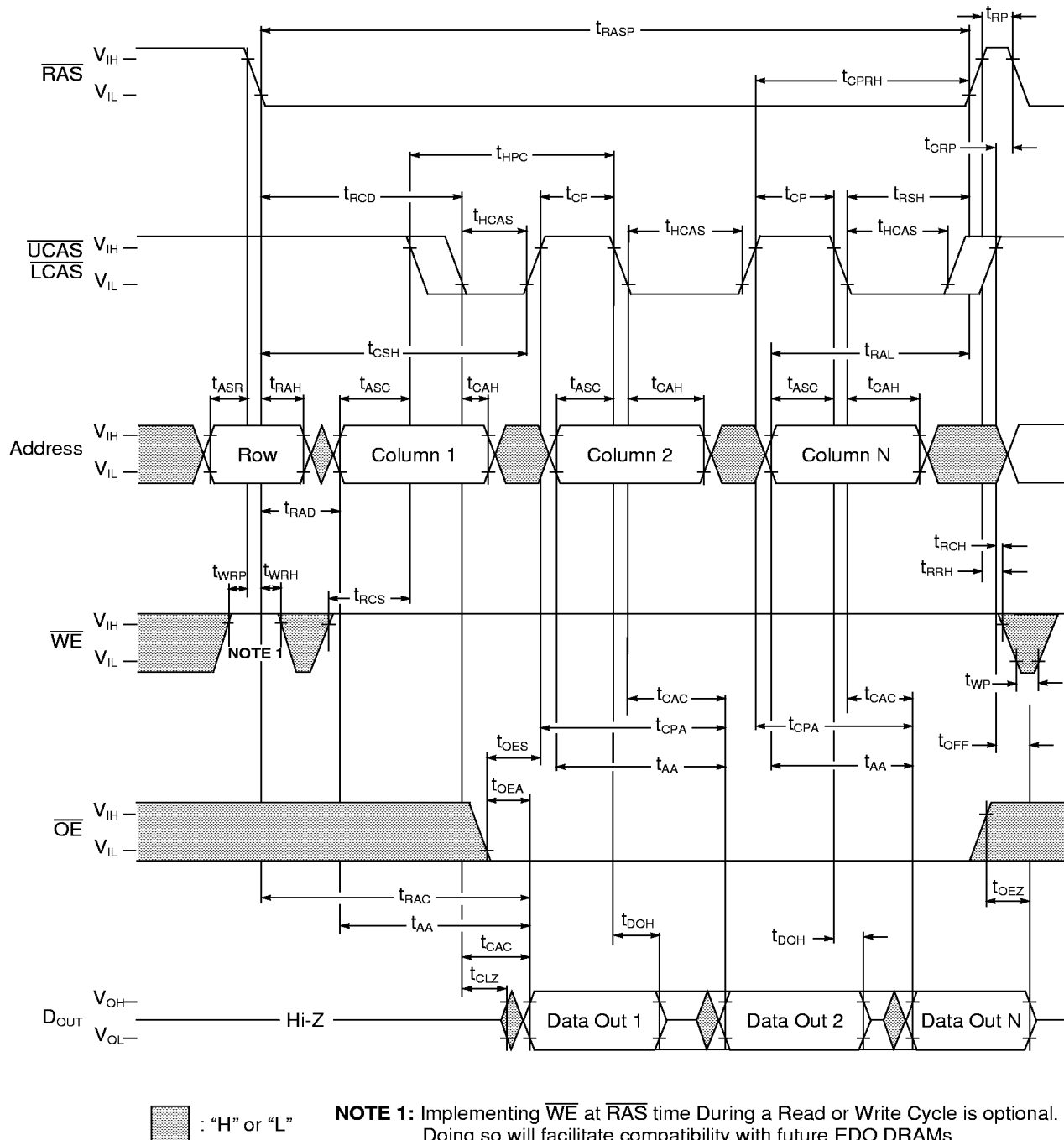
NOTE 1: Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

The diagram illustrates the timing relationships for various DRAM control and data signals. The signals shown are $\overline{\text{RAS}}$, $\overline{\text{UCAS/LCAS}}$, Address, $\overline{\text{WE}}$, $\overline{\text{OE}}$, D_{IN} , and D_{OUT} . The timing parameters are defined as follows:

- t_{RWC} : Row Write Cycle time
- t_{RAS} : Row Access time
- t_{RP} : Row Period time
- t_{RCD} : Row to Column Delay time
- t_{CSH} : Column Strobe High time
- t_{RSH} : Row Strobe High time
- t_{CRP} : Column Refresh time
- t_{RAD} : Row Address Delay time
- t_{ASC} : Address Strobe to Column time
- t_{CAH} : Column Address High time
- t_{ASR} : Address Strobe to Row time
- t_{RAH} : Row Address High time
- t_{CWD} : Column Write Delay time
- t_{AWD} : Address Write Delay time
- t_{RWL} : Row Write Latency time
- t_{WRP} : Write Refresh Period time
- t_{WRH} : Write Refresh High time
- t_{RWD} : Row Write Delay time
- t_{CWL} : Column Write Latency time
- t_{WP} : Write Pulse time
- t_{AA} : Address to Array time
- t_{RCS} : Row to Column Strobe time
- t_{OE} : Output Enable time
- t_{OEHA} : Output Enable High to Array time
- t_{OEHL} : Output Enable Low to Array time
- t_{DZC} : Data to Z time
- t_{DZO} : Data to Output time
- t_{CAC} : Column Access time
- t_{CLZ} : Column Latency time
- t_{OED} : Output Enable Delay time
- t_{OEZ} : Output Enable to Z time
- t_{DS} : Data Strobe time
- t_{DH} : Data Hold time
- t_{RAC} : Row Access time

NOTE 1: Implementing $\overline{\text{WE}}$ at $\overline{\text{RAS}}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

EDO (Hyper Page) Mode Read Cycle

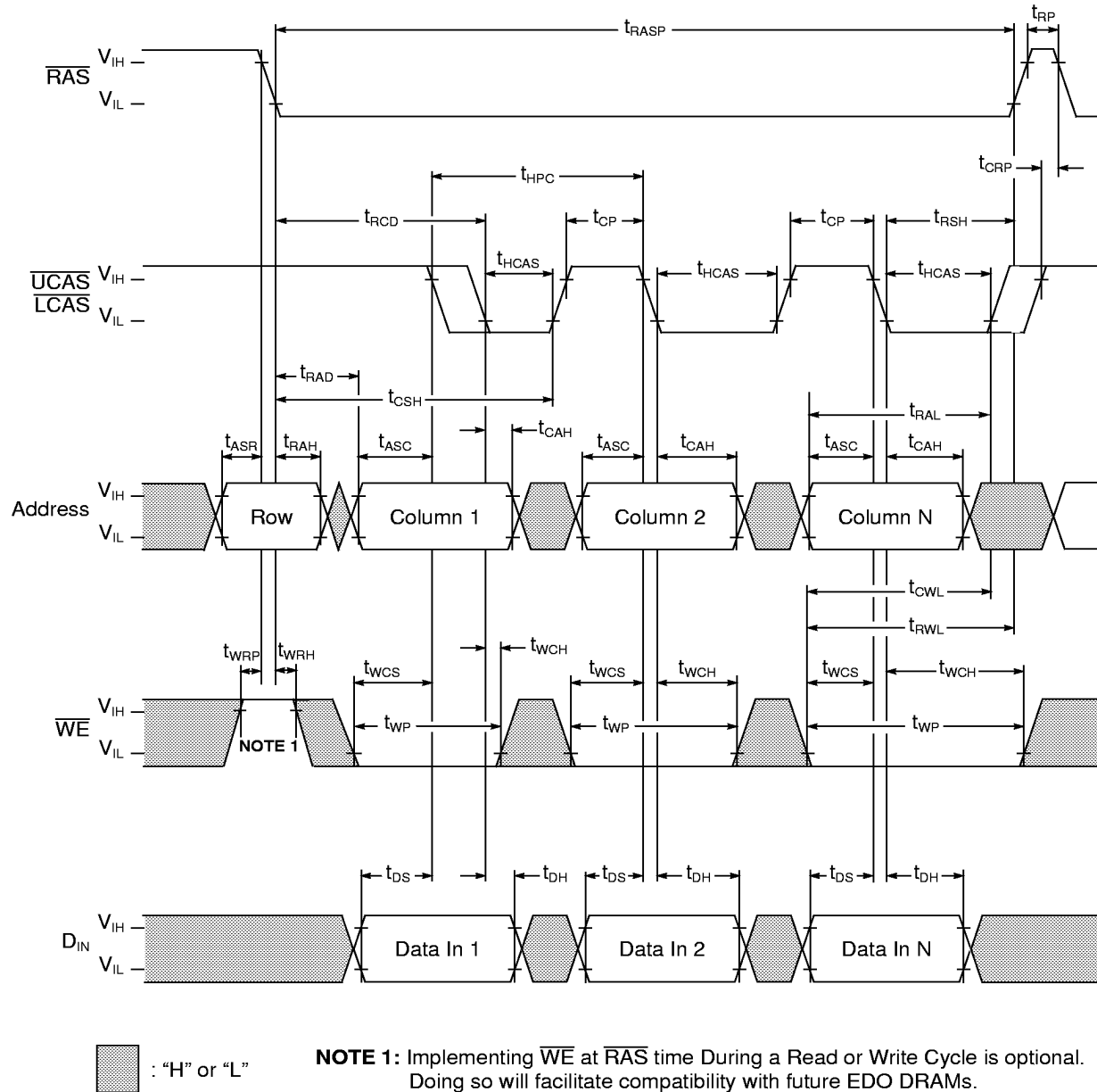


[illegible]

[illegible]

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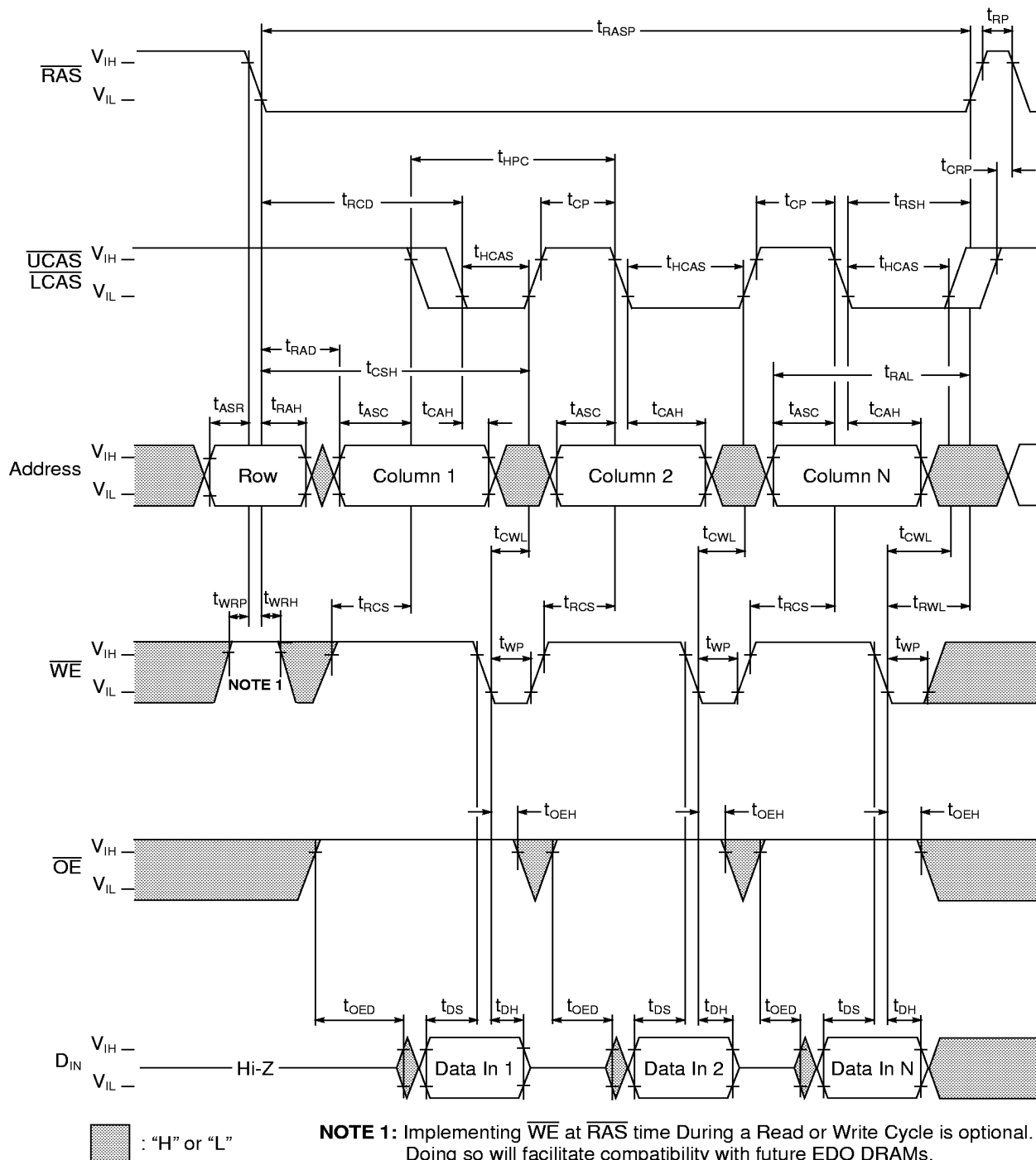
EDO (Hyper Page) Mode Early Write Cycle



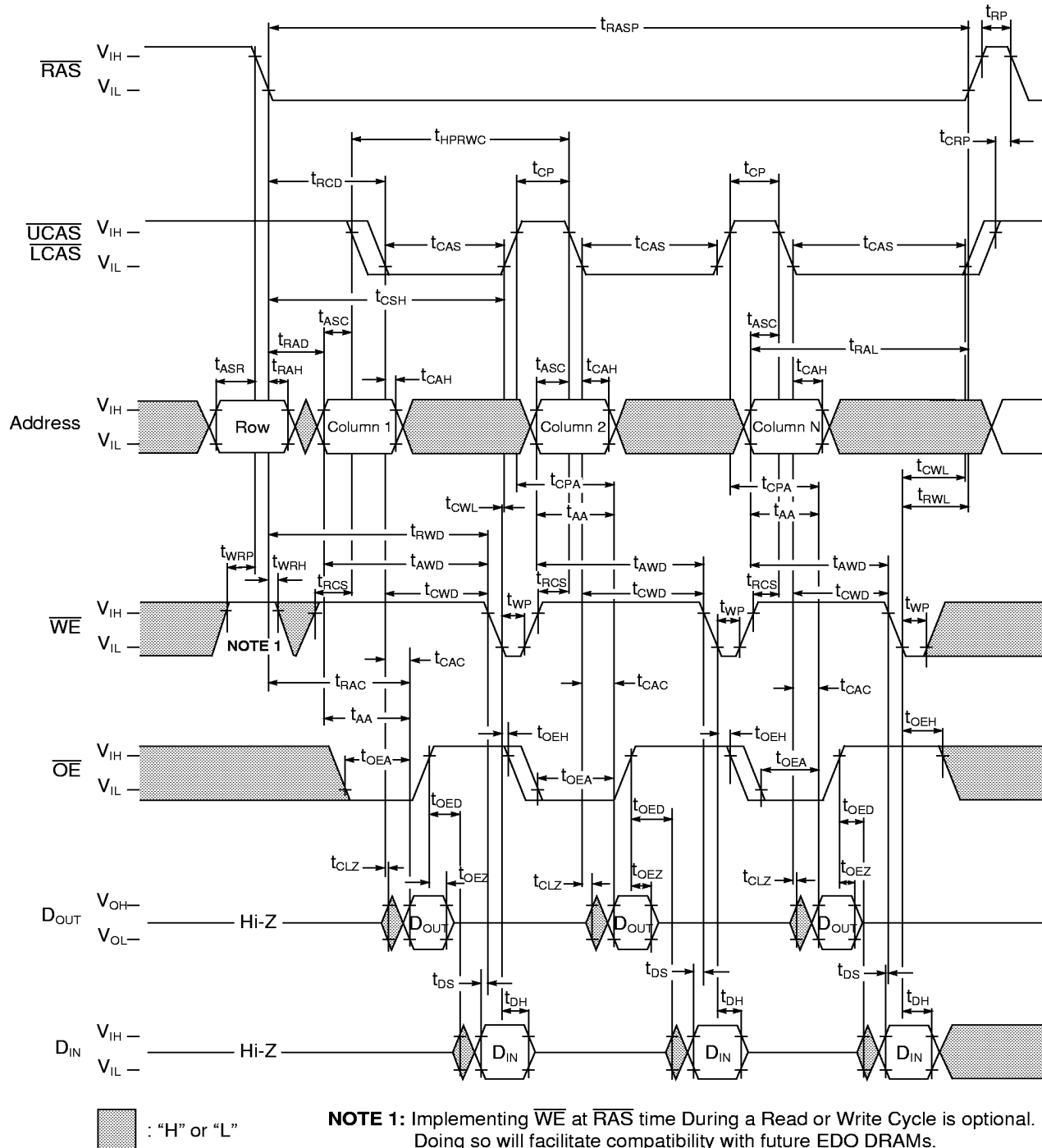
◻ : "H" or "L"

$\overline{OE}$ = Don't care

EDO (Hyper Page) Mode Late Write Cycle



EDO (Hyper Page) Mode Read Modify Write Cycle

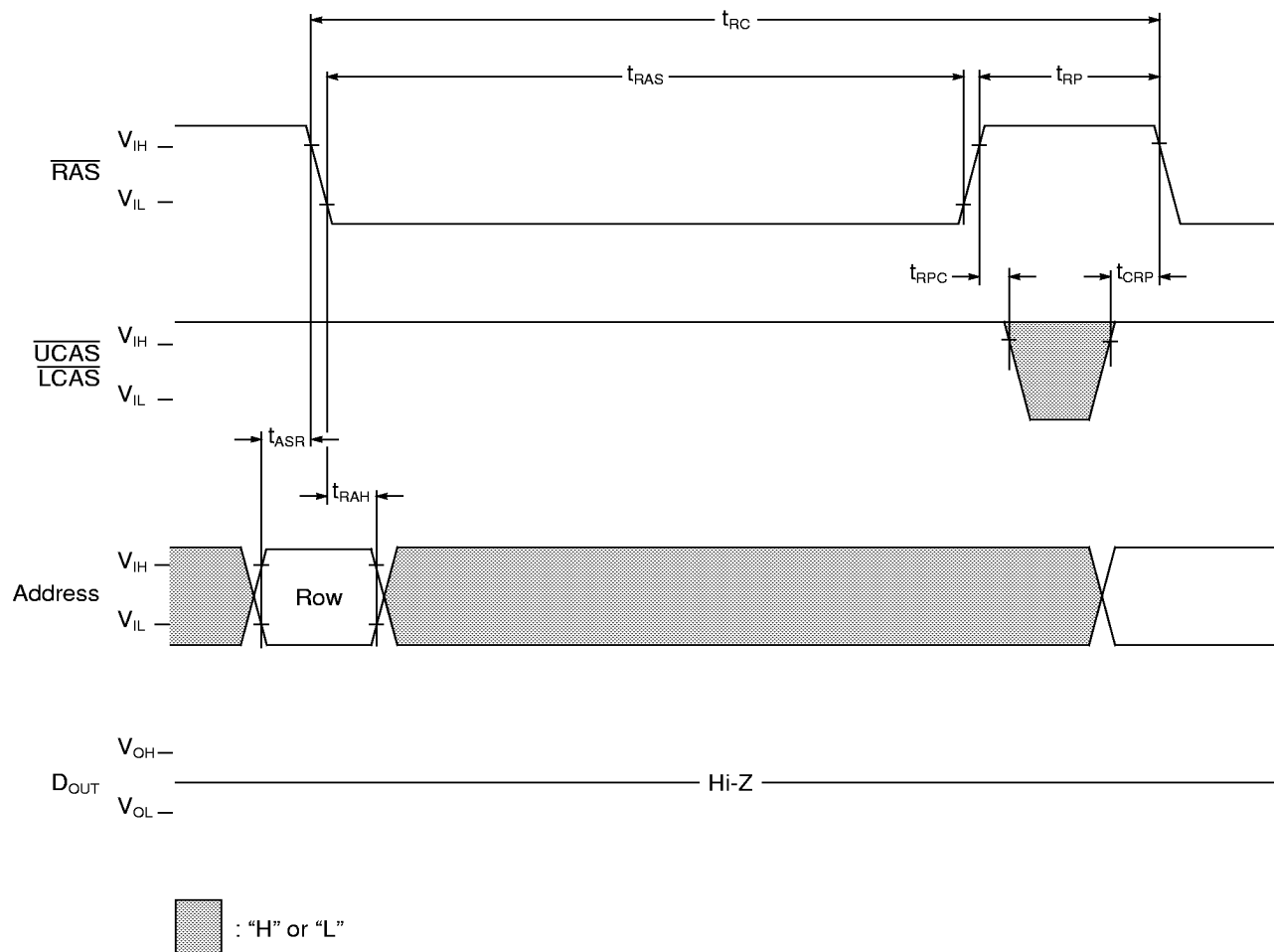


The diagram illustrates the timing relationships for a DRAM read cycle. Key signals and their timing parameters are as follows:

- RAS**: $\overline{\text{RAS}}$ signal. Timing parameters include t_{RAS} (pulse width), t_{RCD} (row-to-column delay), t_{HPC} (high pulse to column precharge), t_{CP} (column precharge), t_{RSH} (row-to-strobe high), t_{RAD} (row-to-address delay), t_{CSH} (column-to-strobe high), t_{ASC} (address-to-strobe), t_{CAH} (column-to-address high), t_{ASR} (address-to-strobe), t_{RAH} (row-to-address high), t_{ASG} (address-to-strobe), t_{RAL} (row-to-address low), t_{CRP} (column-to-row precharge), and t_{RP} (row precharge).
- UCAS/LCAS**: $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ signals. Timing parameters include t_{HPC} (high pulse to column precharge), t_{CP} (column precharge), t_{RSH} (row-to-strobe high), t_{RAD} (row-to-address delay), t_{CSH} (column-to-strobe high), t_{ASC} (address-to-strobe), t_{CAH} (column-to-address high), t_{ASG} (address-to-strobe), t_{RAL} (row-to-address low), t_{CRP} (column-to-row precharge), and t_{RP} (row precharge).
- Address**: Signal for Row, Column 1, Column 2, and Column N. Timing parameters include t_{ASR} (address-to-strobe), t_{RAH} (row-to-address high), t_{ASC} (address-to-strobe), t_{CAH} (column-to-address high), t_{ASG} (address-to-strobe), t_{RAL} (row-to-address low), t_{CRP} (column-to-row precharge), and t_{RP} (row precharge).
- WE**: $\overline{\text{WE}}$ signal. Timing parameters include t_{WRP} (write precharge), t_{WRH} (write-to-row high), t_{RCS} (row-to-column strobe), t_{RCH} (row-to-column strobe), t_{WCS} (write-to-column strobe), t_{WCH} (write-to-column strobe), t_{CPA} (column precharge to address), t_{AA} (address-to-address), t_{OEA} (output enable to address), t_{CAC} (column-to-address), t_{DOH} (data output high), t_{WHZ} (write-to-high impedance), t_{DS} (data strobe), t_{DH} (data high), t_{CLZ} (column-to-low impedance), t_{DOH} (data output high), t_{WHZ} (write-to-high impedance), t_{DS} (data strobe), and t_{DH} (data high).
- OE**: $\overline{\text{OE}}$ signal. Timing parameters include t_{OEA} (output enable to address), t_{CAC} (column-to-address), t_{DOH} (data output high), t_{WHZ} (write-to-high impedance), t_{DS} (data strobe), and t_{DH} (data high).
- DOUT**: D_{OUT} signal. Timing parameters include t_{CLZ} (column-to-low impedance), t_{DOH} (data output high), t_{WHZ} (write-to-high impedance), t_{DS} (data strobe), and t_{DH} (data high).
- DIN**: D_{IN} signal. Timing parameters include t_{CLZ} (column-to-low impedance), t_{DOH} (data output high), t_{WHZ} (write-to-high impedance), t_{DS} (data strobe), and t_{DH} (data high).

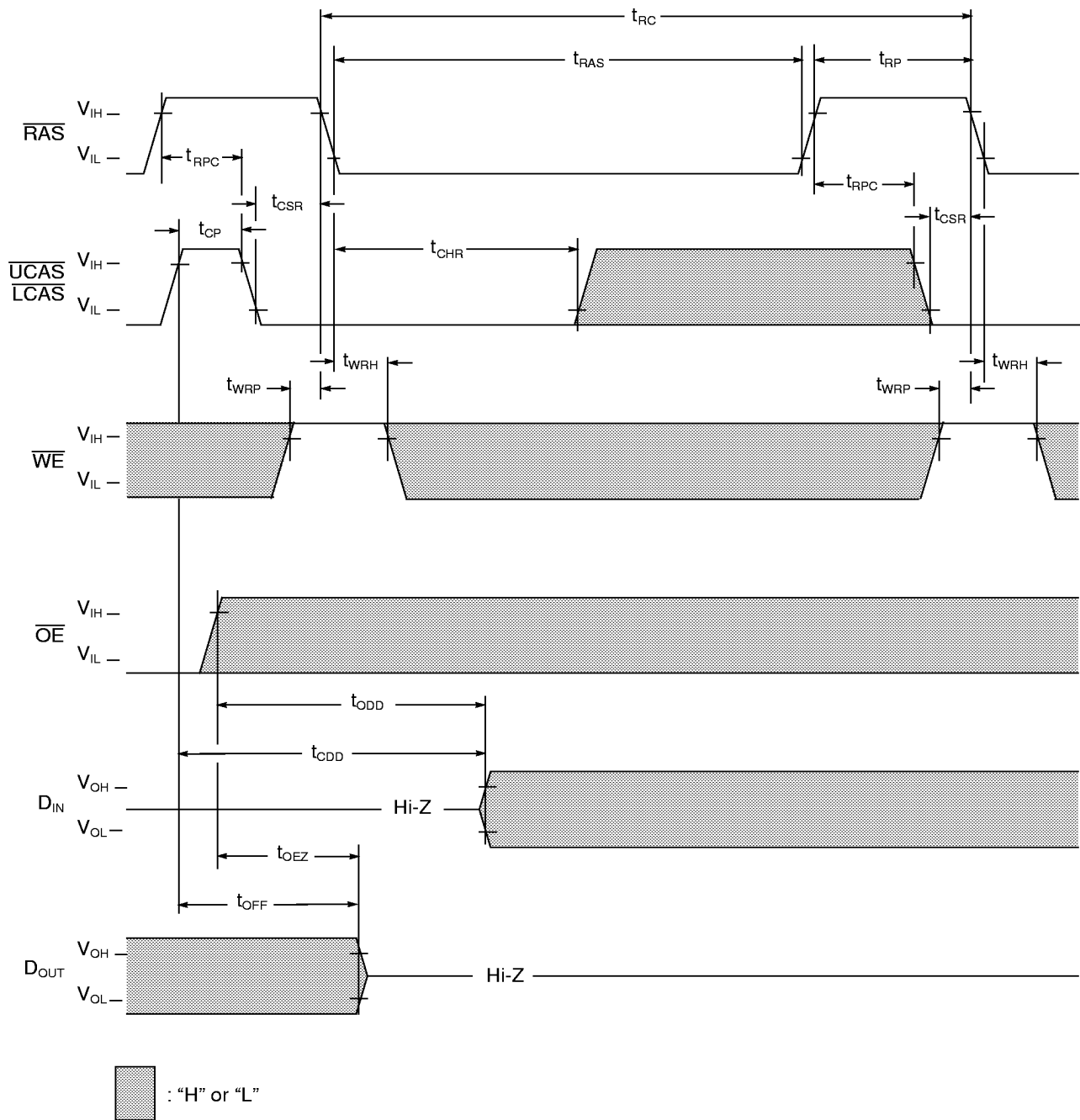
NOTE 1: Implementing $\overline{\text{WE}}$ at $\overline{\text{RAS}}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

$\overline{\text{RAS}}$ Only Refresh Cycle



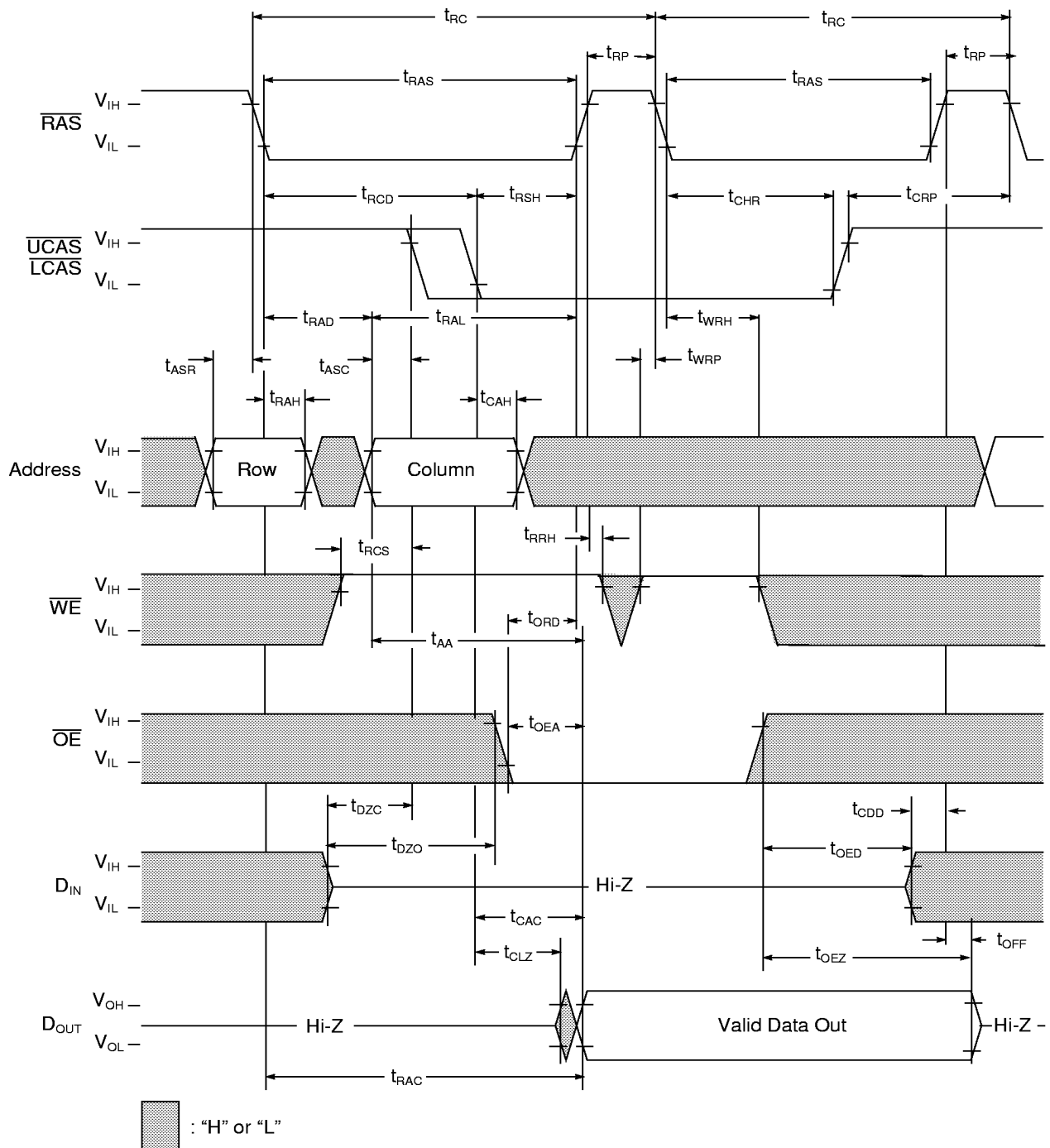
NOTE: $\overline{\text{WE}}$, $\overline{\text{OE}}$ and D_{IN} are "H" or "L"

CAS Before RAS Refresh Cycle

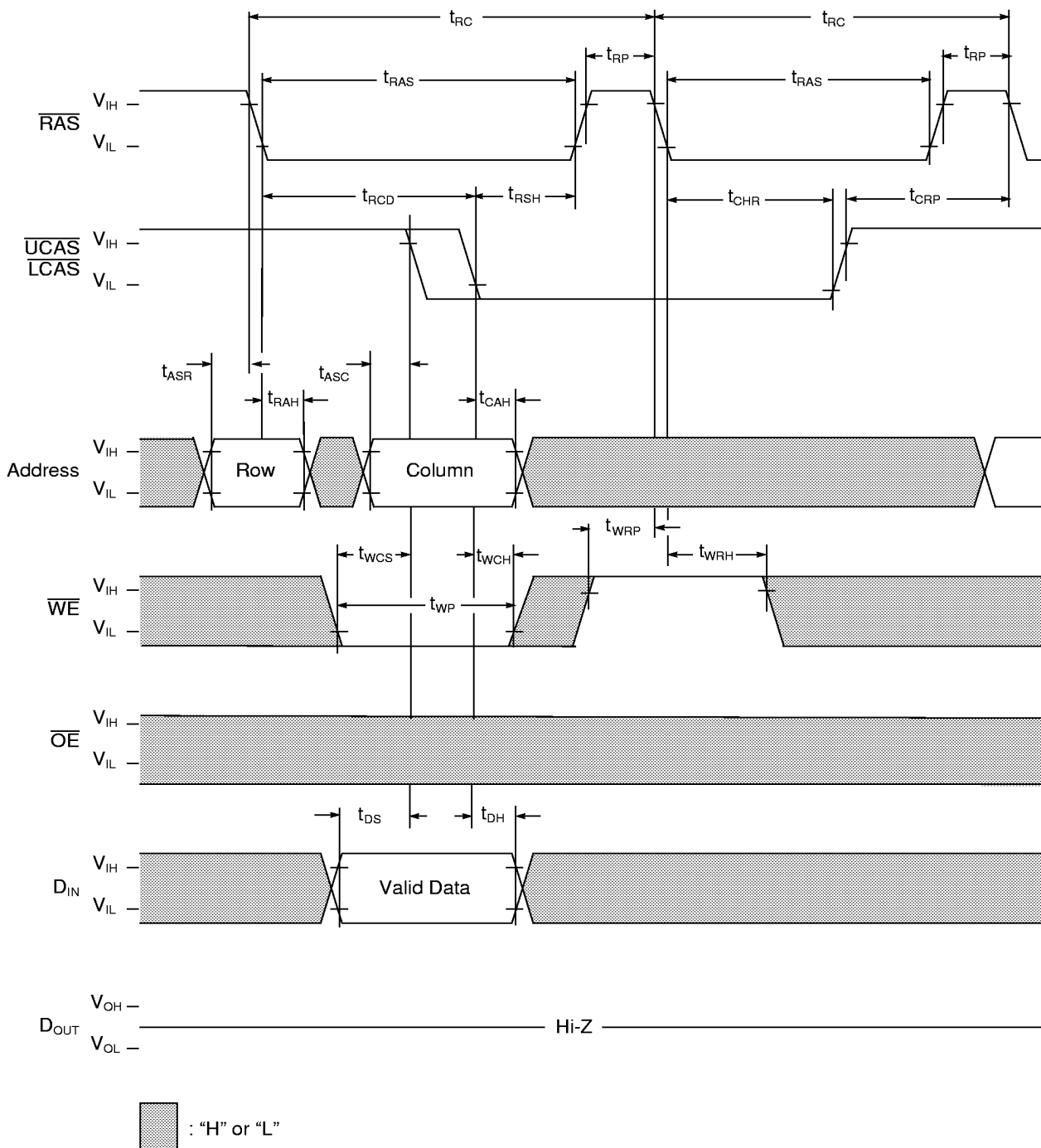


NOTE: Address is "H" or "L"

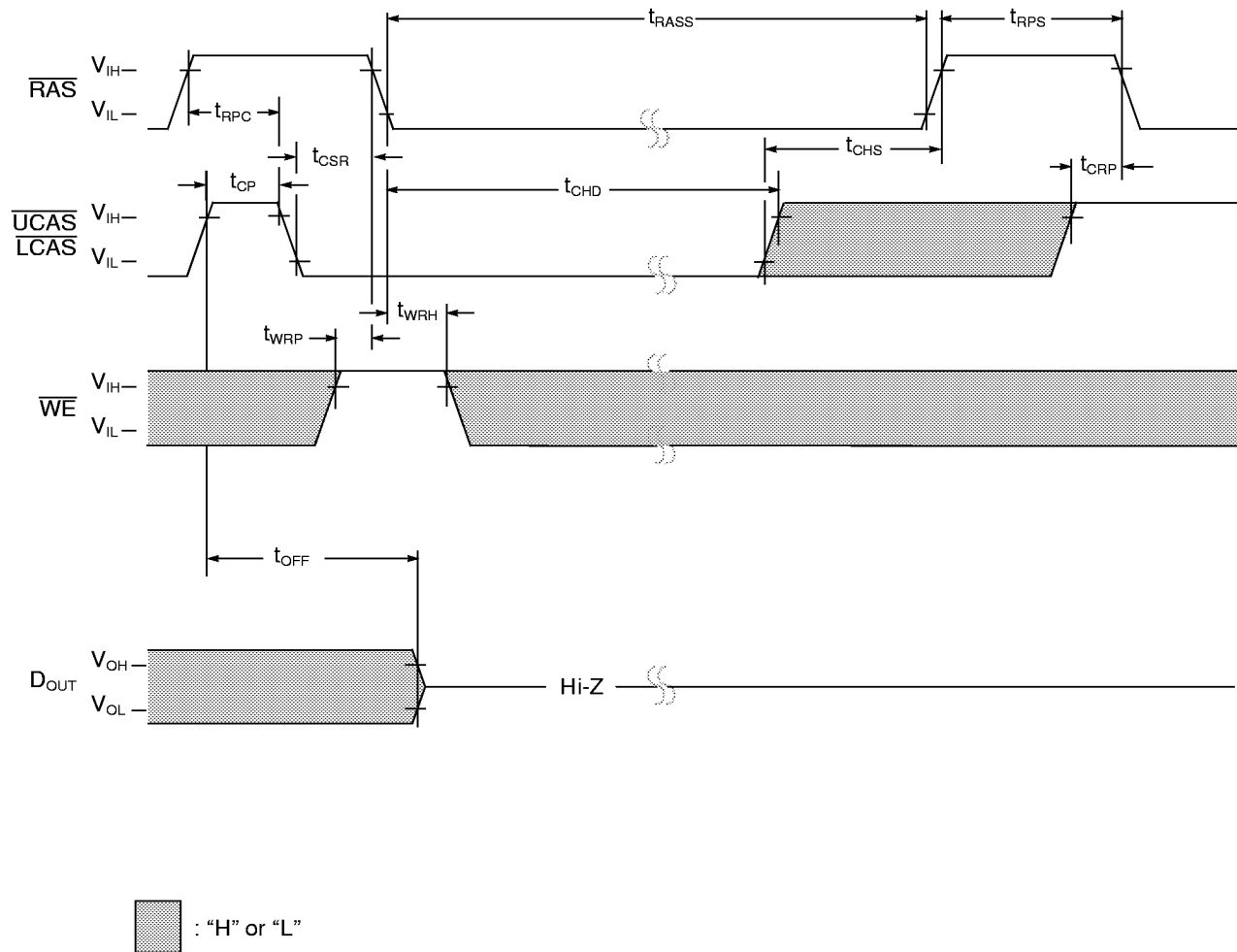
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



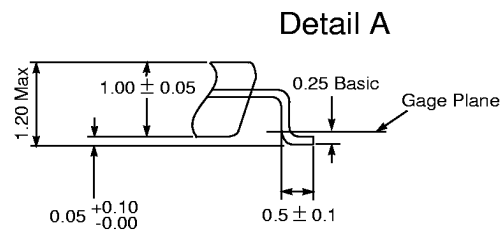
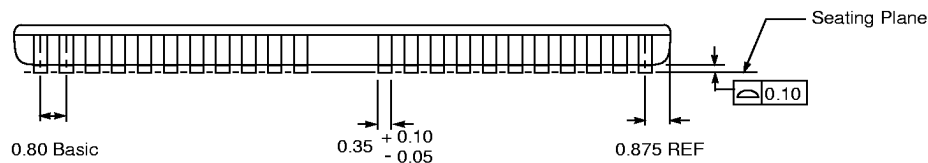
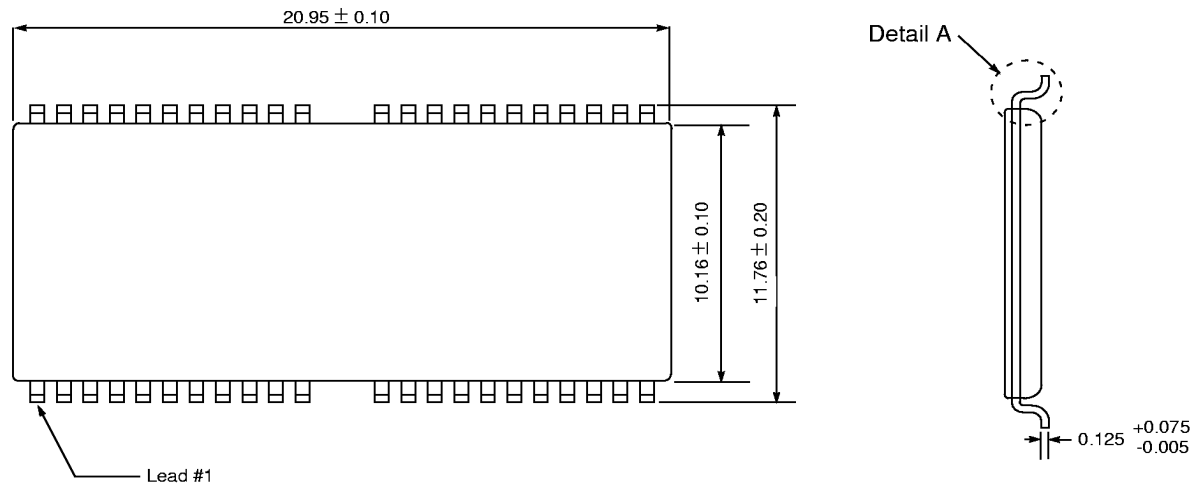
Self Refresh Cycle (Sleep Mode) - Low Power version only



NOTES:

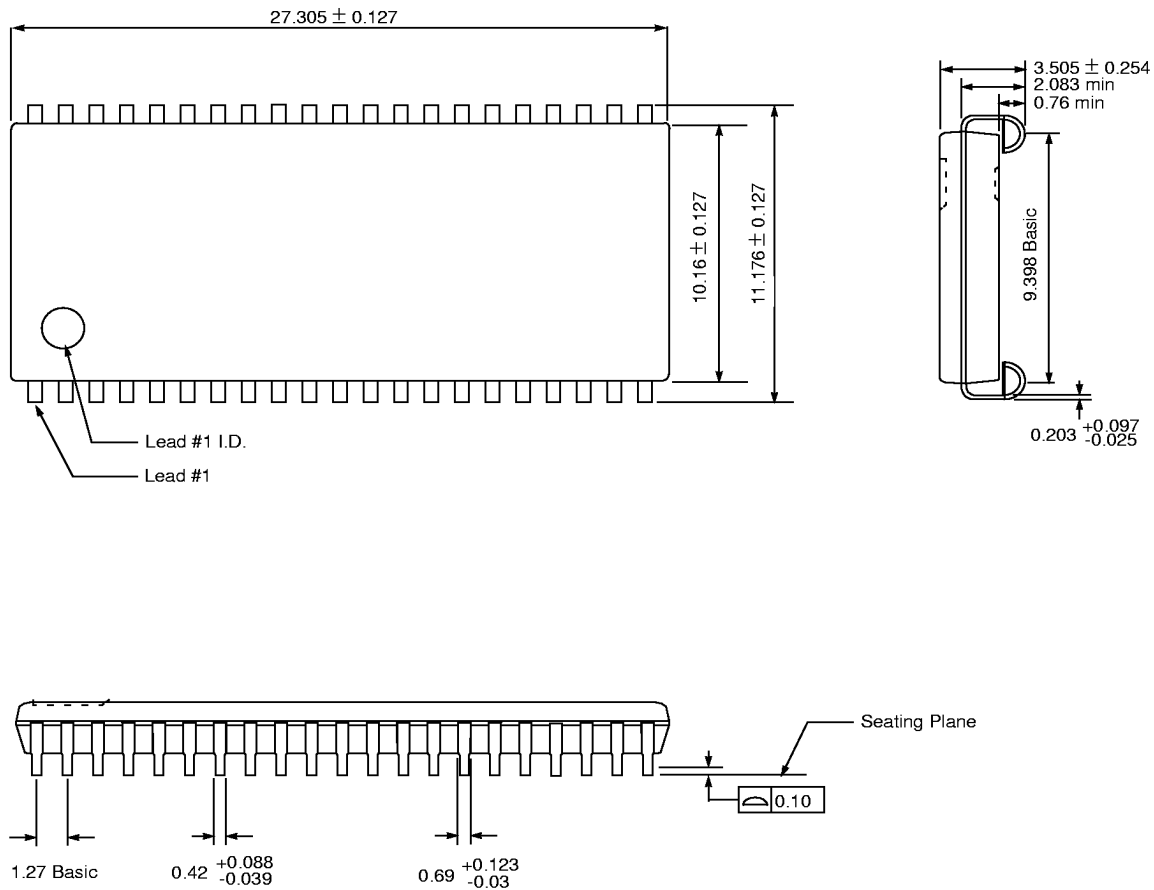
1. Address and $\overline{\text{OE}}$ are "H" or "L"
2. Once $\overline{\text{RAS}}$ (min) is provided and $\overline{\text{RAS}}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."
3. If $t_{\text{RASS}} > t_{\text{CHD}}$ (min) then t_{CHD} applies.
 If $t_{\text{RASS}} \leq t_{\text{CHD}}$ (min) then t_{CHS} applies.

PACKAGE DIMENSIONS (400mil; 50/44 lead; Thin Small Outline Package)



NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

PACKAGE DIMENSIONS (400mil; 42/42 lead; Small Outline J-Lead)



NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

Revision Log

Revision	Contents Of Modification
11/15/95	Initial Release
12/10/95	1. The Low Power and Standard Power Specifications were combined. ES# 28H4722 and ES# 28H4723 were combined into ES# 28H4723. 2. Added Die Rev E part numbers. 3. A -6R speed sort was added, with the following differences over the -60 speed sort: - t_{CAC} was increased from 15ns to 17ns for the -6R speed sort - t_{RCD} (max) was decreased from 45ns to 43ns for the -6R speed sort. - t_{CWD} was increased from 34ns to 36ns for the -6R speed sort. - t_{OEA} was increased from 15ns to 17ns for the -6R speed sort. 4. t_{CHD} was added to the Self Refresh Cycle with a value of 350μs for all speed sorts. 5. The Self Refresh timing diagram was changed to allow $\overline{CAS}$ to go high t_{CHD} (350μs) after $\overline{RAS}$ falls entering a Self Refresh. 6. The CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles. 7. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from "L" to "H".