4M x 4 Stacked DRAM

Features

- 4,194,304 word by 4 bit organization by 2 High
- 4,194,304 word by 4 bit organization by 4 High
- Single 3.3V or 5.0V power supply
- 4096 refresh cycles 64ms
- High Performance:

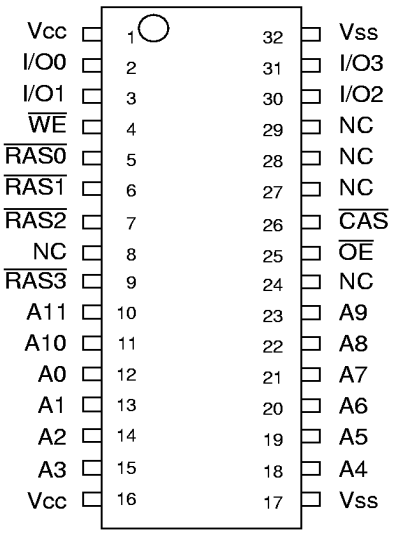
		-60	Units
t_{RAC}	$\overline{RAS}$ Access Time	60	ns
t_{CAC}	$\overline{CAS}$ Access Time	15	ns
t_{AA}	Column Address Access Time	30	ns
t_{RC}	Cycle Time	110	ns
t_{PC}	Fast Page Mode Cycle Time	40	ns

- Low Power Dissipation (per deck)
  - Active (max) - 45mA
  - Standby (TTL Inputs) - 1.0mA (max)
  - Standby (CMOS Inputs) - 1.0mA (max)
- Fast Page Mode
- Read-Modify-Write
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
- $\overline{RAS}$ only Refresh
- Hidden Refresh
- Package: TSOJ-32 (400mil x 825mil)

Description

The IBM01164B0 and IBM01164D0 are dynamic RAMs organized 4,194,304 words by 4 bits in 2 high or 4 high stacks, respectively. These devices are fabricated in IBM's advanced 0.5µm CMOS silicon gate process technology. The circuit and process have been carefully designed to provide high performance, low power dissipation, and high reliability. The devices operate with a single 3.3V or 5.0V power supply. The 22 addresses required to access any bit of data are multiplexed (12 are strobed with $\overline{RAS}$, 10 are strobed with $\overline{CAS}$). The 2 High requires 2 $\overline{RAS}$ pins and the 4 High requires 4 $\overline{RAS}$ pins.

Pin Assignments (Top View)



Pin Description

$\overline{RAS0}$-$\overline{RAS1}$	Row Address Strobe- 2 High
$\overline{RAS0}$-$\overline{RAS3}$	Row Address Strobe- 4 High
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/Write Input
A0 - A11	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O3	Data Input/Output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground

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GA14-4248-02
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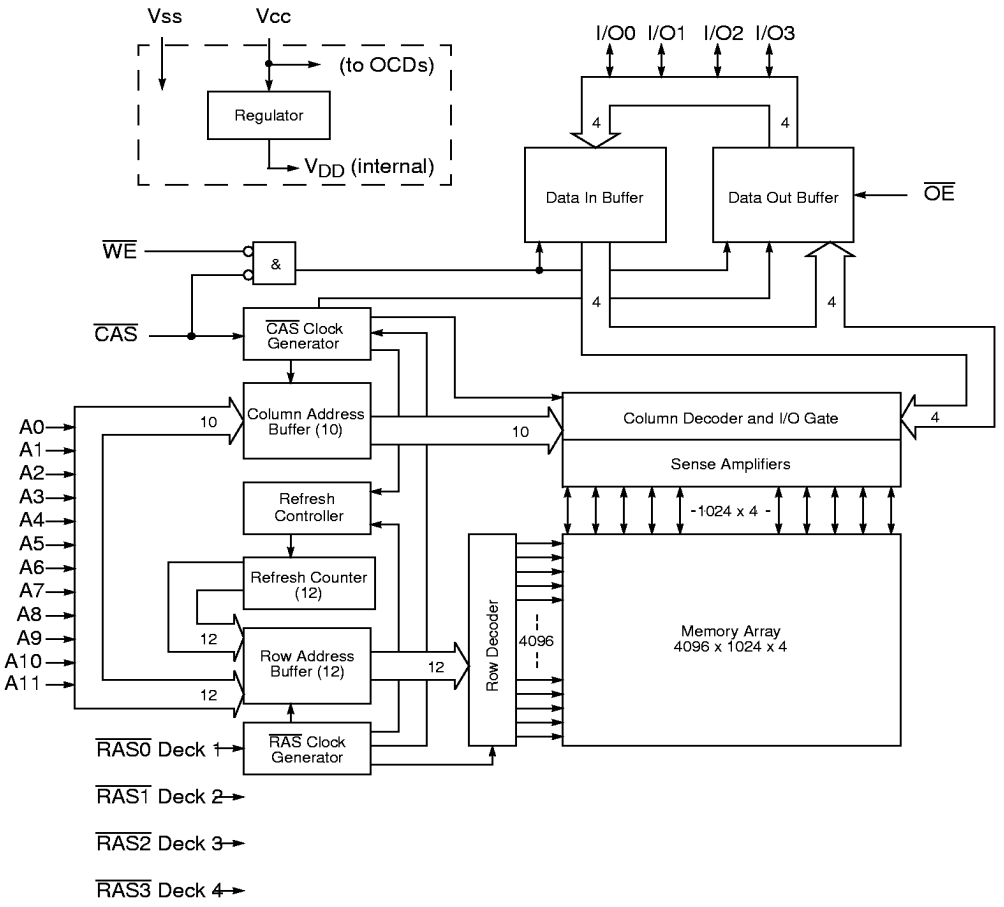
Ordering Information

Part Number	Power Supply	Speed	Package
IBM01164B0BT3 -60	3.3V	60ns	400mil TSOJ 32- 2 High
IBM01164B0T3 -60	5.0V	60ns	400mil TSOJ 32- 2 High
IBM01164D0BT3 -60	3.3V	60ns	400mil TSOJ 32- 4 High
IBM01164D0T3 -60	5.0V	60ns	400mil TSOJ 32- 4 High

Block Diagram



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Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Col Address	I/O0 - I/O3
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col	Data Out
Early-Write		L	L	L	X	Row	Col	Data In
Delayed-Write		L	L	H→L	H	Row	Col	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H→L	H	L	Row	Col	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col	Data Out
Fast Page Mode Write	1st Cycle	L	H→L	L	X	Row	Col	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col	Data In
Fast Page Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col	Data Out
	Write	L→H→L	L	L→H	X	Row	Col	Data In

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Absolute Maximum Ratings

Symbol	Parameter	3.3 Volt Device	5.0 Volt Device	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to +4.6	-1.0 to +7.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	-0.5 to min (V_{CC}+0.5, 7.0)	V	1
T_{CASE}	Operating Temperature (Case)	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A = 0 to 70˚C)

Symbol	Parameter	3.5Volt Device			5.0Volt Device			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.5	5.0	5.5	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.5	2.4	—	V_{CC}+ 0.5	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt pulse widths,or Vcc+2.0V for pulse widths of≤4.0ns (or Vcc+1.0V for ≤8.0ns) with 5.0Volt. Additionally, V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns with 3.3 Volt or to -2.0V for pulse widths ≤4.0ns (or 1.0V for ≤8.0ns) with 5.0Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance (T_A= 25°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	—	5	pF	1, 2
C_{RAS}	Input Capacitance ($\overline{RAS0}$-$\overline{RAS3}$)	—	7	pF	1
C_{I2}	Input Capacitance ($\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1, 2
C_O	Output Capacitance (I/O0 - I/O3)	—	7	pF	1, 2

1. Input capacitance measurements made with rise time shift method with $\overline{CAS}$ = V_{IH} to disable output.
2. Multiply given planar values by 2 or by 4 for 2 or 4 High stacked DRAM, respectively.

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DC Electrical Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0..3V or V_{CC}= 5.0V ± 0..5V)

Symbol	Parameter	Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min.)	—	45	mA	1, 2, 3
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})	—	1	mA	4
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	—	45	mA	1, 3
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	—	25	mA	1, 2, 3
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)	—	1	mA	4
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	—	45	mA	1, 3
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)), All Other Pins Not Under Test = 0V	-5	+5	µA	4
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC})	-5	+5	µA	4
V_{OH}	Output Level (TTL) Output “H” Level Voltage, I_{OUT} = -2.0mA	2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output “L” Level Voltage, I_{OUT} = +2.0mA	0.0	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ =V_{IL}. In the case of I_{CC4}, it can be changed once or less when $\overline{CAS}$ =V_{IH}.
4. Multiply given planar values by 2 or by 4 for 2 or 4 High stacked DRAM, respectively.

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AC Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required. Each deck in a stacked module must individually receive the pump-up initialization before proper chip operation is guaranteed.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Valid column addresses are A0 through A9.
5. A maximum of 2 $\overline{RAS}$ inputs may be pulsed in a Read, Write or Refresh Cycle.

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	110	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	60	10K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	ns	
t_{CAH}	Column Address Hold Time	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	ns	1
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	ns	2
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	ns	
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	ns	
t_{DZO}	$\overline{OE}$ Delay Time from D_{IN}	0	—	ns	3
t_{DZC}	$\overline{CAS}$ Delay Time from D_{IN}	0	—	ns	3
t_T	Transition Time (Rise and Fall)	3	50	ns	4

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Either t_{DZC} or t_{DZO} must be satisfied.
4. AC measurements assume t_T=5ns.

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Write Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	ns	1
t_{WCH}	Write Command Hold Time	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	15	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	ns	3
t_{DH}	D_{IN} Hold Time	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
2. Either t_{CDD} or t_{OED} must be satisfied.
3. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

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Read Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	ns	1, 3
t_{AA}	Access Time from Address	—	30	ns	1, 2
t_{OEA}	Access Time from $\overline{OE}$	—	15	ns	3
t_{RCS}	Read Command Setup Time	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	ns	3
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	ns	3
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	ns	3
t_{OH}	Output Data Hold Time	3	—	ns	
t_{OHO}	Output Data Hold from $\overline{OE}$	3	—	ns	
t_{OFF}	Output Buffer Turn-Off Delay	—	15	ns	5
t_{OEZ}	Output Buffer Turn-Off Delay from $\overline{OE}$	—	15	ns	5
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	ns	6

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current load and 100pF.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF} (max) and t_{OEZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
6. Either t_{CDD} or t_{OED} must be satisfied.

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Read-Modify-Write Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	150	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Fast Page Mode Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{PC}	Fast Page Mode Cycle Time	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	200K	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	ns	1
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	ns	

1. Measured with the specified current load and 100pF.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	80	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	55	—	ns	1

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPW} \geq t_{CPW}$ (min)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

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Refresh Cycle

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Cycle)	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	ns	

Refresh

Symbol	Parameter	-60		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ms	1

1. 4096 cycles.

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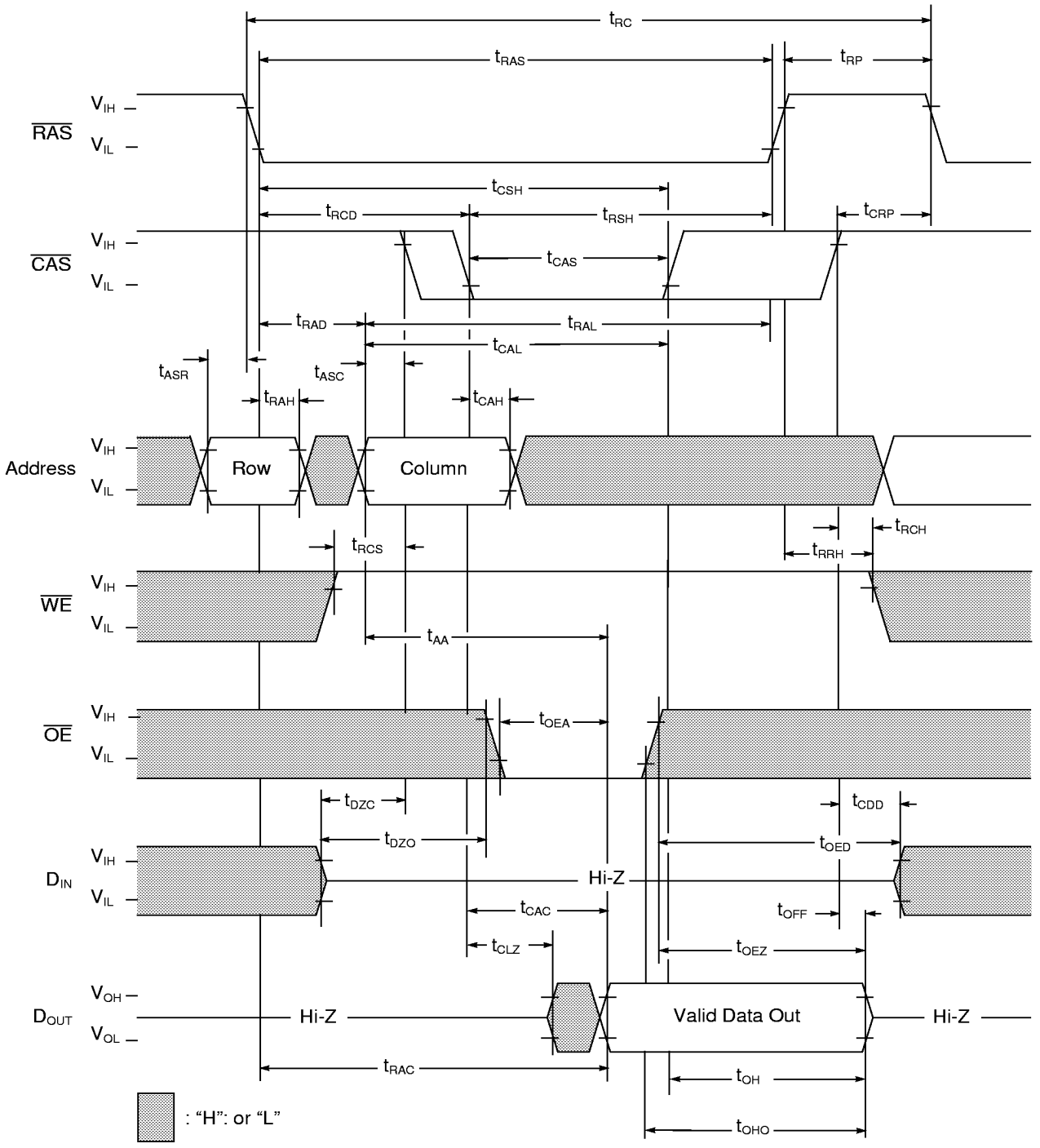
Read Cycle



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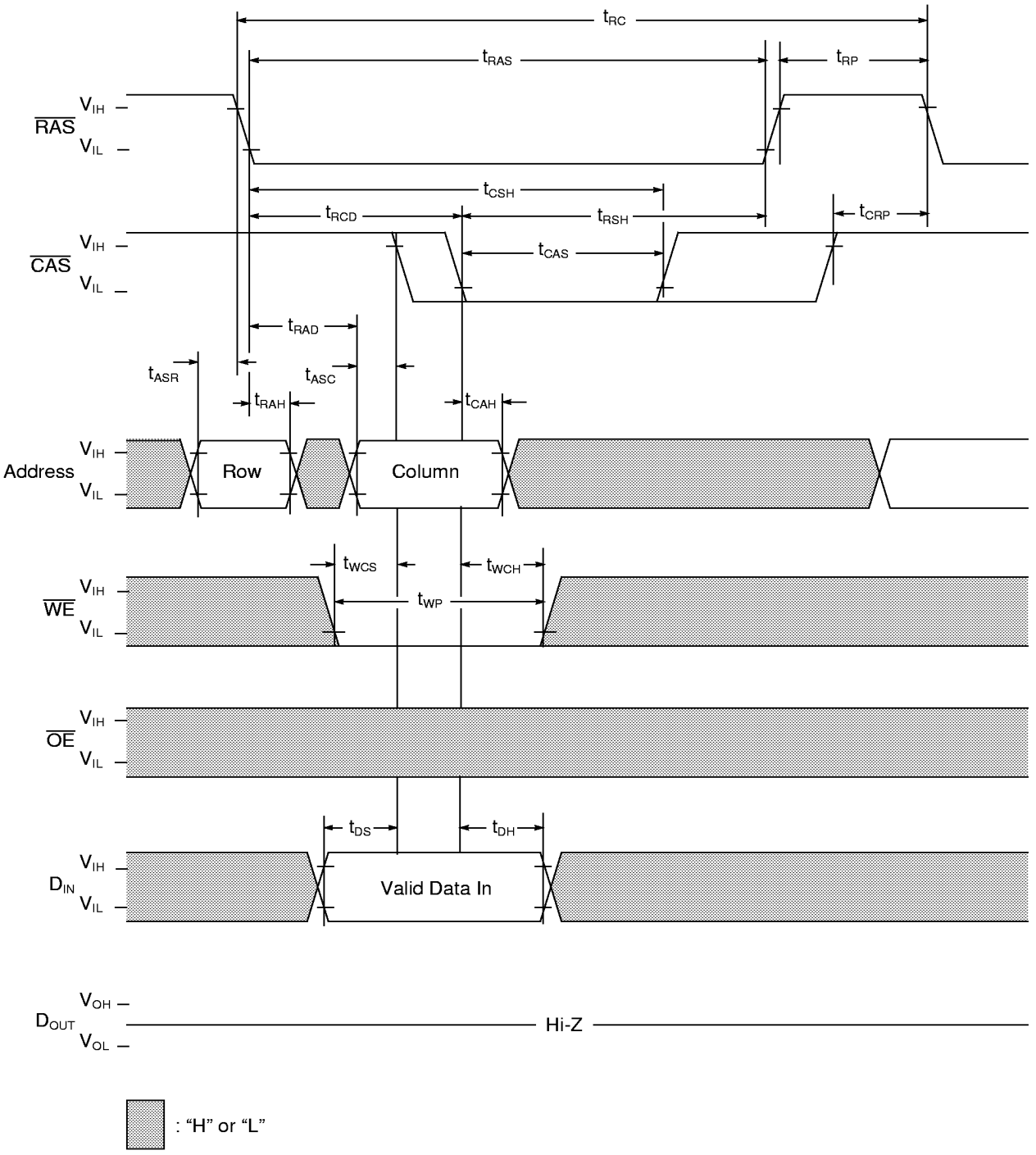
Write Cycle (Early Write)



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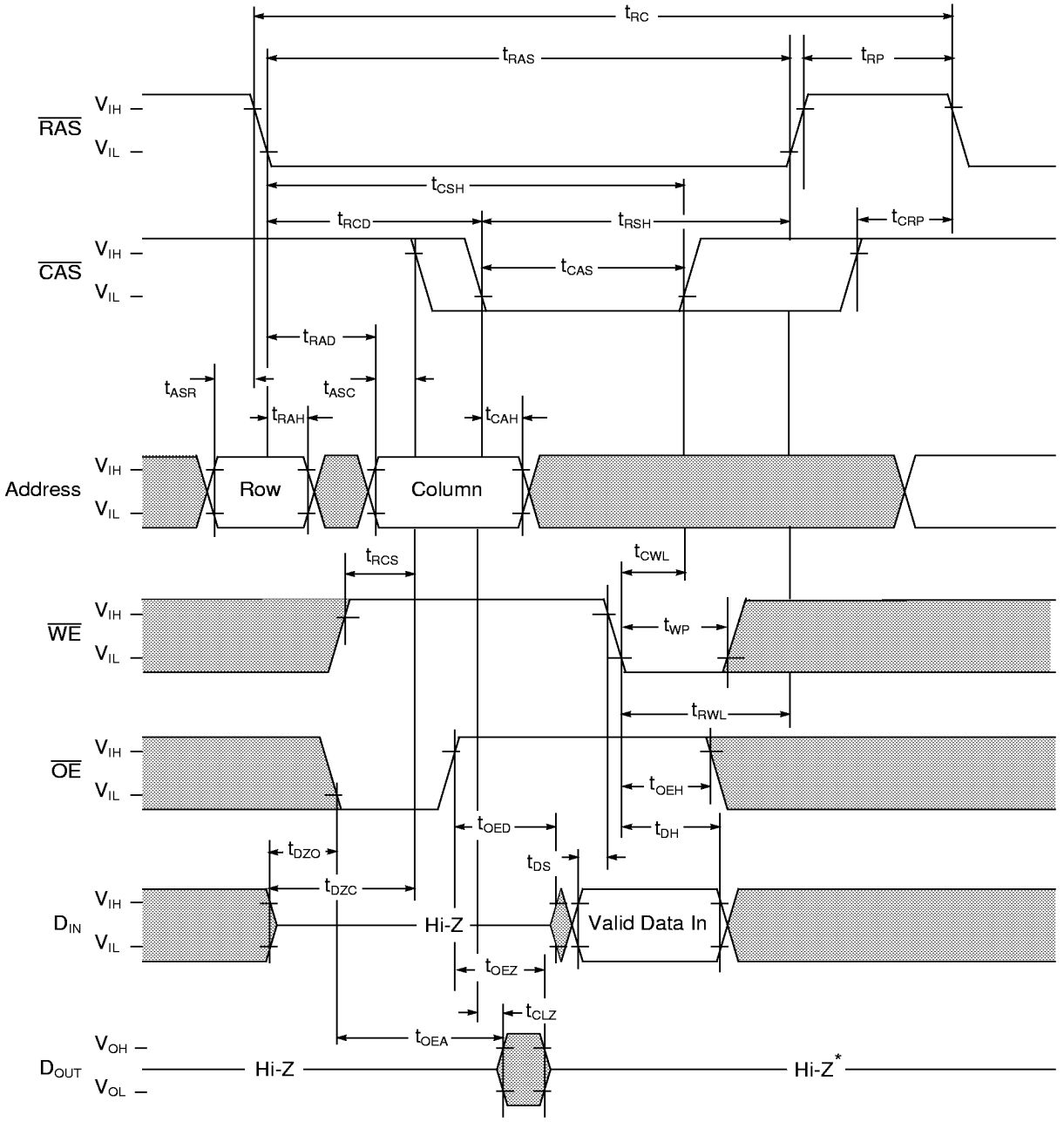
Write Cycle (Delayed Write)



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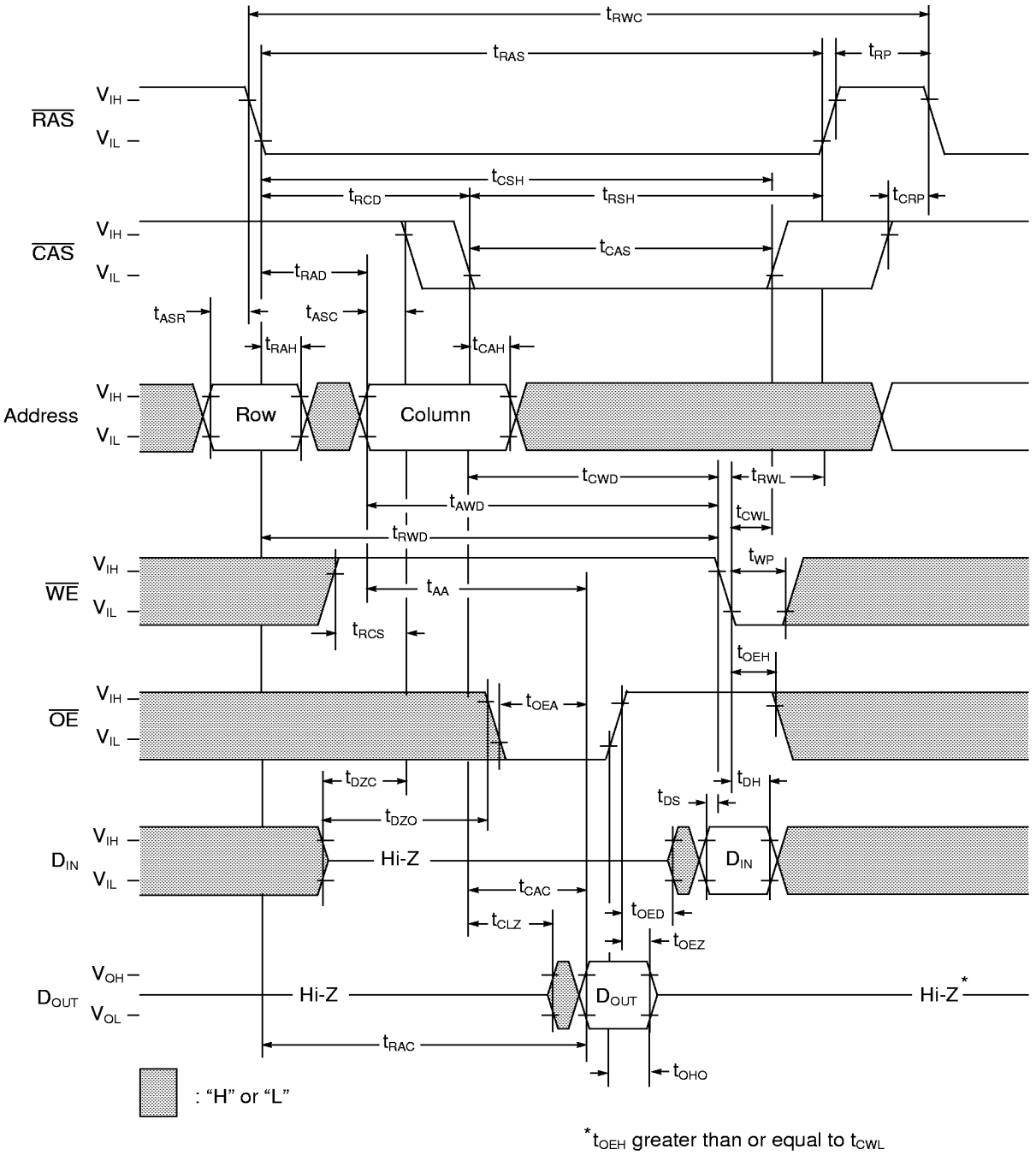
Read-Modify-Write Cycle



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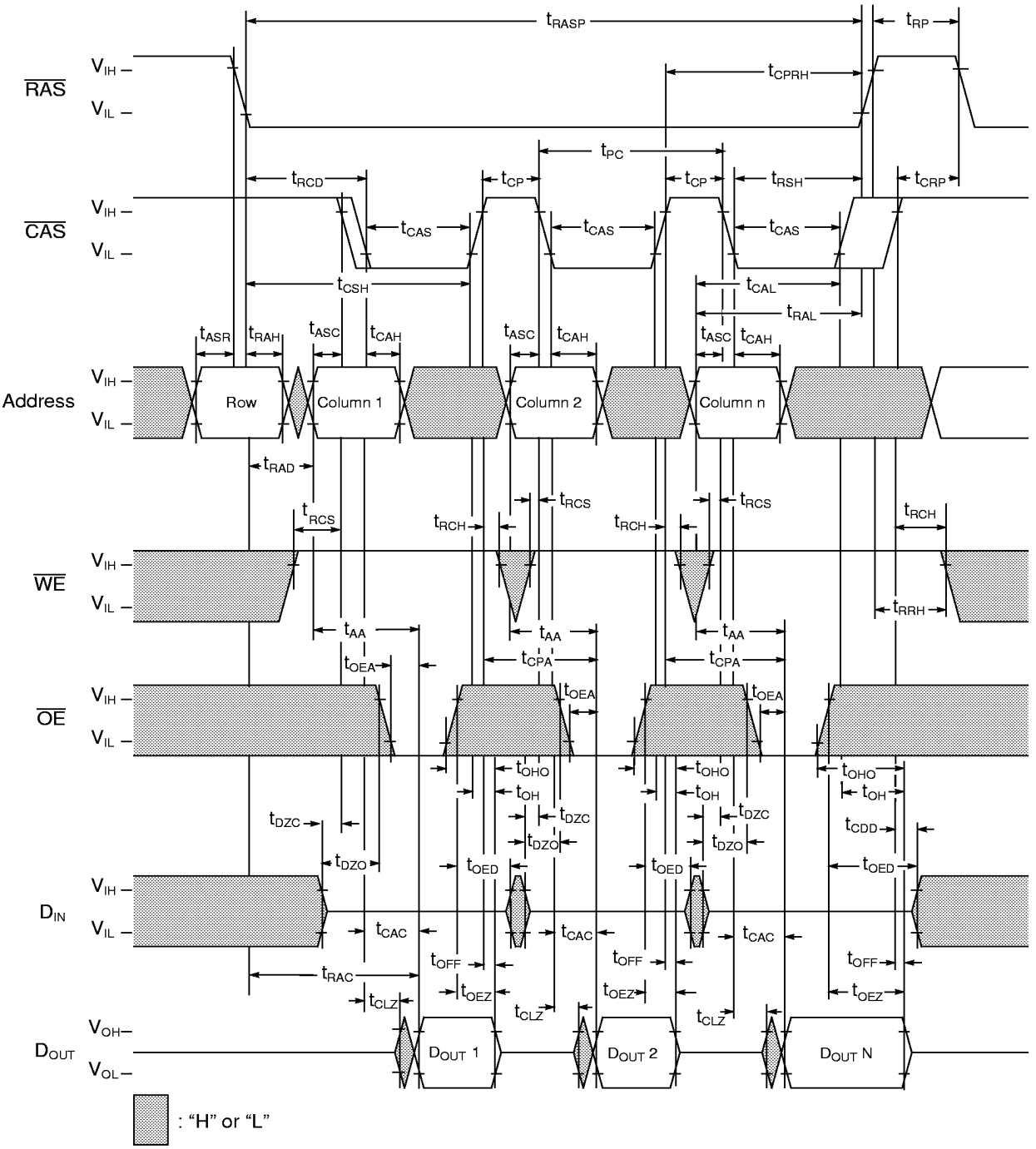
Fast Page Mode Read Cycle



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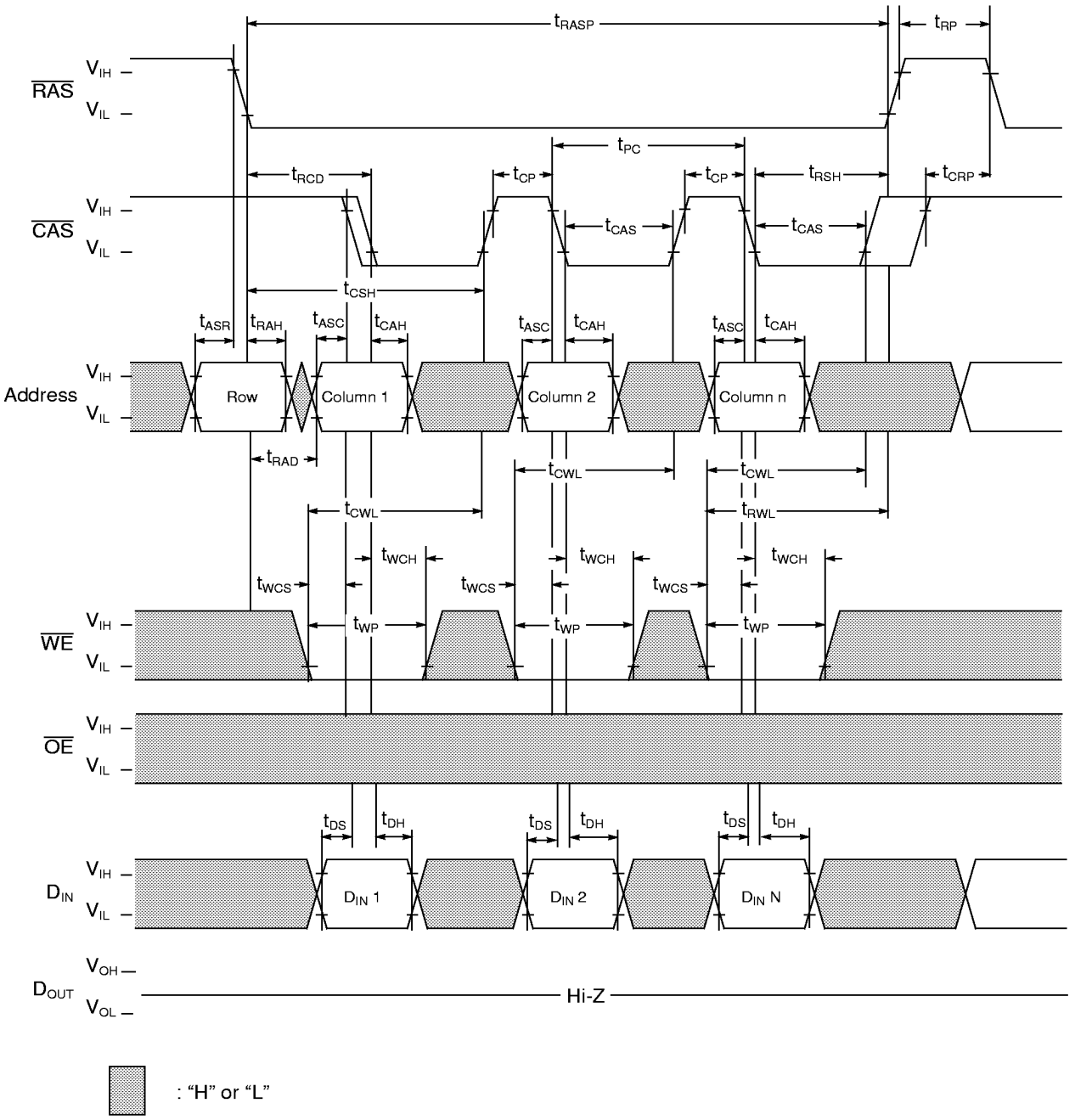
Fast Page Mode Write Cycle



: “H” or “L”

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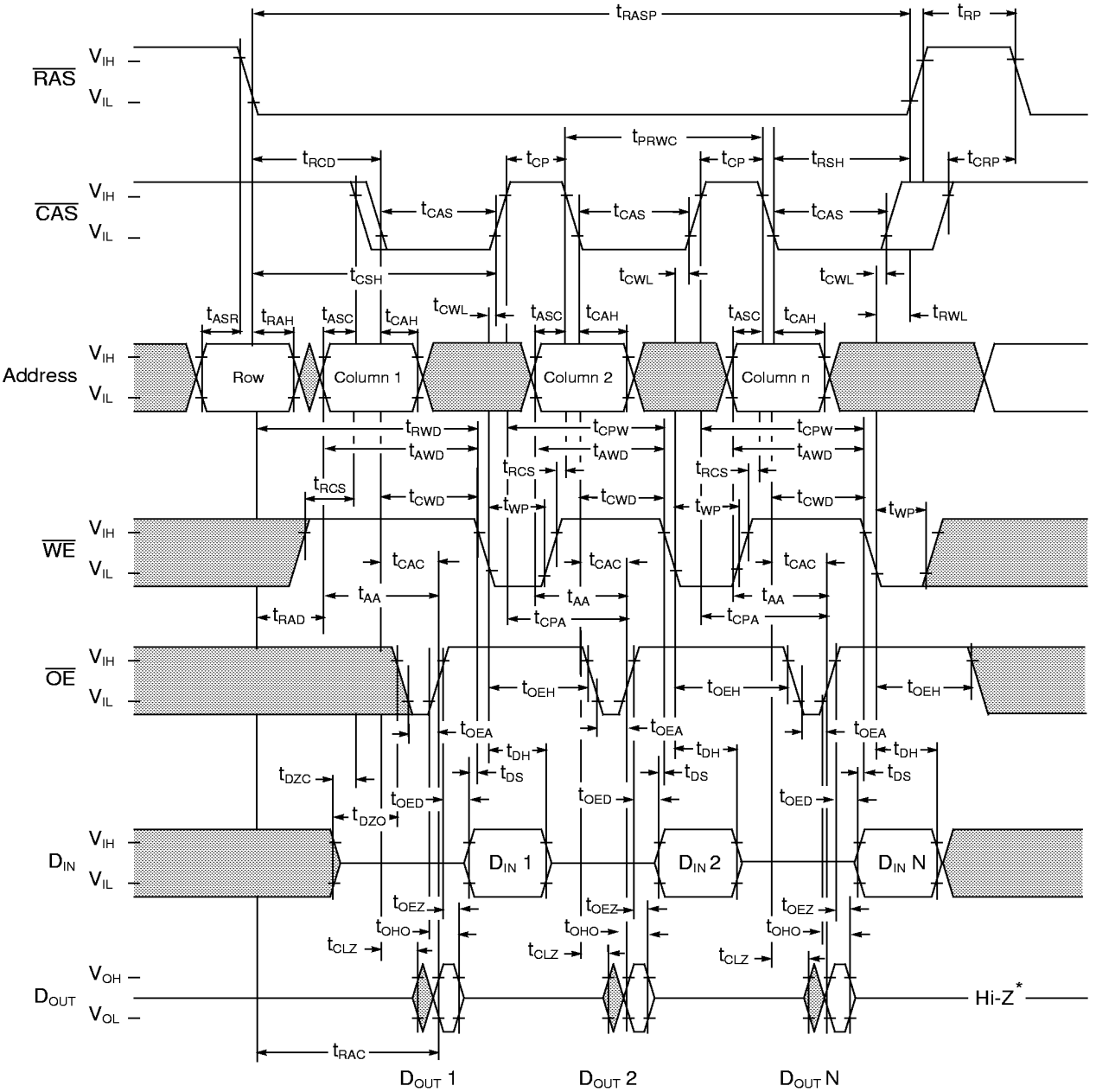
Fast Page Mode Read-Modify-Write Cycle



: "H" or "L"

*t_{OEH} greater than or equal to t_{CWL}

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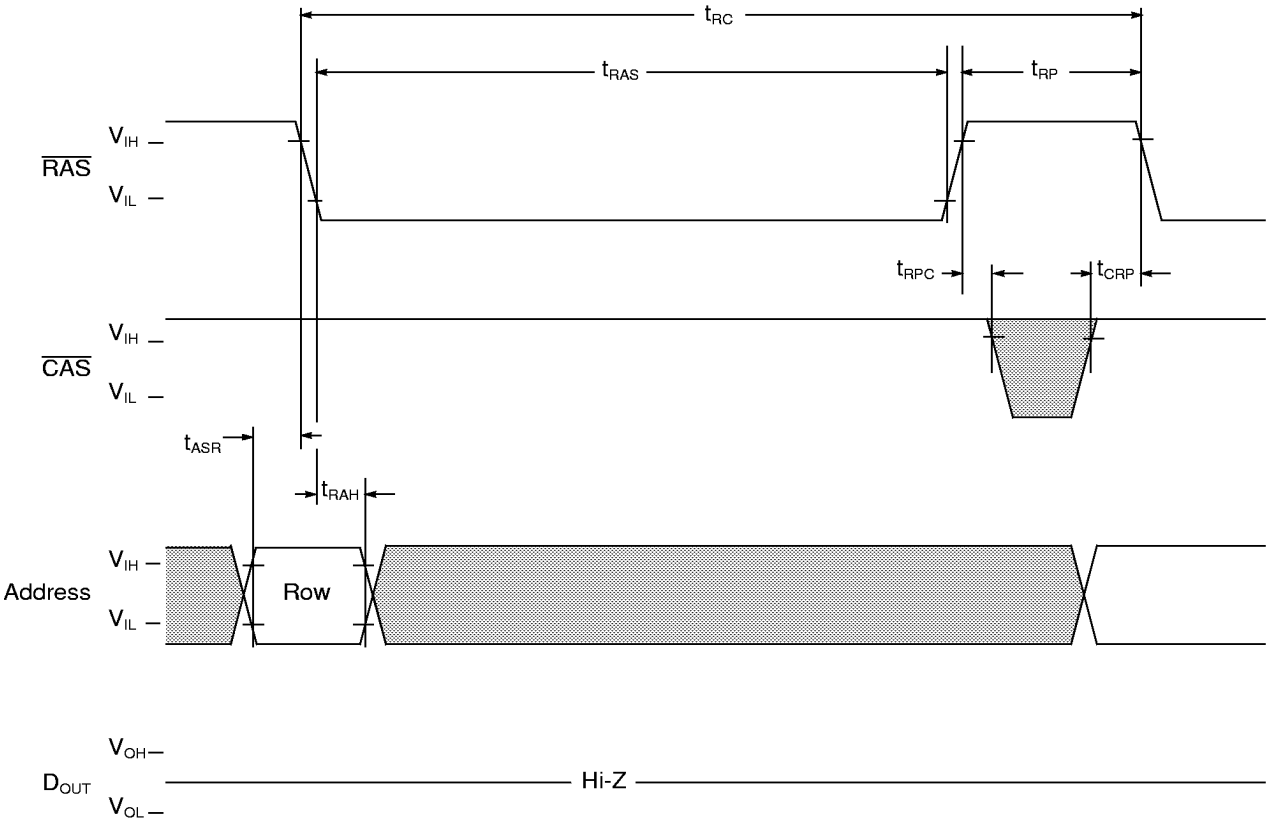
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

NOTE : $\overline{WE}$, $\overline{OE}$ and D_{IN} are "H" or "L"

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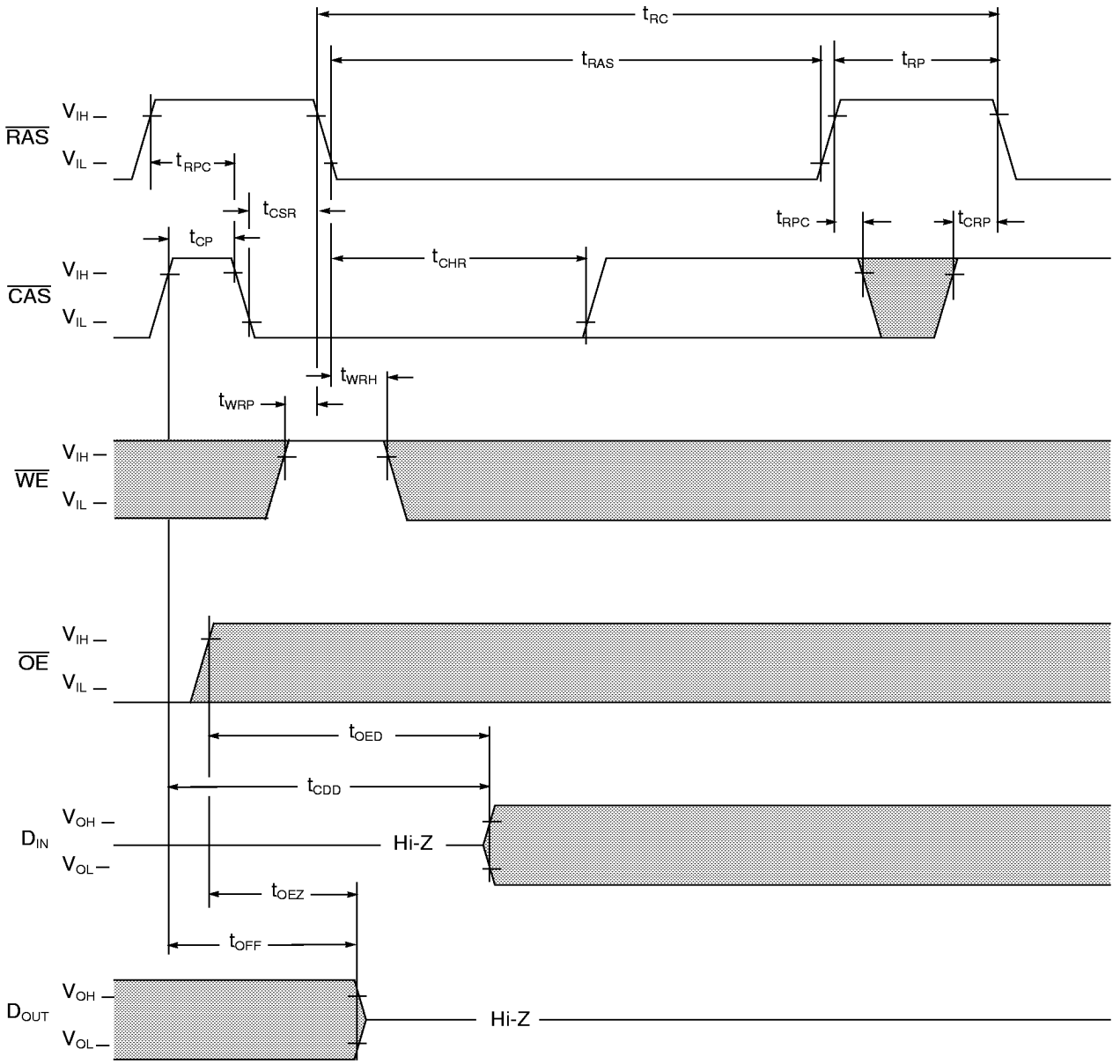
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



: "H" or "L"

NOTE: Address is "H" or "L"

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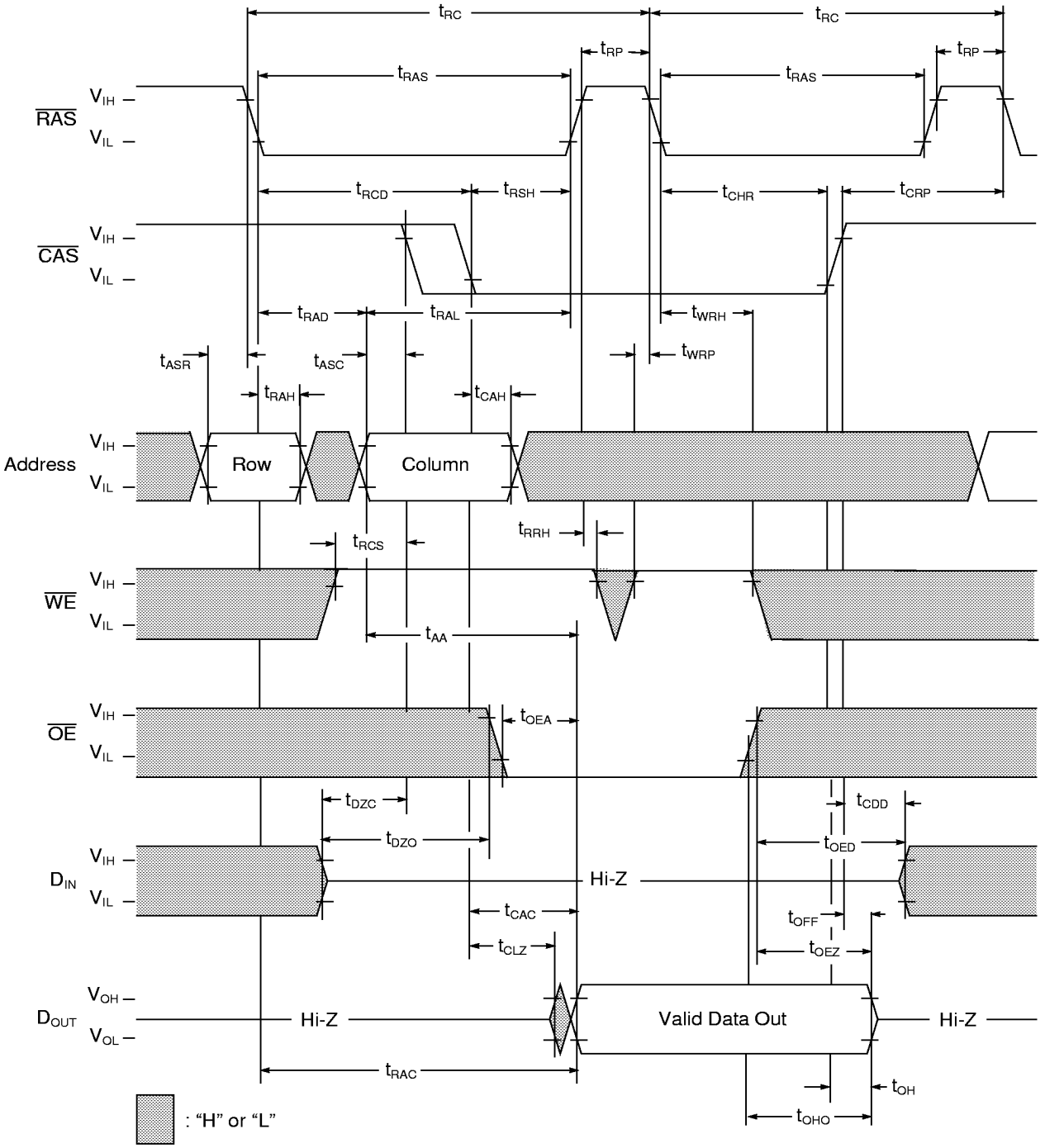
Hidden Refresh Cycle (Read)



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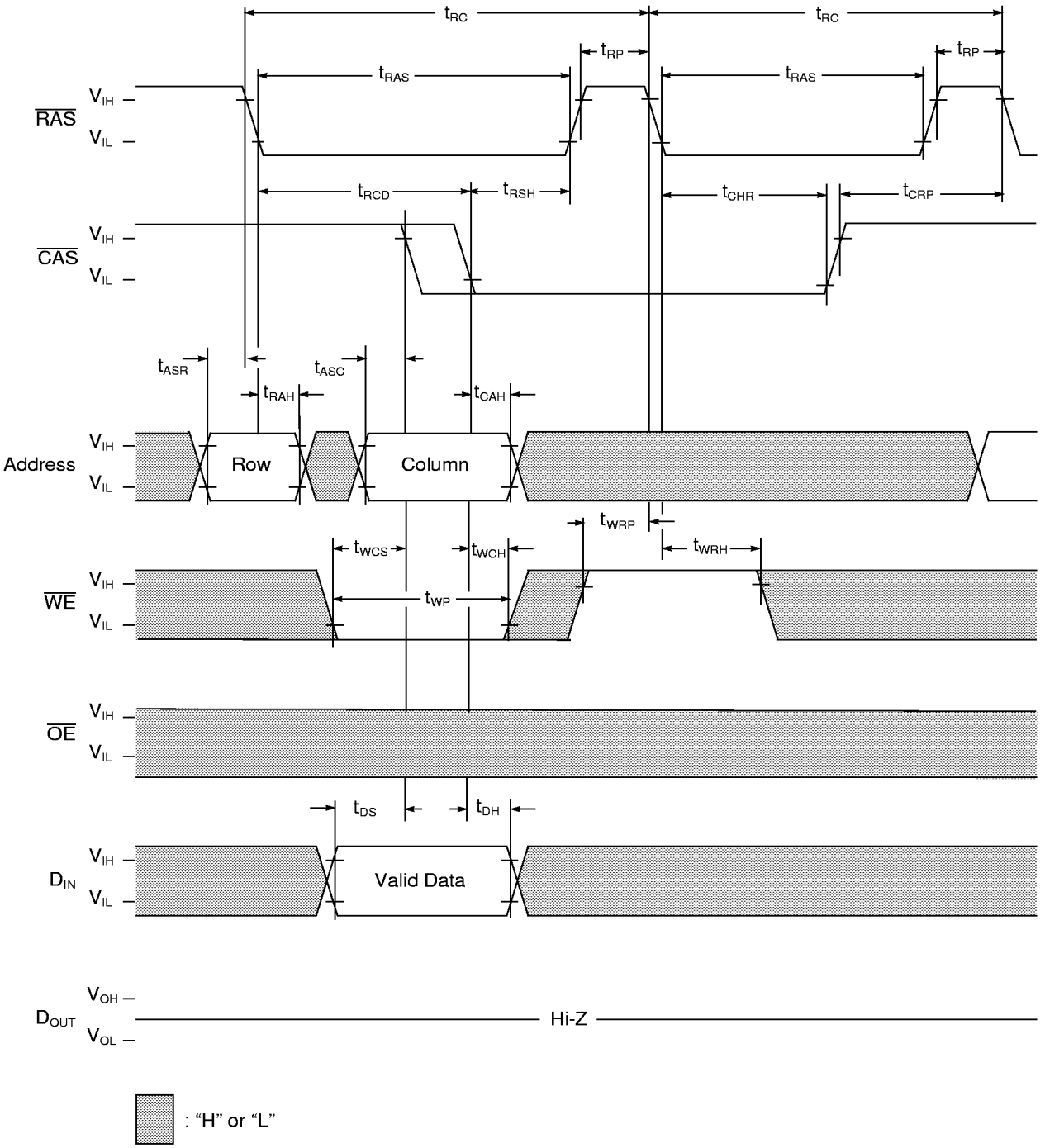
Hidden Refresh Cycle (Write)



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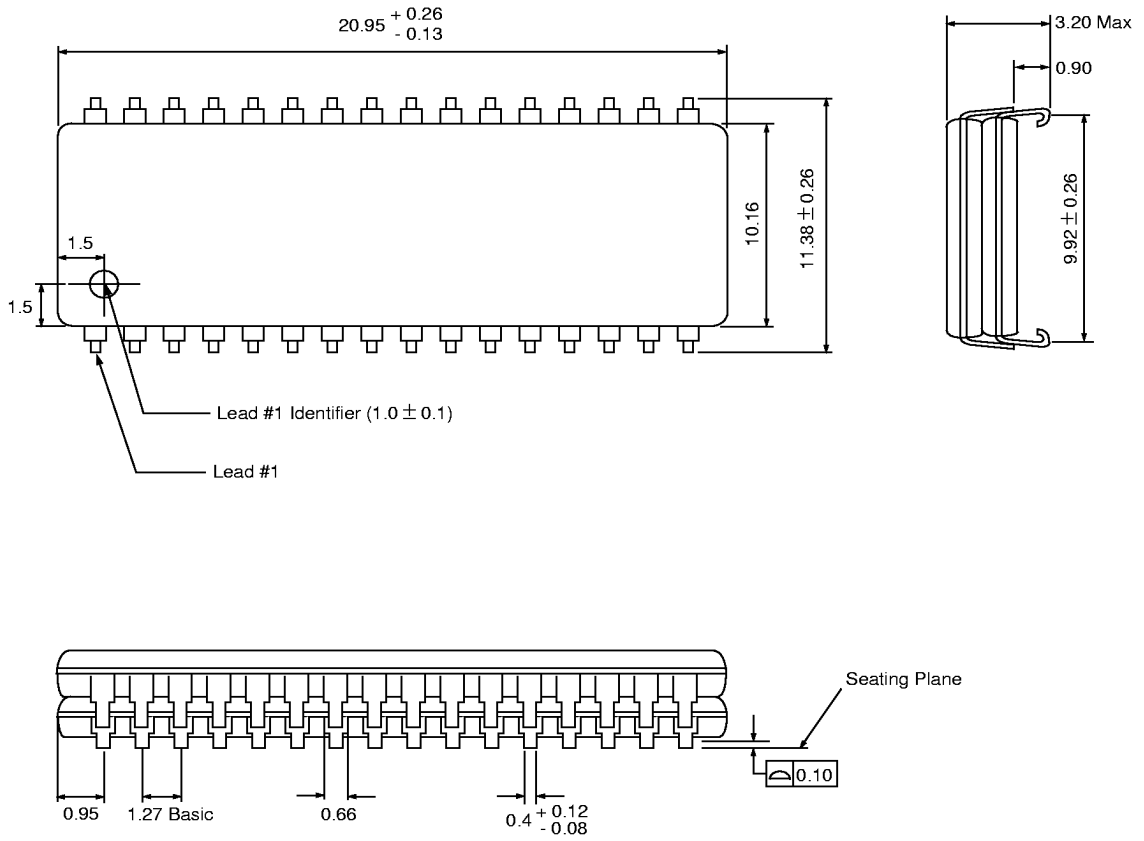
Package Dimensions (400 mil; 32 Lead; 2 High Stack; Thin Small Outline J-Lead)



NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

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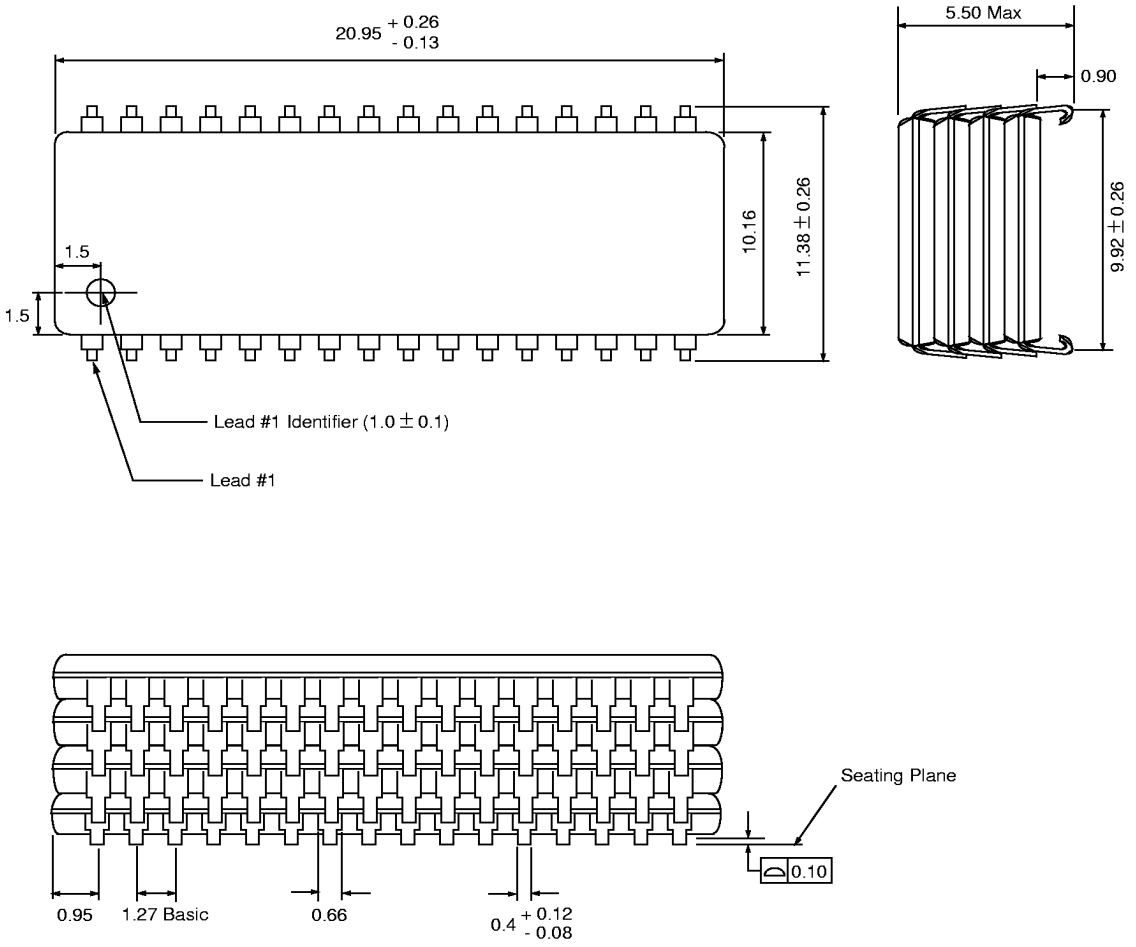
Package Dimensions (400 mil; 32 Lead; 4 High Stack; Thin Small Outline J-Lead)



NOTE: All dimensions are in millimeters; Package Diagrams are not drawn to scale.

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Revision Log

Revision	Contents Of Modification
08/02/96	Initial Release
09/01/96	1. I_{CC2} was changed from 2mA to 1mA. 2. $I_{I(L)}$ and $I_{O(L)}$ were altered from +/- 10uA to +/- 5uA. 3. t_T was initially at a max of 30ns. It has been modified to 50ns for all speed sorts. 4. t_{RASP} max of 125K was raised to 200K for all speed sorts.
03/19/97	1. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “H” to “L”. 2. t_{ODD} was renamed to t_{OED}. 3. t_{OED} was moved from the Common Parameters table to the Write Cycle Parameters Table. 4. The -70 speed sort and timings were removed. 5. I_{cc1}, I_{cc3}, I_{cc6} for the -60 speed sort were reduced from 75mA to 45mA. 6. I_{cc4} for the -60 speed sort was reduced from 65mA to 25mA.

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