1M x 4 10/10 QUAD CAS DRAM

Features

- 1,048,576 word by 4 bit organization
- Power Supply: 3.3 ± 0.3V or 5.0V ± 0.5V
- 1024 Refresh Cycles
  - 16 ms Refresh Rate (SP version)
  - 128 ms Refresh Rate (LP version)
- QUAD $\overline{CAS}$ Parity
- High Performance:

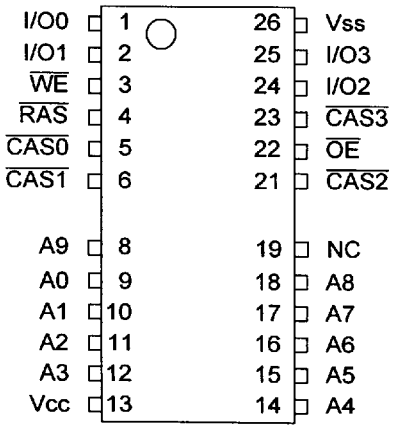
		-60	-70	Units
t_{RAC}	$\overline{RAS}$ Access Time	60	70	ns
t_{CAC}	$\overline{CAS}$ Access Time	15	18	ns
t_{AA}	Column Address Access Time	30	35	ns
t_{RC}	Cycle Time	110	130	ns
t_{PC}	Fast Page Mode Cycle Time	40	40	ns

- Low Power Dissipation
  - Active (max)
    - 95 mA / 80 mA (3.3V)
    - 85 mA / 70 mA (5.0V)
  - Standby Current: TTL Inputs (max)
    - 2.0 mA (SP version)
    - 1.0 mA (LP version)
  - Standby Current: CMOS Inputs (max)
    - 1.0 mA (SP version)
    - 0.15 mA (LP version)
- Fast Page Mode
- $\overline{RAS}$, $\overline{CAS}$ before $\overline{RAS}$, and Hidden Refreshing
- Self Refresh (LP version only)
- Packages: SOJ-26/24 (300mil)
  TSOP-26/24 (300mil)

Description

The IBM014440 is a Quad $\overline{CAS}$ fast-page dynamic RAM organized 1,048,576 words by 4 bits. Each of the four $\overline{CAS}$ pins uniquely controls the write operation to a corresponding I/O pin, much in the same manner as the write per bit function. This device was designed with memory parity systems in mind and can be a cost effective solution in that it replaces four 1M x 1 or two 2M x 2 DRAM devices. Other benefits include lower system power and reduced board space. This device is fabricated in IBM's 4M-bit Shrink 2 CMOS silicon gate technology. The circuits and process have been designed to provide high performance, low power dissipation, and high reliability. The devices operate with either a 5.0V ± 0.5V or 3.3V ± 0.3V power supply and are offered in a 26/24 pin 300mil TSOP or SOJ package. Refreshing may be accomplished by means of a $\overline{CAS}$ before $\overline{RAS}$ refresh cycle (CBR) that internally generates the refresh address, and is initiated by bringing any of the $\overline{CAS}$ pins low prior to $\overline{RAS}$ falling. Self-Refresh mode is entered by holding $\overline{RAS}$ low for ≥ 100µS during a CBR cycle. Detection of this long $\overline{RAS}$ time during a CBR cycle starts an internal oscillator that maintains data integrity without external clocking. Self-Refresh mode is included as a standard feature for Low Power devices (IBM014440M and IBM014440P). All low power devices support Extended Data Retention of 128ms, eight times (8x) the retention supported by IBM's standard power devices.

Pin Assignments



Pin Description

A0 - A9	Address Input
I/O0 - I/O3	Data Input/Output
$\overline{RAS}$	Row Address Strobe
$\overline{CAS0}$ - $\overline{CAS3}$	Column Address Strobe
$\overline{WE}$	Read/Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power (5.0V or 3.3V)
V_{SS}	Ground

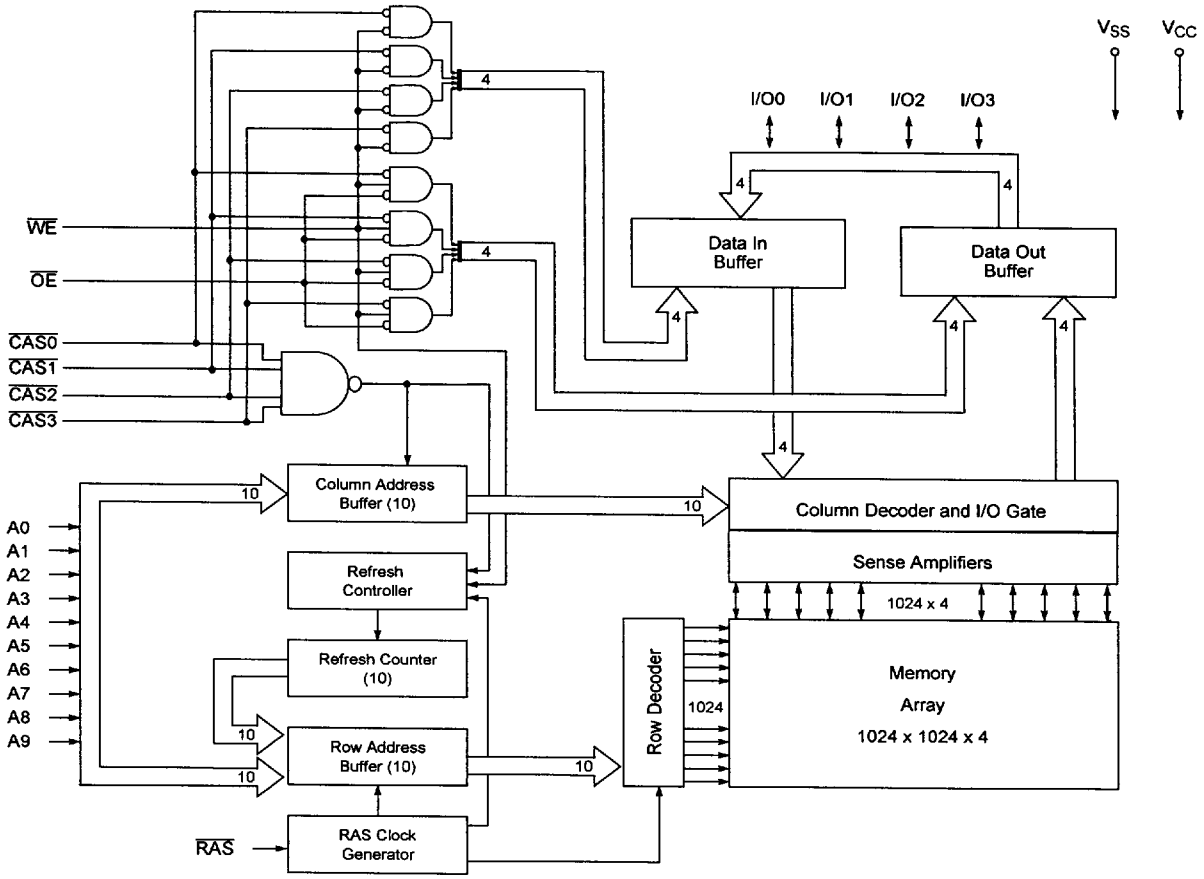
82F6673
SA14-4218-05
Revised 6/96

Ordering Information

Part Number	SP / LP	Self Refresh	Power Supply	Speed	Package	Notes
IBM014440J1 -60	SP	No	5.0V	60ns	300mil SOJ 26/24	1
IBM014440J1 -70	SP	No	5.0V	70ns	300mil SOJ 26/24	1
IBM014440MT1 -60	LP	Yes	5.0V	60ns	300mil TSOP 26/24	1
IBM014440MT1 -70	LP	Yes	5.0V	70ns	300mil TSOP 26/24	1
IBM014440PT1 -60	LP	Yes	3.3V	60ns	300mil TSOP 26/24	1
IBM014440PT1 -70	LP	Yes	3.3V	70ns	300mil TSOP 26/24	1

1. SP = Standard Power version (IBM014440); LP = Low Power version (IBM014440M and IBM014440P)

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$0-3	$\overline{WE}$	$\overline{OE}$	Row Address	Col. Address	I/O0 - I/O3
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col.	Data Out
Early-Write		L	L	L	X	Row	Col.	Data In
Delayed-Write		L	L	H→L	H	Row	Col.	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col.	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H→L	H	L	Row	Col.	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col.	Data Out
Fast Page Mode Write	1st Cycle	L	H→L	L	X	Row	Col.	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col.	Data In
Fast Page Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col.	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col.	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh Read		L→H→L	L	H	L	Row	Col.	Data Out
Self Refresh (LP version only)		H→L	L	L	H	X	X	X

Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt Device	5.0 Volt Device		
V_{CC}	Power Supply Voltage	-0.5 to +4.1	-1.0 to +6.0	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.1)	-0.5 to min (V_{CC}+0.5, 6.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.1)	-0.5 to min (V_{CC}+0.5, 6.0)	V	1
T_A	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	20	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Symbol	Parameter	5.0 Volt Devices			3.3 Volt Devices			Units	Notes
		Min.	Typ.	Max.	Min.	Typ.	Max.		
V_{CC}	Supply Voltage	4.5	5.0	5.5	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC} + 0.5	2.0	—	V_{CC} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}=0V.

Capacitance (T_A=25°C, f=1MHz)

Symbol	Parameter	Min.	Max	Units	Notes
C_{I1}	Input Capacitance (A0 - A9)	—	5	pF	1
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CASx}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	1
C_O	Output Capacitance (I/O0 - I/O3)	—	7	pF	1

1. Input capacitance measurements made with rise time shift method with $\overline{CAS}$ = V_{IH} to disable output.

DC Electrical Characteristics (T_A= 0 to +70 C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		3.3 Volt Device Min.	3.3 Volt Device Max.	5.0 Volt Device Min.	5.0 Volt Device Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$ and $\overline{CAS}$ Cycling: t_{RC} = t_{RC} min.)	-60	—	95	—	85	mA	1,2,3,4
		-70	—	80	—	70		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH} min)	SP version	—	2.0	—	2.0	mA	4
		LP version	—	1.0	—	1.0		
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥ V_{IH} min: t_{RC} = t_{RC} min)	-60	—	95	—	85	mA	1,3,4
		-70	—	80	—	70		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ ≤ V_{IL} min, $\overline{CAS}$ Cycling, t_{PC} = t_{PC} min)	-60	—	65	—	60	mA	1,2,3,4
		-70	—	65	—	60		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ ≥ V_{IH})	SP version	—	1	—	1	mA	7,8
		LP version	—	0.15	—	0.15		
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ before $\overline{RAS}$, t_{RC} = t_{RC} min)	-60	—	95	—	85	mA	1,3,4,5
		-70	—	80	—	70		
I_{CC7}	Self Refresh Current, LP version only Average Power Supply Current during Self Refresh (CBR cycle with $\overline{RAS}$ ≥ t_{RASS} (min))		—	170	—	170	µA	7,8
I_{CC8}	Battery Backup Refresh Current, LP version only Average Power Supply Current during Battery Backup refresh ($\overline{CAS}$ ≤V_{IL}, $\overline{WE}$ ≥V_{IH}, t_{RAS} ≤ 1µSec, t_{RC}=125µSec)		—	300	—	300	µA	7,8,9
I_{CC9}	Standby Current Standby current with Output's enabled ($\overline{RAS}$ ≥ V_{IH} (min) and $\overline{CAS}$ ≤ V_{IL} (max))		—	5	—	5	mA	4,6
$I_{I(L)}$	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 1.0V)) for 5.0V, or (0.0 ≤ V_{IN} ≤ (V_{CC} + 0.3V)) for 3.3V. All Other Pins Not Under Test = 0V		-10	+10	-10	+10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC} max)		-10	+10	-10	+10	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -5mA for 5.0V, or I_{OUT} = -2mA for 3.3V)		2.4	V_{CC}	2.4	V_{CC}	V	
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +4.2mA for 5.0V, or I_{OUT} = +2mA for 3.3V)		—	0.4	—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4} and I_{CC6} depend on cycle rate.
2. I_{CC1} and I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Column address can be changed once or less while $\overline{RAS}$ =V_{IL} and $\overline{CAS}$ =V_{IH}.
4. All I/O and other input pins must be ≤ V_{IL}(max) or ≥V_{IH}(min).
5. Enables on-chip refresh and address counters.
6. Assumes no resistive loads on I/O pins.
7. ((V_{CC}-0.2V ≤ V_{IH} ≤ V_{CC}+0.5V) and (0.0V ≤ V_{IL} ≤ 0.2V)) for 5.0V, or
   ((V_{CC}-0.2V ≤ V_{IH} ≤ V_{CC}+0.3V) and (0.0V ≤ V_{IL} ≤ 0.2V)) for 3.3V.
8. All other I/O and other inputs at V_{IH} or V_{IL}.
9. 1024 rows at 128µs = 128ms.

AC Characteristics (T_A=0 to +70°C)

1. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles or 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
5. If $\overline{OE}$ is tied permanently low, Late-Write or Read-Modify-Write operations are not possible.
6. If $\overline{CASx} \geq V_{IH}$(min), the data output (I/Ox) is in high impedance.

Read, Write, Read-Modify-Write and Ref. Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	110	—	130	—	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	1, 2
t_{RAS}	$\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	15	100K	18	100K	ns	3
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	4
t_{CAH}	Column Address Hold Time	10	—	10	—	ns	4
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	45	20	52	ns	4, 5
t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	ns	6
t_{RSH}	$\overline{RAS}$ Hold Time	15	—	18	—	ns	7
t_{CSH}	$\overline{CAS}$ Hold Time	60	—	70	—	ns	8
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	8
t_{CLCH}	Last $\overline{CAS}$ Going Low to First $\overline{CAS}$ to Return High	10	—	10	—	ns	9
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	10, 11, 12

1. Last rising $\overline{CASx}$ edge to first falling $\overline{CASx}$ edge.
2. If $\overline{CASx}$ is low at the falling edge of $\overline{RAS}$, the corresponding I/Ox output will be maintained from the previous cycle.
3. Each $\overline{CASx}$ must meet the minimum pulse width.
4. The first $\overline{CASx}$ edge to transition low.
5. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
6. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max) can be met. t_{RAD}(max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
7. Last $\overline{CASx}$ to go low.
8. The last $\overline{CASx}$ edge to transition high.
9. Last falling $\overline{CASx}$ edge to first rising $\overline{CASx}$ edge.
10. AC measurements assume t_T=5ns.
11. V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
12. In addition to meeting the transition rate specification, all input signals must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1, 2
t_{WCH}	Write Command Hold Time	10	—	15	—	ns	3, 4
t_{WP}	Write Command Pulse Width	10	—	15	—	ns	3
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	18	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	18	—	ns	5
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	6, 7
t_{DH}	D_{IN} Hold Time	12	—	15	—	ns	6, 7

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. t_{RWD}, t_{CWD}, and t_{AWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an Early Write cycle and the data I/O pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), the cycle is a Read-Modify-Write cycle and the data I/O pins will contain read data from the selected cells. If neither of the above sets of conditions are satisfied, the condition of the data I/O pins (at access time) is indeterminate.
2. The first $\overline{CASx}$ edge to transition low.
3. Parameter t_{WP} is applicable for a Delayed-Write cycle such as a Read-Write or Read-Modify-Write cycle. For Early-Write cycles, both t_{WCS} and t_{WCH} must be met.
4. Last $\overline{CASx}$ to go low.
5. The last $\overline{CASx}$ edge to transition high.
6. Output parameter (I/Ox) is referenced to corresponding $\overline{CAS}$ input; I/O0 by $\overline{CAS0}$, I/O1 by $\overline{CAS1}$, I/O2 by $\overline{CAS2}$, and I/O3 by $\overline{CAS3}$.
7. These parameters are referenced to the falling edge of $\overline{CAS}$ for Early-Write cycles and to the falling edge of $\overline{WE}$ for Delayed-Write or Read-Modify-Write cycles.

Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	145	—	175	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	80	—	90	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	35	—	40	—	ns	1, 2
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	50	—	55	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	15	—	15	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD} and t_{AWD} are not restrictive operating parameters. t_{RWD}, t_{CWD}, and t_{AWD} apply to Read-Modify-Write cycles. If $t_{WCS} \geq t_{WCS}$(min), the cycle is an Early Write cycle and the data I/O pins will remain open circuit (high impedance) throughout the entire cycle. If $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{AWD} \geq t_{AWD}$(min), the cycle is a Read-Modify-Write cycle and the data I/O pins will contain read data from the selected cells. If neither of the above sets of conditions are satisfied, the condition of the data I/O pins (at access time) is indeterminate.
2. The first $\overline{CASx}$ edge to transition low.
3. Late-Write and Read-Modify-Write cycles must have both t_{OEZ} and t_{OEH} satisfied ($\overline{OE}$ high during Write cycle) in order to insure that the output buffers will be in high impedance during the Write cycle. The data I/O pins will remain in high impedance until the next valid Read cycle.

Read Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	18	ns	2, 3, 4, 5
t_{AA}	Access Time from Address	—	30	—	35	ns	2, 5, 6
t_{OEA}	Access Time From $\overline{OE}$	—	15	—	18	ns	2, 7
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	8
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	9, 10
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	9
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	4
t_{OFF}	Output Buffer Turn-Off Delay From $\overline{CAS}$	0	15	0	15	ns	4, 11, 12
t_{OEZ}	Output Buffer Turn-Off Delay From $\overline{OE}$	0	15	0	15	ns	11, 12, 13

1. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, then t_{RAC} will exceed the value shown.
2. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
3. Assumes that $t_{RCD} \geq t_{RCD}(max)$ and $t_{RAD} \leq t_{RAD}(max)$.
4. Output parameter (I/Ox) is referenced to corresponding $\overline{CAS}$ input; I/O0 by $\overline{CAS0}$, I/O1 by $\overline{CAS1}$, I/O2 by $\overline{CAS2}$, and I/O3 by $\overline{CAS3}$.
5. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
6. Assumes that $t_{RCD} \leq t_{RCD}(max)$ and $t_{RAD} \geq t_{RAD}(max)$.
7. If $\overline{OE}$ is tied permanently low, Late-Write or Read-Modify-Write operations are not possible.
8. The first $\overline{CASx}$ edge to transition low.
9. Either t_{RCH} or t_{RRH} must be satisfied for a Read cycle.
10. The last $\overline{CASx}$ edge to transition high.
11. $t_{OFF}(max)$ and $t_{OEZ}(max)$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
12. The I/O pins go into high impedance during Read cycles once t_{OEZ} or t_{OFF} occurs. If $\overline{CASx}$ goes high first, $\overline{OE}$ becomes a "don't care". If $\overline{OE}$ goes HIGH and $\overline{CASx}$ stays low, $\overline{OE}$ is not a "don't care", and the I/Os will provide the previously read data if $\overline{OE}$ is taken back low (while $\overline{CASx}$ remains low).
13. All I/Os controlled, regardless of $\overline{CASx}$.

Fast Page Mode Read-Modify-Write Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{PRWC}	Fast Page Mode Read-Modify-Write Cycle Time	85	—	90	—	ns	1

1. Last rising $\overline{CASx}$ edge to next cycle's last rising $\overline{CASx}$ edge.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Unit	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Fast Page Mode Cycle Time	40	—	40	—	ns	1
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	2
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	3, 4

1. Last rising $\overline{CASx}$ edge to the next cycle's last rising $\overline{CASx}$ edge.
2. t_{RASP} defines t_{RAS} in fast page mode cycles.
3. Measured with a load circuit equivalent to 2 TTL loads and 100pF.
4. Output parameter (I/Ox) is referenced to corresponding $\overline{CAS}$ input; I/O0 by $\overline{CAS0}$, I/O1 by $\overline{CAS1}$, I/O2 by $\overline{CAS2}$, and I/O3 by $\overline{CAS3}$.

Refresh Cycle

Symbol	Parameter		-60		-70		Unit	Notes
			Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		10	—	10	—	ns	1, 2
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		10	—	10	—	ns	1, 3
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh)		10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time		0	—	0	—	ns	
t_{REF}	Refresh period	SP version	—	16	—	16	ms	4
		LP version	—	128	—	128		

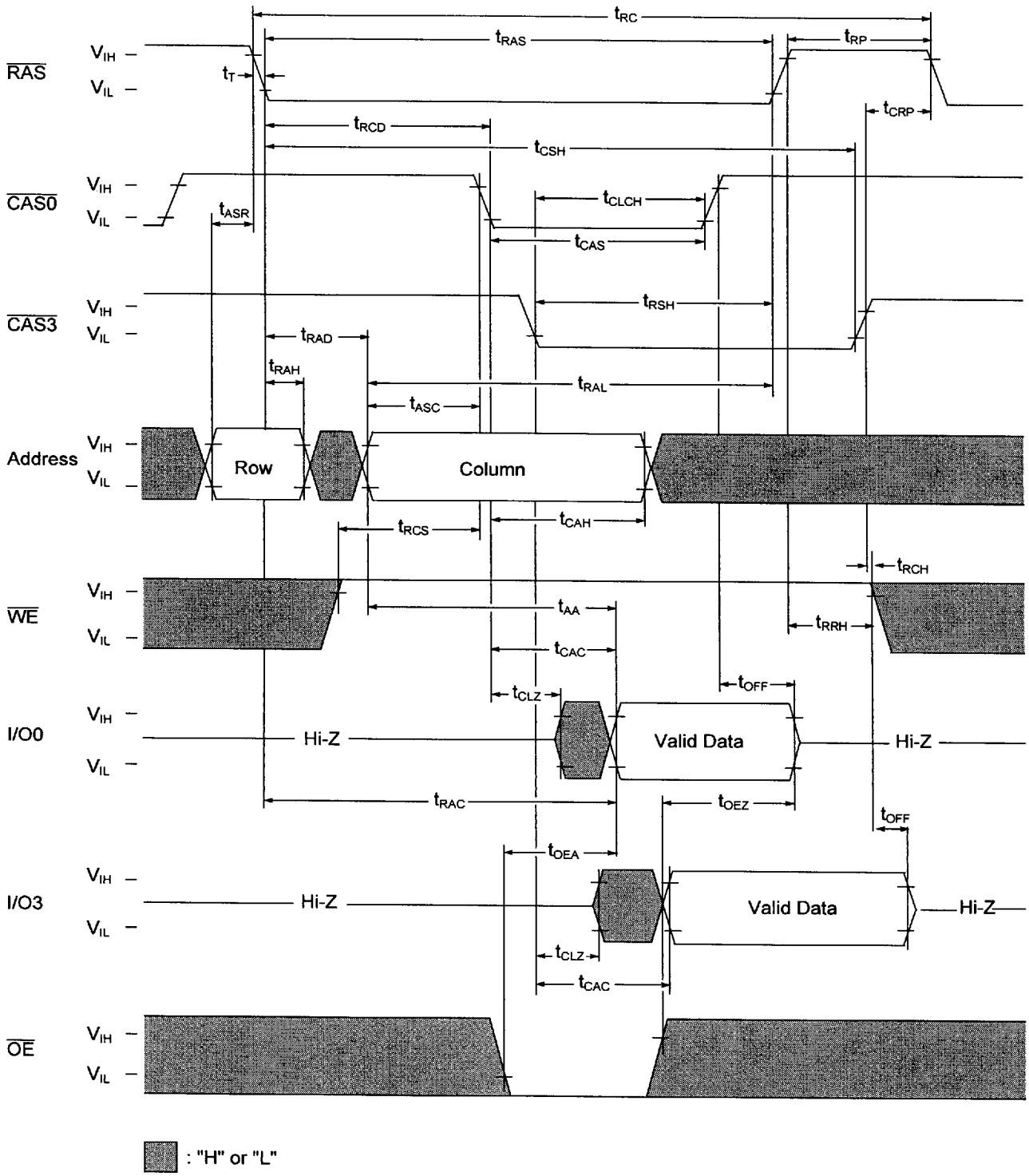
1. Enables on-chip refresh and address counters.
2. The first $\overline{CASx}$ edge to transition low.
3. The last CASx edge to transition high.
4. 1024 cycles.

Self Refresh Cycle - Low Power version only

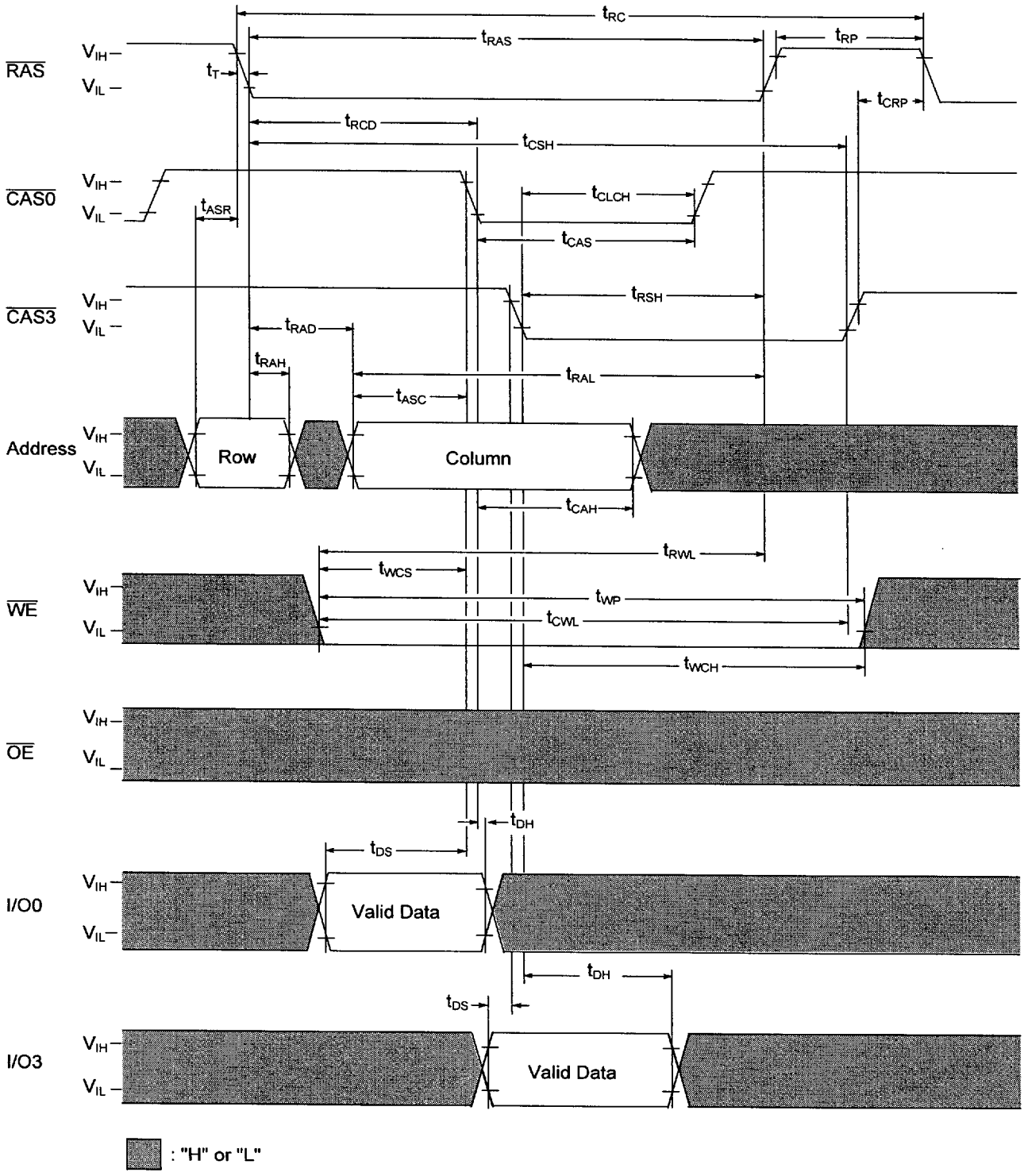
Symbol	Parameter	-60		-70		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width (Self Refresh)	100	—	100	—	µs	1,2
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	110	—	130	—	ns	1
t_{CHD}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	10	—	10	—	ns	1

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in a ROR manner over the refresh interval, then a full burst of all row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh. If row addresses are being refreshed in a CBR-Burst manner over the refresh interval (i.e. burst of 8), then upon exiting from Self Refresh the user must conform to whatever refresh (i.e. burst of 8) method that was being used prior to entering Self Refresh.
2. I/O pins will go into high impedance after 100µs.

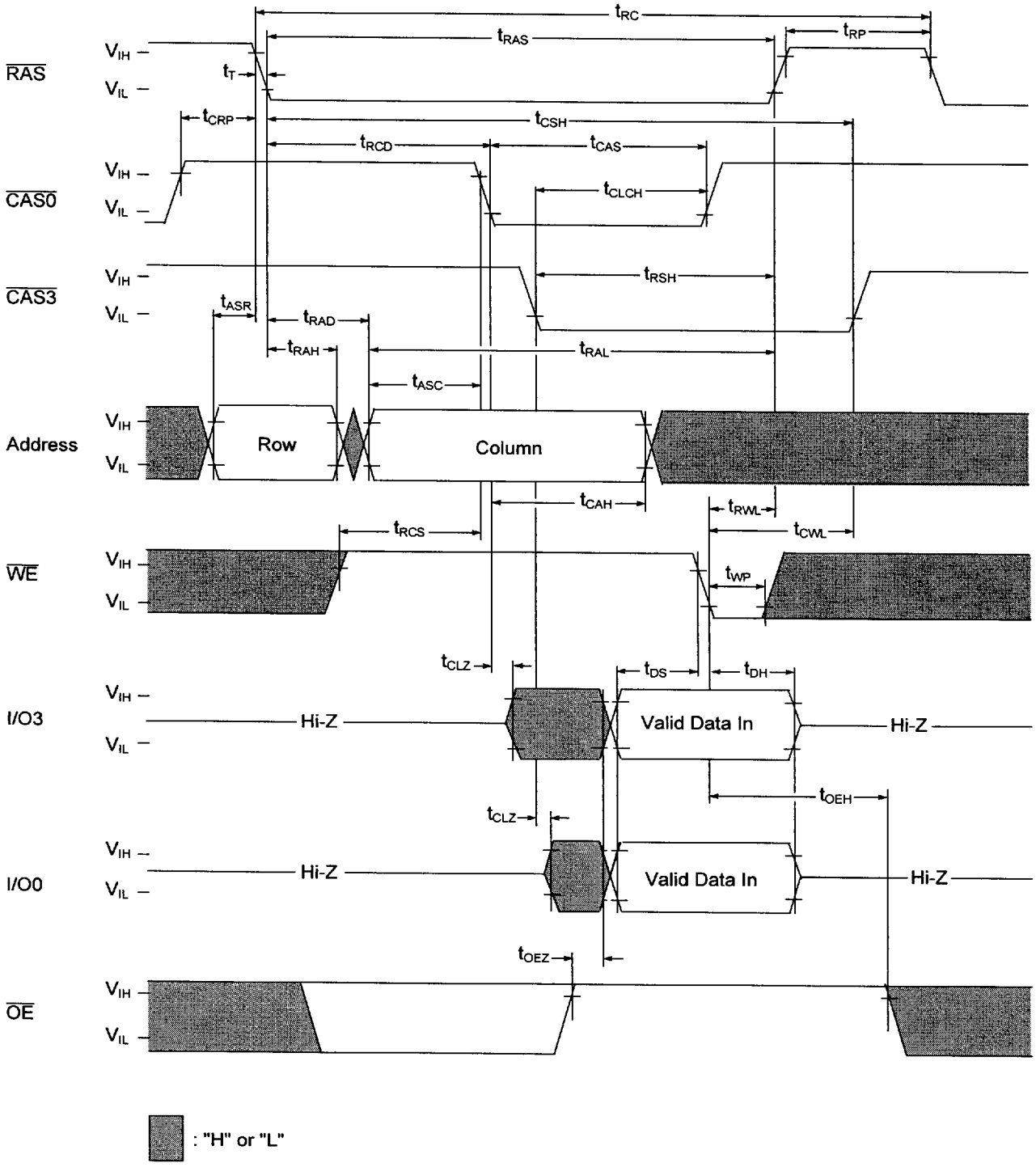
Read Cycle



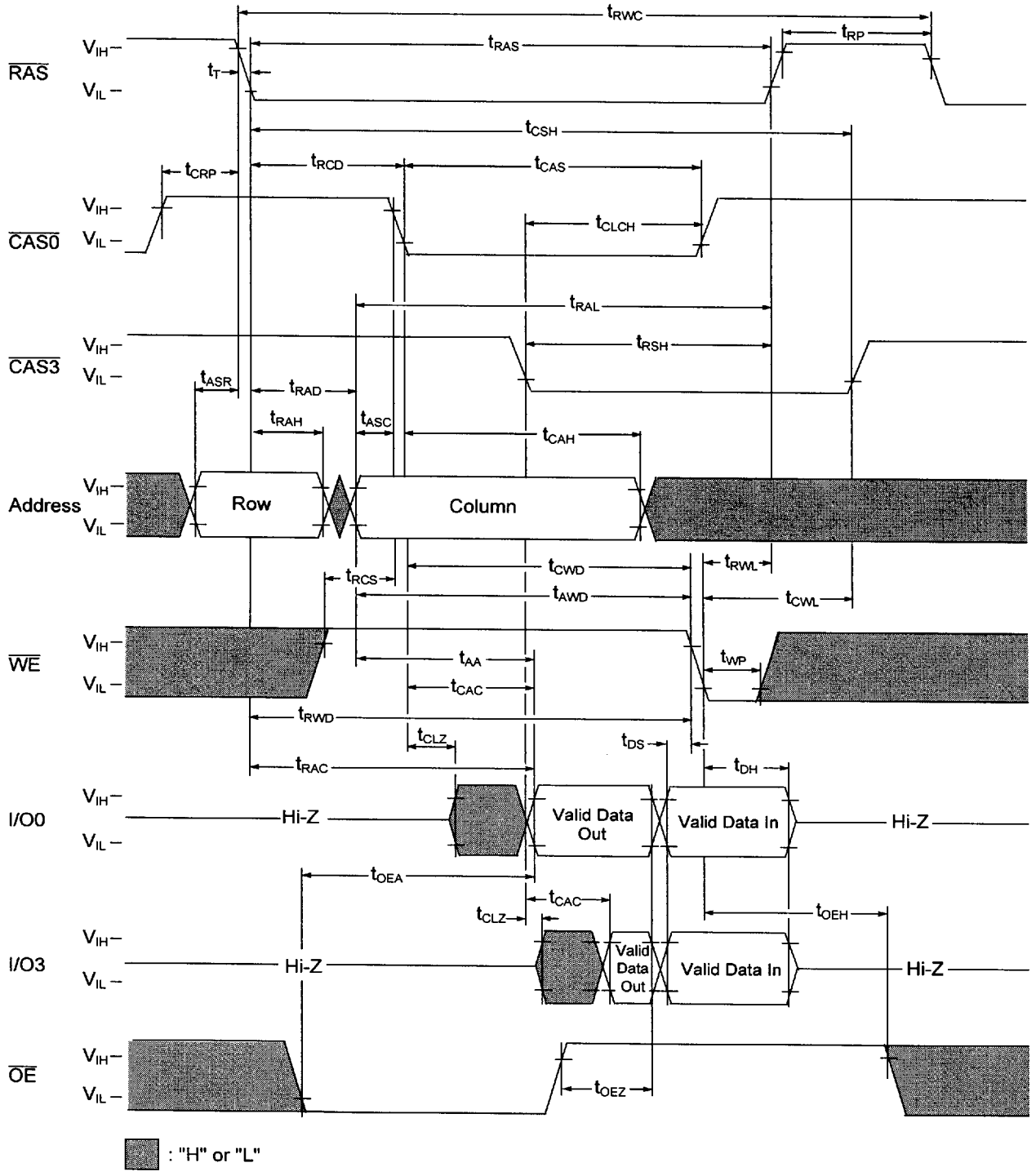
Write Cycle (Early Write)



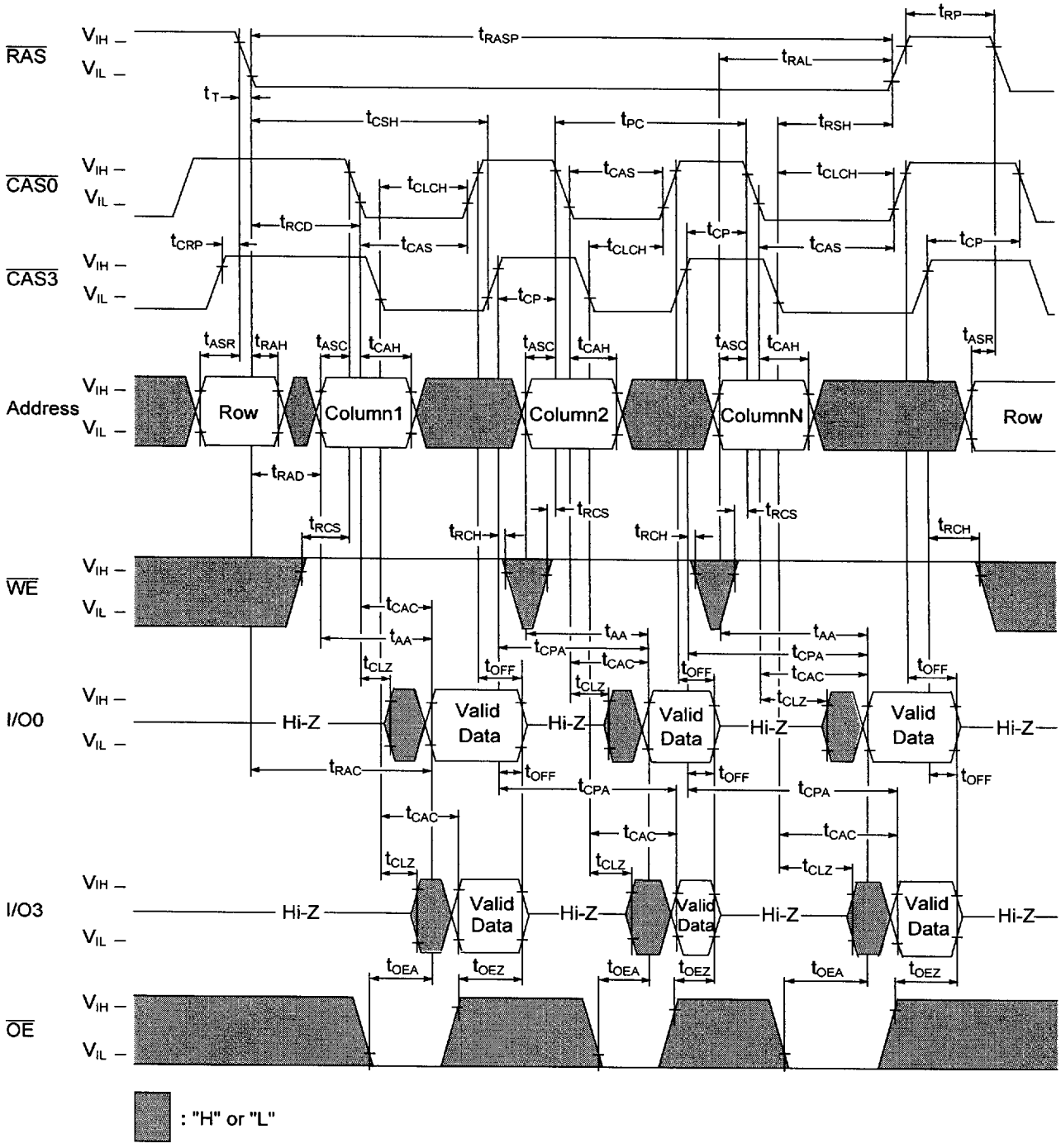
Write Cycle (Delayed Write)



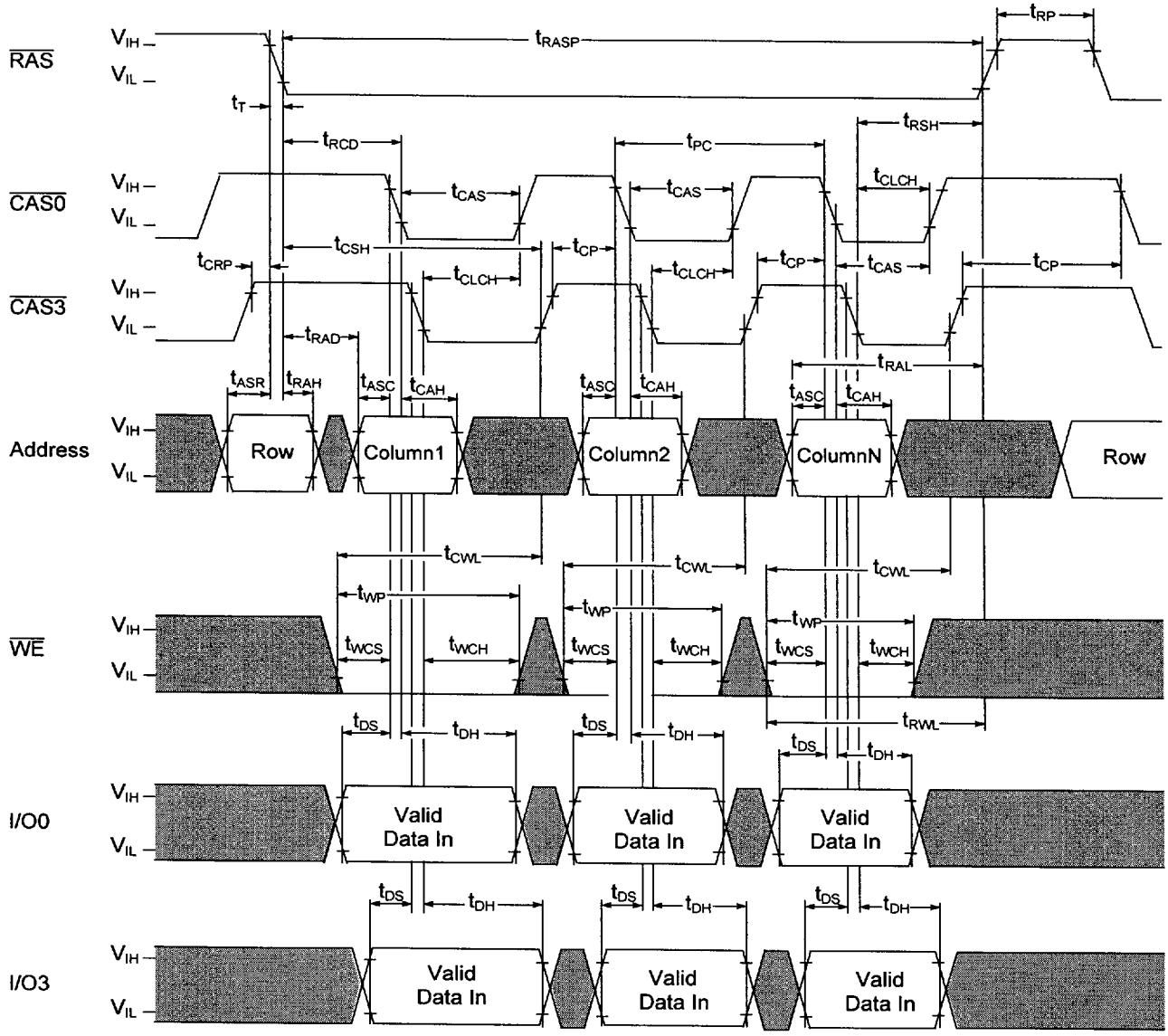
Read-Modify-Write Cycle



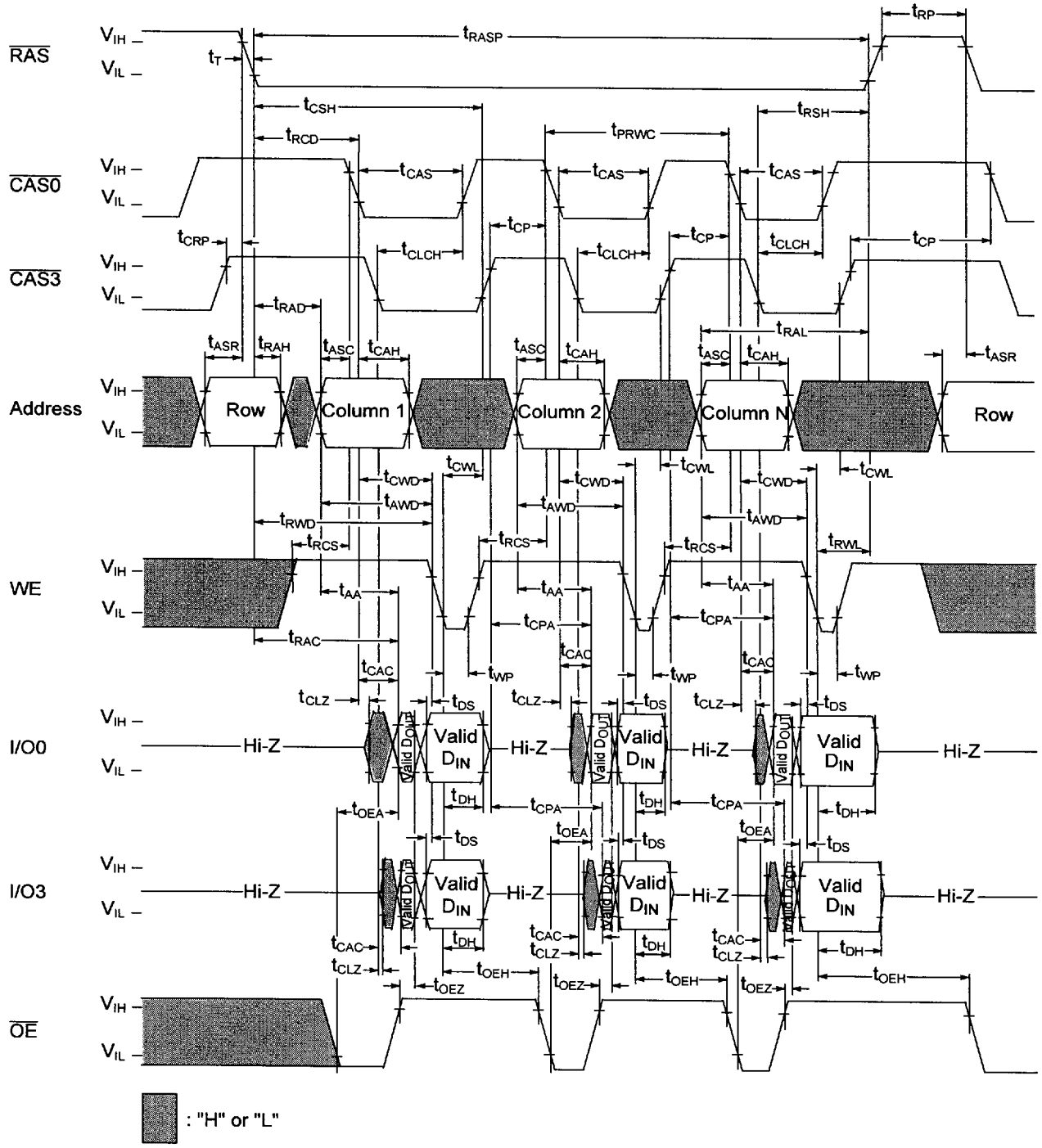
Fast Page Mode Read Cycle



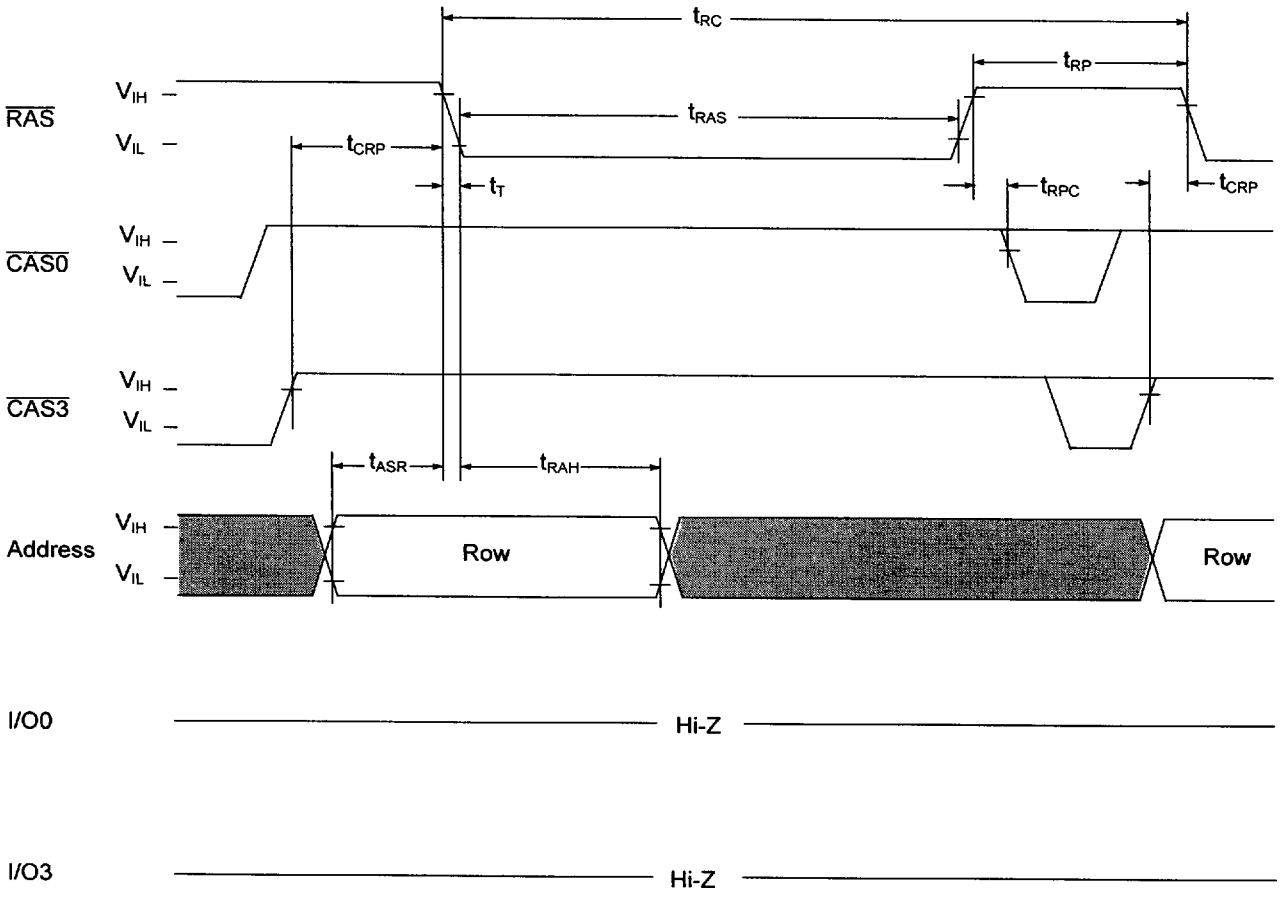
Fast Page Mode Write Cycle



Fast Page Mode Read-Modify-Write Cycle



$\overline{RAS}$ Only Refresh Cycle



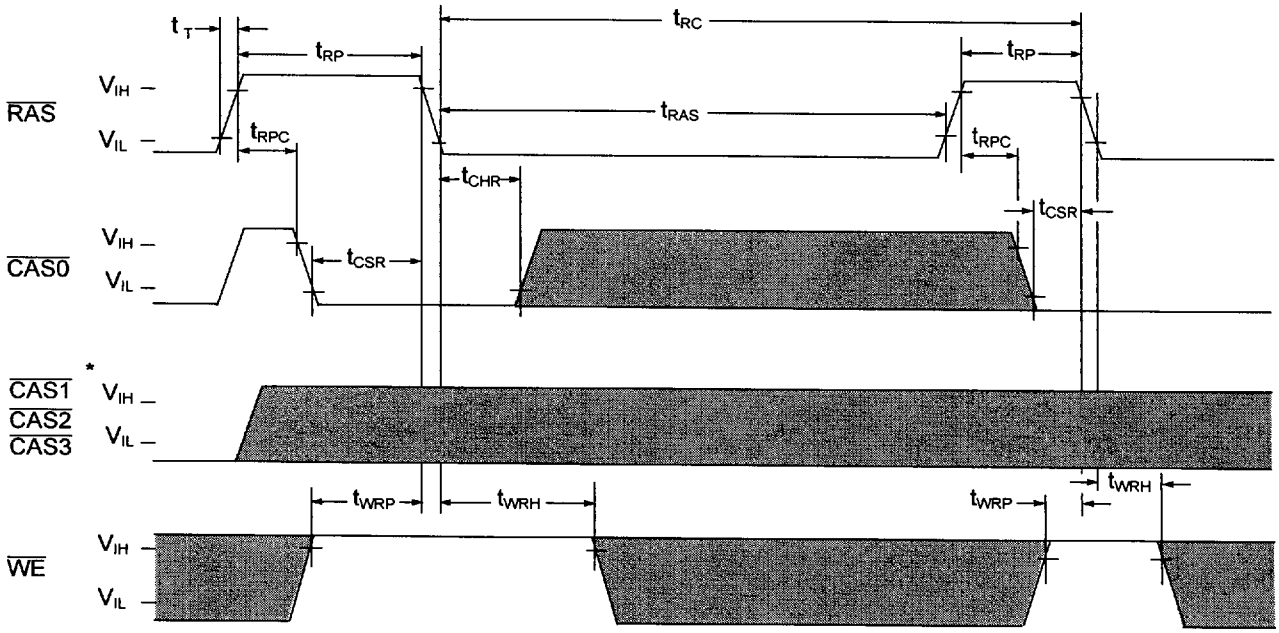
$\overline{WE}$ = DON'T CARE

$\overline{OE}$ = DON'T CARE

: "H" or "L"

REFRESH ADDRESS FIELD = A0-A9

$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



I/O0 — Hi-Z

I/O3 — Hi-Z

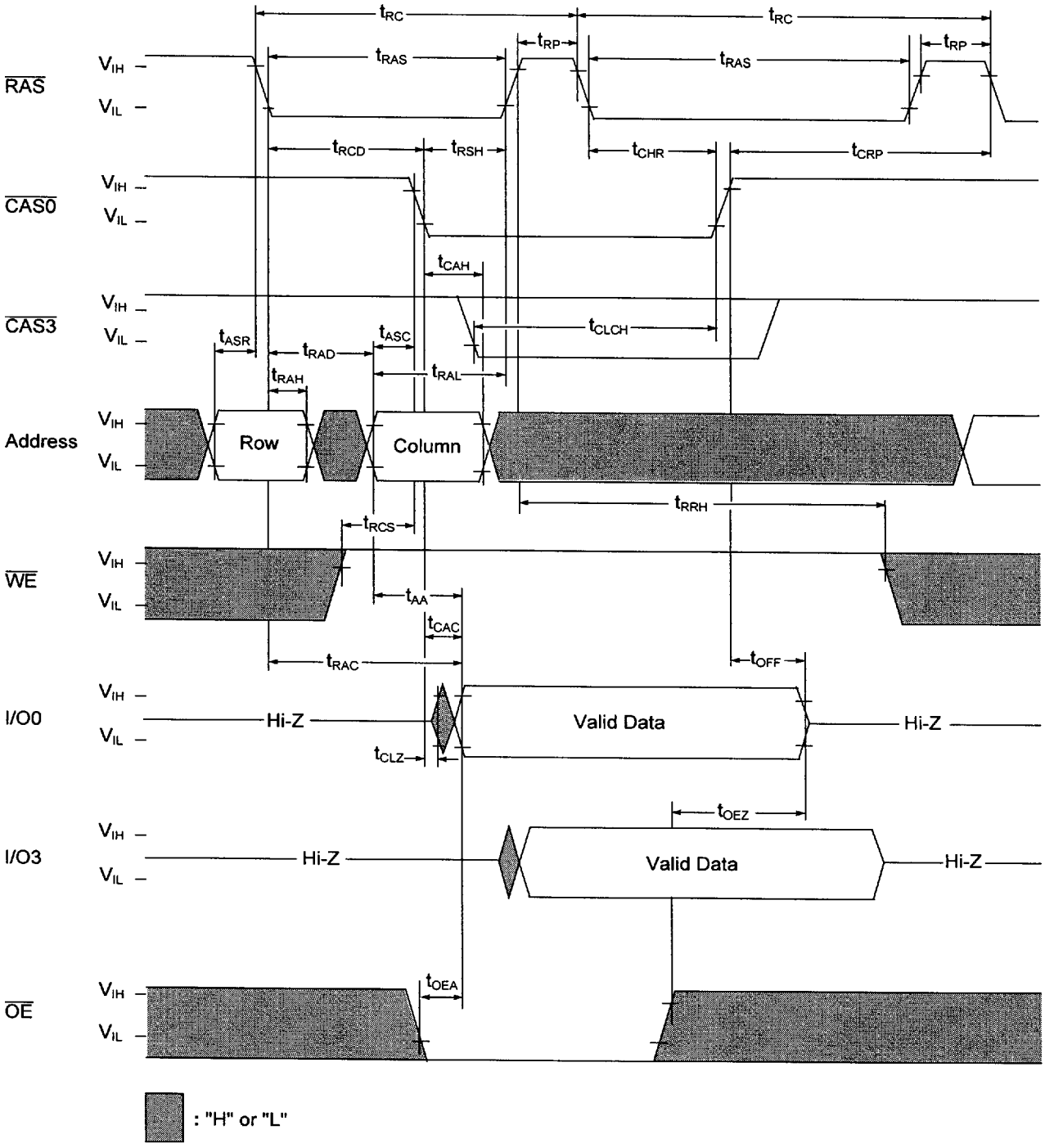
A0-A9 = DON'T CARE

$\overline{OE}$ = DON'T CARE

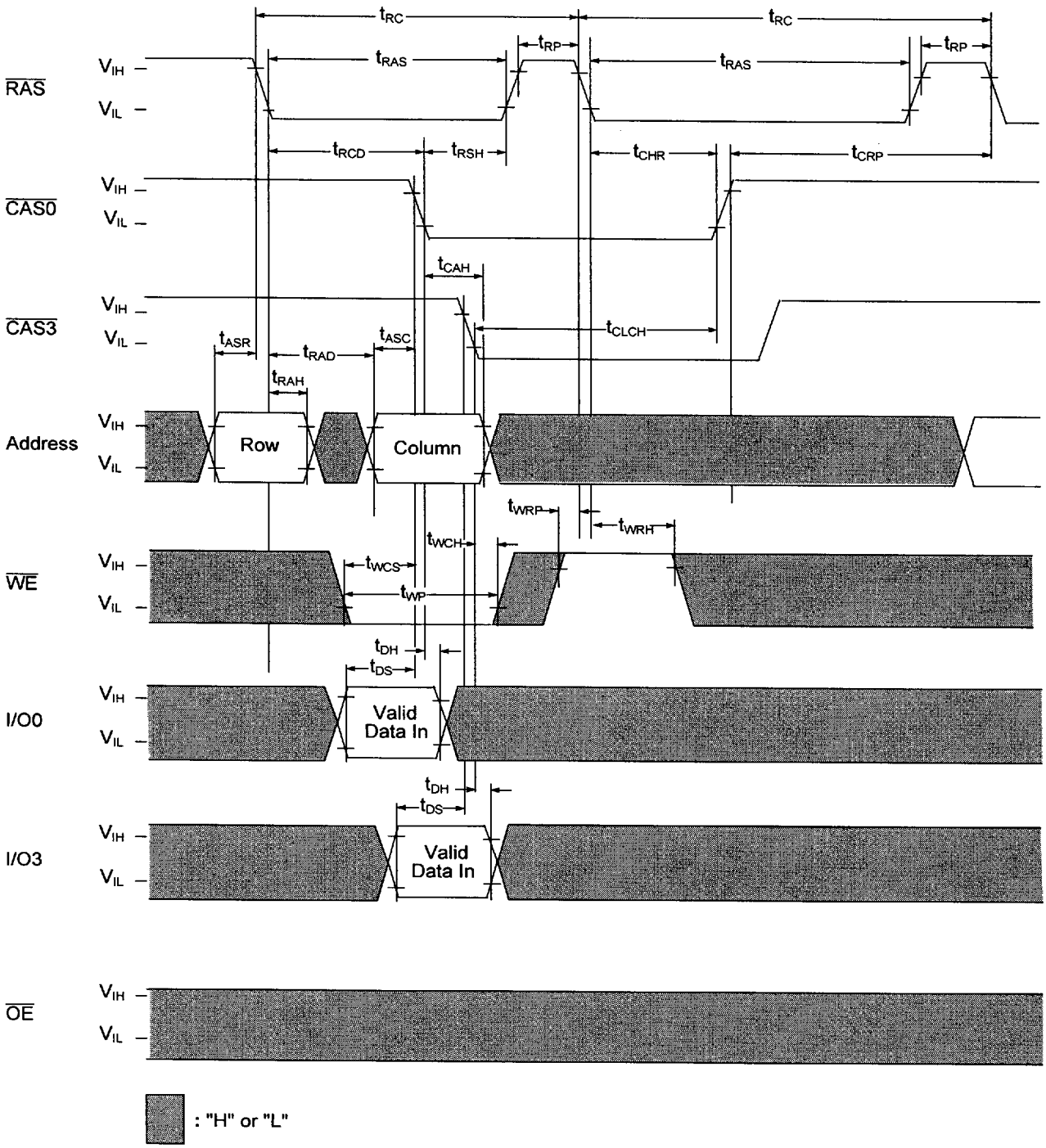
: "H" or "L"

*Any one $\overline{CAS}$ ($\overline{CAS0}$,$\overline{CAS1}$,$\overline{CAS2}$, or $\overline{CAS3}$) can initiate a CBR cycle.

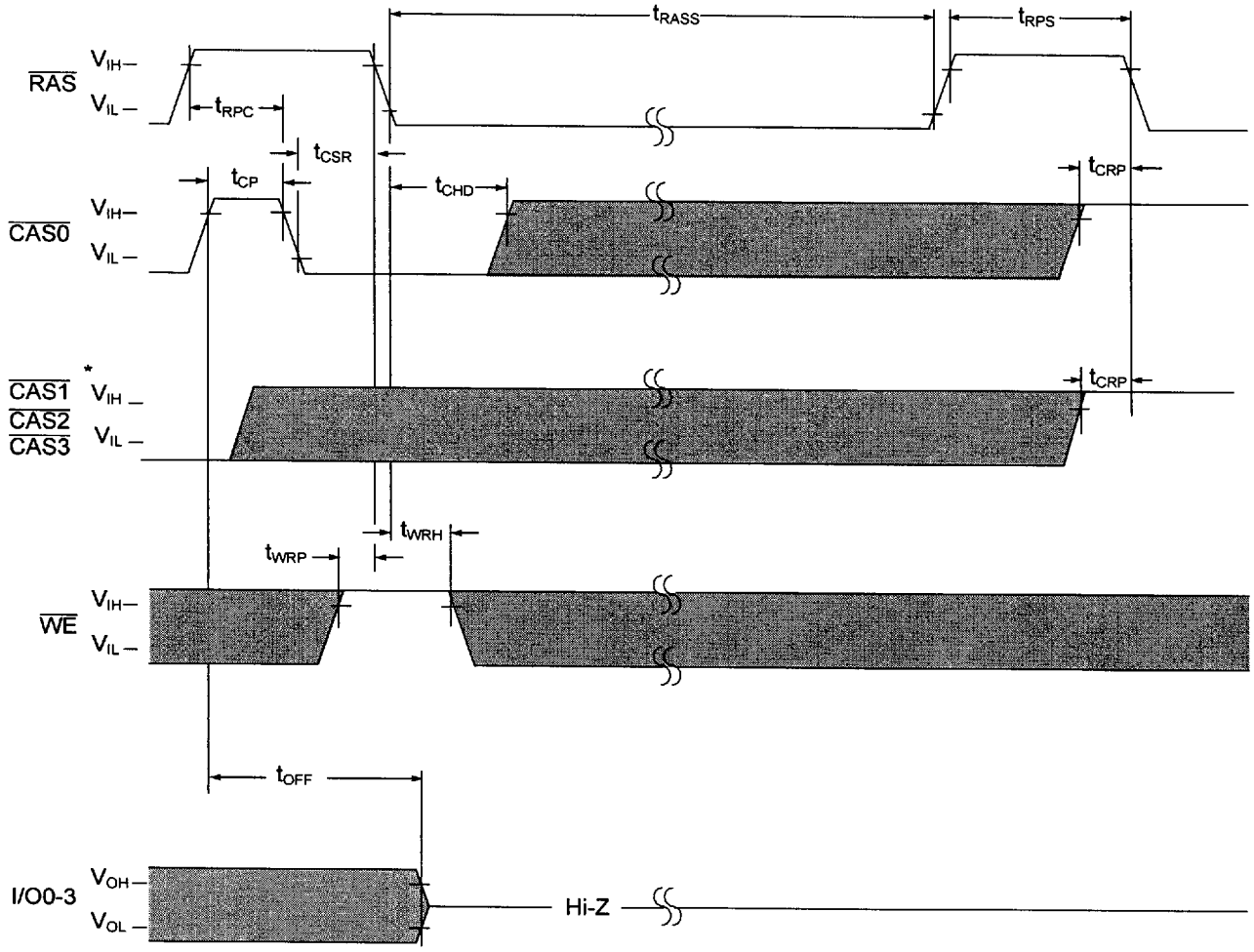
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode) - Low Power version only

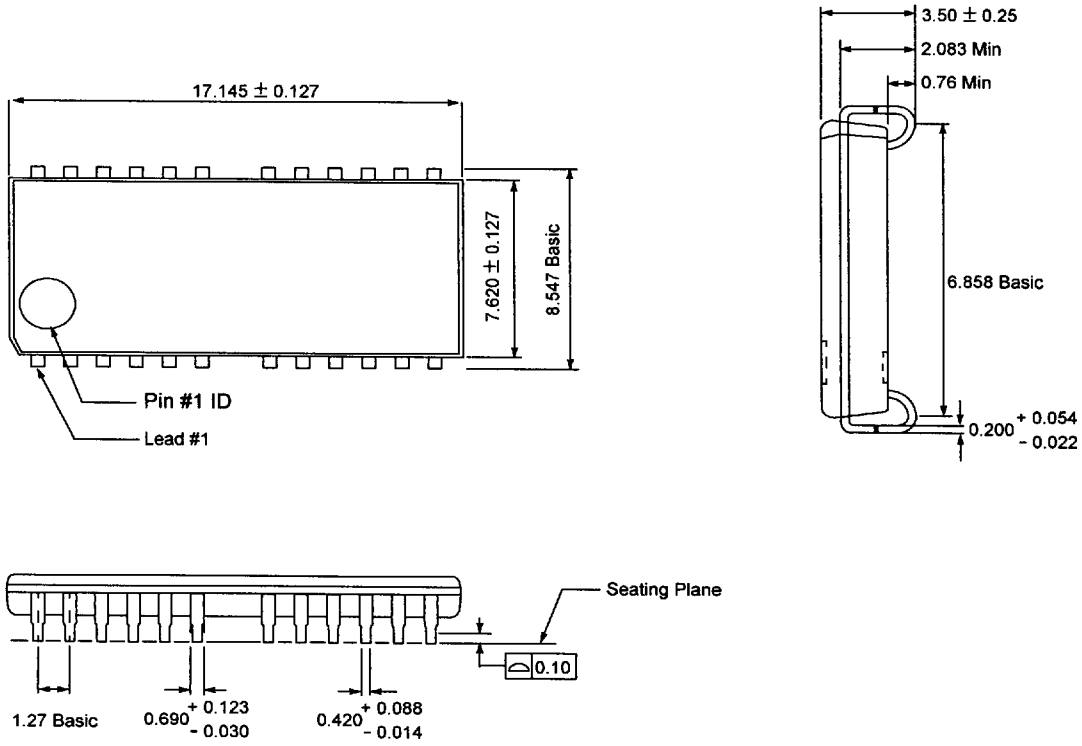


: "H" or "L"

*Any one $\overline{CAS}$ ($\overline{CAS0}$,$\overline{CAS1}$,$\overline{CAS2}$, or $\overline{CAS3}$) can initiate a Self Refresh cycle.

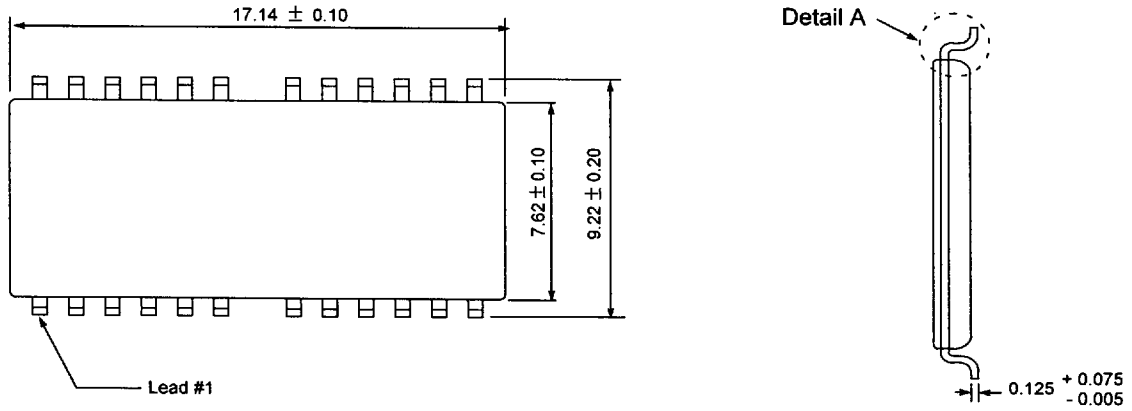
NOTE: Address and OE are "H" or "L"
Once $\overline{RAS}$ (min) is provided and $\overline{RAS}$ remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

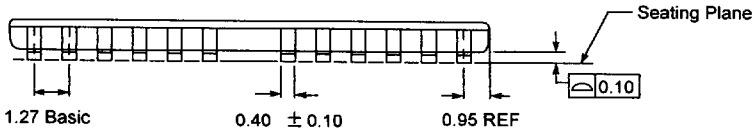
Package Dimensions (300 mil; 26/24 lead; Small Outline J-Lead)

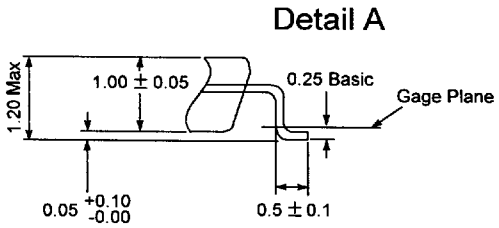


NOTE: All dimensions are in millimeters; Packages diagrams are not drawn to scale.

Package Dimensions (300 mil; 26/24 lead; Thin Small Outline Package)







NOTE: All dimensions are in millimeters; Package diagrams are not drawn to scale.

Revision Log

Revision	Contents of Modification
01/05/95	Initial Release
1/17/95	1. t_{RPC}, t_{CSR}, t_{CHR} removed from $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle timing diagram (end of cycle only). t_{CLCH} removed from timing. $\overline{CAS0}$ changed to $\overline{CASW}$ and specified as "Don't Care" after t_{CHR}. $\overline{CAS3}$ changed to $\overline{CASX,Y,Z}$ and specified as "Don't Care". t_{CRP} added to $\overline{CAS}$ timings.
12/10/95	1. Packaging diagram updated. 2. Low Power with Self Refresh option was added to the spec. along with the Low Power retention time and Standby currents. 3. Truth Table was added. 4. V_{IN} and V_{OUT} were added to the Absolute Maximum Ratings table. 5. t_{CAH} was changed from 15ns to 10ns for the -70 speed sort. 6. t_{DH} was reduced from 15ns to 12ns for the -60 speed sort. 7. t_{CHS} was removed from the Self Refresh Cycle. 8. t_{CHD} was added to the Self Refresh Cycle with a value of 10ns for all speed sorts. 9. The Self Refresh timing diagram was changed to allow $\overline{CAS}$ to go high t_{CHD} (10ns) after $\overline{RAS}$ falls entering a Self Refresh. 10. The CBR timing diagram was changed to allow $\overline{CAS}$ to remain low for back-to-back CBR cycles.
5/06/96	1. Corrected Read Cycle timing diagram. 2. Corrected package information in "Features" section.
6/13/96	1. Add Die Revision G part numbers. 2. Add Hidden Refresh (Write) timing diagram. 3. Corrected $\overline{CAS}$ naming convention in CBR/Self Refresh timing diagram.