256K X 16 DRAM

Features

- 256K x 16 DRAM
- Performance:

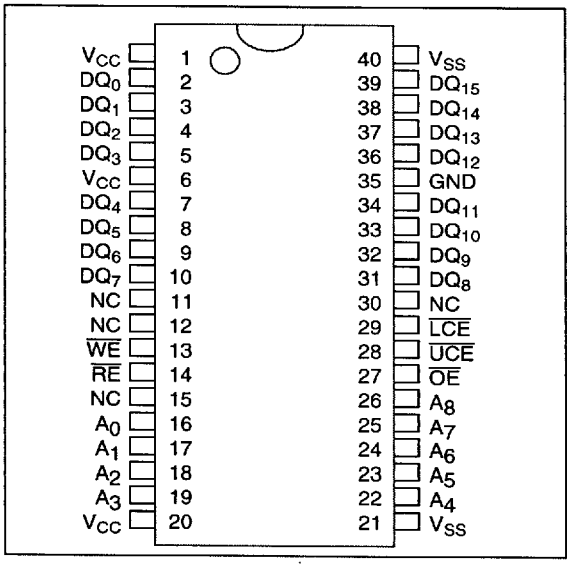
Parameter		-40	-50	-60
t_{RP}	$\overline{RE}$ Precharge	20ns	25ns	30ns
t_{CAC}	Access Time from $\overline{CE}$	12ns	14ns	15ns
t_{AA}	Column Address Access Time	20ns	25ns	30ns
t_{RC}	Read or Write Cycle Time	75ns	90ns	110ns
t_{PC}	Fast Page Mode Cycle Time	20ns	25ns	30ns
t_{HPC}	Extended Data Out Cycle Time	15ns	20ns	25ns

- 66MHz EDO performance
- Non-Persistent WPBM mode
- Power Supply: 5.0V ± 0.5V and 3.3V ± 0.3V
- High Performance, CMOS 0.45µm process
- SOJ-40 JEDEC Standard
- TTL compatible

Description

This 4Mb DRAM is organized as 256K x 16. The parts are available in three speed sorts:40, 50and 60ns. Fast page (FP) as well as Extended Data Out (EDO) devices are available in 5V and 3.3V. The 40ns parts have an EDO performance of 66MHz which can improve performance of graphics applications. Refresh may be accomplished by a $\overline{CE}$ before $\overline{RE}$ refresh cycle (CBR) that internally generates the refresh address. $\overline{RE}$ - only refresh cycles will also refresh all memory locations. However, $\overline{RE}$ - only refresh requires row address to be provided externally. CBR cycles are required to clear any modes that might be inadvertently set during power up.

Pin Assignments (Top View)



Pin Description

$\overline{RE}$	Row Enable
$\overline{LCE}$, $\overline{UCE}$	Lower & Upper Column Enable
$\overline{W}$	Write
$\overline{OE}$	Output Enable
A_8-A_0	Address Inputs
DQ_{15} - DQ_0	Random Port Data Input/Output
V_{CC}	Voltage (5.0V ± 0.5V or 3.3V ± 0.3V). All voltages are referenced to the nearest V_{SS} pin.
V_{SS}	Ground. V_{SS}=0V
NC	No Connect

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Detailed Pin Description

$\overline{RE}$ - Row Enable; also known as $\overline{RAS}$

This pin is functionally equivalent to a chip enable signal in that whenever it is activated, 8192 storage cells of the selected row are sensed simultaneously and the sense amplifiers restore all data. The falling edge of $\overline{RE}$ latches data on address pins A_0 -A_8. $\overline{CE}$, $\overline{OE}$, and $\overline{W}$ are simultaneously latched to invoke the DRAM port operations.

$\overline{LCE}$, $\overline{UCE}$ - Lower and Upper Column Enable (Dual $\overline{CE}$ parts only).

These pins enable lower and upper byte respectively of the selected column for Read/Write. The falling edge of either $\overline{LCE}$ or $\overline{UCE}$ latches the column address.

$\overline{W}$ - Write

This pin enables the DRAM port write circuitry.

$\overline{OE}$ - Output Enable

This pin enables the DRAM data outputs.

A_0 - A_8 - Address Inputs

These pins are multiplexed as row and column address inputs. Row addresses are first used to select one of the possible 512 rows for a Read, Write, or Refresh cycles. Column addresses are then supplied to select one of the possible 512 columns for a Read or a Write cycle.

DQ_0 - DQ_{15} - Random Port Data Input/Output

In a Read cycle, these pins serve as outputs for the selected storage cells. In a Write cycle, data input on these pins is latched by the falling edge of $\overline{CE}$ or $\overline{W}$ whichever occurs later. Data will not appear at the outputs until after both $\overline{CE}$ and $\overline{OE}$ have been brought low. At $\overline{RE}$ falling edge, the data input at these pins can be used for loading the Write-per-Bit Mask (WPBM).

V_{cc} - (5.0V $\pm$ 0.5V) or (3.3V $\pm$ 0.3V) voltage.

All voltages are referenced to the nearest V_{ss} pin.

V_{ss} - Circuit ground. V_{ss} = 0V.

NC - No Connect.

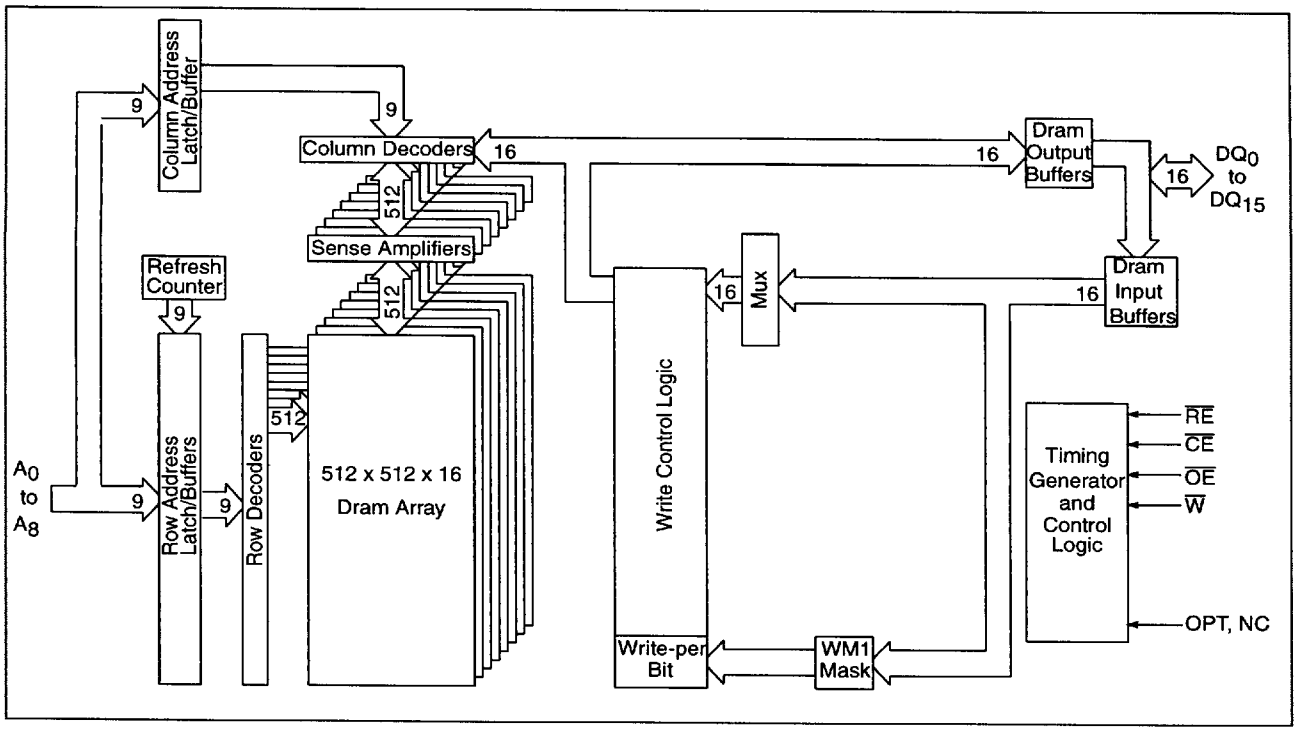
NC implies that the pin(s) should not be grounded or connected to any other signal. These pins might be used for testing some modes at factory. Consult factory before using any one of NC pins.

Ordering Information

Part Number	Features	Voltage	Speed	Package	Notes
IBM 015160LJ3A-40	Dual $\overline{CE}$, Fast Page	5.0V	40ns	SOJ-40 400 mil	1
IBM 015160NJ3A-40	Dual $\overline{CE}$, Fast Page	3.0V	40ns		1
IBM 015161LJ3A-40	Dual $\overline{CE}$, EDO Page	5.0V	40ns		1
IBM 015161NJ3A-40	Dual $\overline{CE}$, EDO Page	3.0V	40ns		1
IBM 015160LJ3A-50	Dual $\overline{CE}$, Fast Page	5.0V	50ns		
IBM 015160NJ3A-50	Dual $\overline{CE}$, Fast Page	3.0V	50ns		
IBM 015161LJ3A-50	Dual $\overline{CE}$, EDO Page	5.0V	50ns		
IBM 015161NJ3A-50	Dual $\overline{CE}$, EDO Page	3.0V	50ns		
IBM 015160LJ3A-60	Dual $\overline{CE}$, Fast Page	5.0V	60ns		
IBM 015160NJ3A-60	Dual $\overline{CE}$, Fast Page	3.0V	60ns		
IBM 015161LJ3A-60	Dual $\overline{CE}$, EDO Page	5.0V	60ns		
IBM 015161NJ3A-60	Dual $\overline{CE}$, EDO Page	3.0V	60ns		

1. --40parts are high performance parts with an EDO performance of 66MHz.

Block Diagram



Truth Table

Function	$\overline{RE}$	$\overline{LCE}$	$\overline{UCE}$	$\overline{WE}$	$\overline{OE}$	Address t_R	Address t_C	DQs DQ_{0-7}	DQs DQ_{8-15}	Notes
Standby	H	X	X	X	X	X	X	High-Z	High-Z	
Row Refresh Only	L	H	H	X	X	Row	-	High-Z	High-Z	
$\overline{CE}$-before-$\overline{RE}$	L	L	L	H	X	X	X	High-Z	High-Z	2
Lower Byte Read	L	L	H	H	L	Row	Col.	Output	High-Z	
Upper Byte Read	L	H	L	H	L	Row	Col.	High-Z	Output	
Word Read Cycle	L	L	L	H	L	Row	Col.	Output	Output	
Lower Byte Write	L	L	H	L	H	Row	Col.	Input	High-Z	1
Upper Byte Write	L	H	L	L	H	Row	Col.	High-Z	Input	1
Word Write Cycle	L	L	L	L	H	Row	Col.	Input	Input	1

1. Write of the input data will be dependent on the mask provided at $\overline{RE}$ fall time. If $\overline{WE}$ is high at $\overline{RE}$ fall time, no mask will be applied to the data input. However, if $\overline{WE}$ is low at $\overline{RE}$ fall time, DQs latched at $\overline{RE}$ fall time acts as Write-per-Bit (WPB)mask for the input data provided at $\overline{CE}$ fall time for page cycles for the whole $\overline{RAS}$ cycle.
2. Truth table for $\overline{CE}$ before $\overline{RE}$ (CBR) is slightly different than Micron, NEC etc.

Absolute Maximum Ratings

Symbol	Item	Rating 5.0 Volt	Rating 3.3 Volt	Units	Notes
V_{CC}	Power Supply Voltage	-1.0 to +6.0	-0.5 to +4.6	V	1
T_A	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	1.0	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to +70°C)

Symbol	Parameter	5.0 Volt Min.	5.0 Volt Typ.	5.0 Volt Max.	3.3 Volt Min.	3.3 Volt Typ.	3.3 Volt Max.	Units	Notes
V_{CC}	Supply Voltage	4.5	5.0	5.5	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.4	—	V_{CC}+0.5	2.0	—	V_{CC}+0.3	V	1
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f= 1.0 MHz)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (Addresses)	—	5	pF	
C_{I2}	$\overline{RE}$, $\overline{CE}$, $\overline{W}$, $\overline{OE}$	—	7	pF	
C_O	Output Capacitance (DQ_i)	—	7	pF	

Output Drivers

Driver	Impedance	Output Voltage, Low (Max)	Output Voltage, High (Min)
Parallel Port	45±15 Ω	I_{OUT}=2.0 mA, V=0.4	I_{OUT}=-1 mA, V=2.4

AC Measurement Conditions

Port	Detect	Load
Parallel Port Output Detect Level	2.0V / 0.8V	—
Parallel Port Output Load	—	1 TTL + 50pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC}= 3.3V ± 0.3V or V_{CC}= 5.0V ± 0.5V)

Symbol	Parameter		5.0 Volt		3.3 Volt		Units	Notes
			Min.	Max.	Min.	Max.		
I_{CC1}	Operating Current (Random) Average Power Supply Operating Current ($\overline{RE}$ and $\overline{CE}$ Cycling, t_{RC} =90ns for -40and -50, t_{RC} =110ns for -60ns)	-40	—	135	—	135	mA	1,2,3,5
		-50	—	135	—	135		
		-60	—	130	—	130		
I_{CC2}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RE}$ = V_{IL} Min., $\overline{CE}$ Cycling, t_{PC} = 20ns for -40and -50, t_{PC}=25ns for -60)	-40	—	80	—	80	mA	1,2,4,5
		-50	—	80	—	80		
		-60	—	70	—	70		
I_{CC3}	Standby Supply Current Power Supply Standby Current ($\overline{RE}$ = $\overline{CE}$ = V_{CC})		—	1	—	1	mA	
$I_{I(L)}$	Input Leakage Current, any input (0.0 ≤ V_{IN} ≤ (V_{CC} + 1.0V)), All Other Pins Not Under Test = 0V		-10	+10	-10	10	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≤ V_{OUT} ≤ V_{CC}(max))		-10	+10	-10	10	µA	
V_{OH}	Output Level (TTL) Output "H" Level Voltage (I_{OUT} = -1mA, Random)		2.4	—	2.4	—	V	4
V_{OL}	Output Level (TTL) Output "L" Level Voltage (I_{OUT} = +2.0mA, Random)		—	0.4	—	0.4	V	4

1. I_{CC1}, I_{CC2}, and I_{CC3} depend on cycle rate.
2. I_{CC1}, I_{CC2}, and I_{CC3} depend on output loading. Specified values are obtained with the output open.
3. Measured with one address change per $\overline{RE}$ cycle.
4. Measured with one column address change per page cycle.
5. Measured with $\overline{OE}$ = V_{IH} when $\overline{CE}$ = V_{IL}.

AC Characteristics (T_A= 0 to +70°C)

Read, Write, Read-Modify-Write and Refresh. Cycles (Common Parameters)

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ASC}	Column address setup time	0	—	0	—	0	—	ns	
t_{ASR}	Row address setup time	0	—	0	—	0	—	ns	
t_{AR}	Column address hold time after $\overline{RE}$ low	20	—	20	—	20	—	ns	
t_{CAH}	Column address hold time after $\overline{CE}$ low	5	—	7	—	10	—	ns	5
t_{CAS}	$\overline{CE}$ pulse width	8	16K	10	16K	15	16K	ns	
t_{CHCL}	First $\overline{CE}$ to return high to last $\overline{CE}$ going low	6	—	6	—	6	—	ns	
t_{CLCH}	Last $\overline{CE}$ going low to first $\overline{CE}$ to return high	6	—	6	—	6	—	ns	
t_{CP}	$\overline{CE}$ precharge time	5	—	7	—	10	—	ns	
t_{CRP}	$\overline{CE}$ high before $\overline{RE}$ low precharge	10	—	12	—	15	—	ns	8
t_{CSH}	$\overline{CE}$ hold time	40	—	50	—	60	—	ns	
t_{MH}	Write mask hold time after $\overline{RE}$ low	5	—	7	—	10	—	ns	
t_{MS}	Data-in setup before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{RAD}	$\overline{RE}$ to column address delay time	12	20	14	25	15	30	ns	4
t_{RAH}	Row address hold time after $\overline{RE}$ low	5	—	7	—	10	—	ns	
t_{RAS}	$\overline{RE}$ pulse width	40	100K	50	100K	60	100K	ns	
t_{RC},t_{WC}	Random read or write cycle time	75	—	90	—	110	—	ns	1,2
t_{RCD}	Delay from $\overline{RE}$ low to $\overline{CE}$ low	17	28	19	35	20	40	ns	3,5
t_{RP}	$\overline{RE}$ precharge time	20	—	25	—	30	—	ns	1,6,7
t_{RSH}	$\overline{RE}$ hold time	12	—	14	—	15	—	ns	
t_T	Transition time (rise and fall)	3	50	3	50	3	50	ns	
t_{WSR}	Write setup time before $\overline{RE}$ low	0	—	0	—	0	—	ns	
t_{WCR}	Write hold time after $\overline{RE}$ low	25	—	30	—	35	—	ns	

1. An initial pause of 100µs is required after power-up followed by 8 $\overline{CE}$ before $\overline{RE}$ refresh cycles for proper device operation
2. AC measurements assume t_T = 5ns.
3. Operation within the t_{RCD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled by t_{CAC}.
4. Operation within the t_{RAD}(max) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max) limit, then access time is controlled by t_{AA}.
5. t_{RCD} and t_{CAH} cannot be at minimum values simultaneously. $t_{RCD} + t_{CAH} \geq$ 40ns (40ns t_{RAC} product), $t_{RCD} + t_{CAH} \geq$ 45ns (50ns t_{RAC} product),$t_{RCD} + t_{CAH} \geq$ 50ns (60ns t_{RAC} product)
6. t_{RWL} and t_{RP} cannot be at minimum values simultaneously. $t_{RWL} + t_{RP} \geq$ 40ns (40ns t_{RAC} product), $t_{RWL} + t_{RP} \geq$ 50ns (50ns t_{RAC} product),$t_{RWL} + t_{RP} \geq$ 60ns (60ns t_{RAC} product)
7. t_{CWL} and t_{RP} cannot be at minimum values simultaneously. $t_{CWL} + t_{RP} \geq$ 40ns (40ns t_{RAC} product), $t_{CWL} + t_{RP} \geq$ 50ns (50ns t_{RAC} product),$t_{CWL} + t_{RP} \geq$ 60ns (60ns t_{RAC} product)
8. t_{CRP} must be 10ns (40ns t_{RAC}) or 12ns (50ns t_{RAC}) or 15ns (60ns t_{RAC}) if a write-per-bit mask is used on the following $\overline{RE}$ cycle due to the fact that t_{OFF} must be met.

Write Cycle

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CWL}	Write Command setup before $\overline{CE}$ high	12		14		15	—	ns	4
t_{DH}	Data-in hold time after $\overline{CE}$ or $\overline{W}$ low, whichever is later	5		8		10	—	ns	1
t_{DHR}	Data-in hold time after $\overline{RE}$ low	20		25		30	—	ns	
t_{DSC}	Data-in setup before $\overline{CE}$ low	0		0		0	—	ns	
t_{DSW}	Data-in setup before $\overline{W}$ low	0		0		0	—	ns	
t_{GHD}	$\overline{OE}$ high before data-in applied on primary port data pins	10		12		15	—	ns	
t_{RWL}	Write setup time before $\overline{RE}$ high	12		14		15	—	ns	3
t_{WCH}	Write hold time after $\overline{CE}$ low	5		7		10	—	ns	
t_{WCS}	Early write command setup before $\overline{CE}$ Low	0		0		0	—	ns	1,2
t_{WP}	Write command pulse width	5		7		10	—	ns	

1. Data-in setup and hold is measured from the later of the two timings - $\overline{CE}$ / $\overline{UCE}$ / $\overline{LCE}$
2. t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{CPW} \geq t_{CPW}$ (min) (Fast Page) mode, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.
3. t_{RWL} and t_{RP} cannot be at minimum values simultaneously. $t_{RWL} + t_{RP} \geq 40$ns (40ns t_{RAC} product), $t_{RWL} + t_{RP} \geq 50$ns (50ns t_{RAC} product),$t_{RWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product
4. t_{CWL} and t_{RP} cannot be at minimum values simultaneously. $t_{CWL} + t_{RP} \geq 40$ns (40ns t_{RAC} product), $t_{CWL} + t_{RP} \geq 50$ns (50ns t_{RAC} product),$t_{CWL} + t_{RP} \geq 60$ns (60ns t_{RAC} product),

Read-Modify-Write Cycle

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AWD}	Column address to $\overline{W}$ low	38		45		50	—	ns	1
t_{CWD}	$\overline{CE}$ low before $\overline{W}$ low	30		35		40	—	ns	1
t_{OEH}	Output disable ($\overline{OE}$ high) hold time from $\overline{W}$ low	0		0		0	—	ns	
t_{RWC}	Read-modify-write cycle time	110		130		165	—	ns	

1. t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive parameters. They are included as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min) the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; if $t_{RWD} \geq t_{RWD}$(min), $t_{CWD} \geq t_{CWD}$(min), and $t_{CPW} \geq t_{CPW}$ (min) (Fast Page) mode, the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions are satisfied, the condition of the data out (at access time) is indeterminate.

Read Cycle

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{AA}	Access time from column address		20		25	—	30	ns	2,3
t_{CAC}	Access time from $\overline{CE}$		12		14	—	15	ns	1,2,3
t_{OEA}	Access time from $\overline{OE}$		12		14	—	15	ns	
t_{OES}	Output enable setup ($\overline{OE}$ low) before $\overline{RE}$ high	1		1		1	—	ns	
t_{OEZ}	Primary output disable from $\overline{OE}$ high		10		12		15	ns	
t_{OFF}	Primary output disable from $\overline{CE}$		10		12	0	15	ns	5
t_{RAC}	Access time from $\overline{RE}$		40		50	—	60	ns	1,2,3
t_{RAL}	Column address to $\overline{RE}$ high	22		25		30	—	ns	
t_{RCH}	Read hold time after $\overline{CE}$ goes high	0		0		0	—	ns	4
t_{RCS}	Read command setup time	0		0		0	—	ns	
t_{RRH}	Read command hold time to $\overline{RE}$ high	0		0		0	—	ns	4

1. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only: If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
2. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met t_{RAD}(max.) is specified as a reference point only: If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
3. Measured with the specified current and 50 pF load for the primary port. Output referenced levels: V_{OH} = 2.0V and V_{OL} = 0.8V.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. t_{OFF}(max.) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

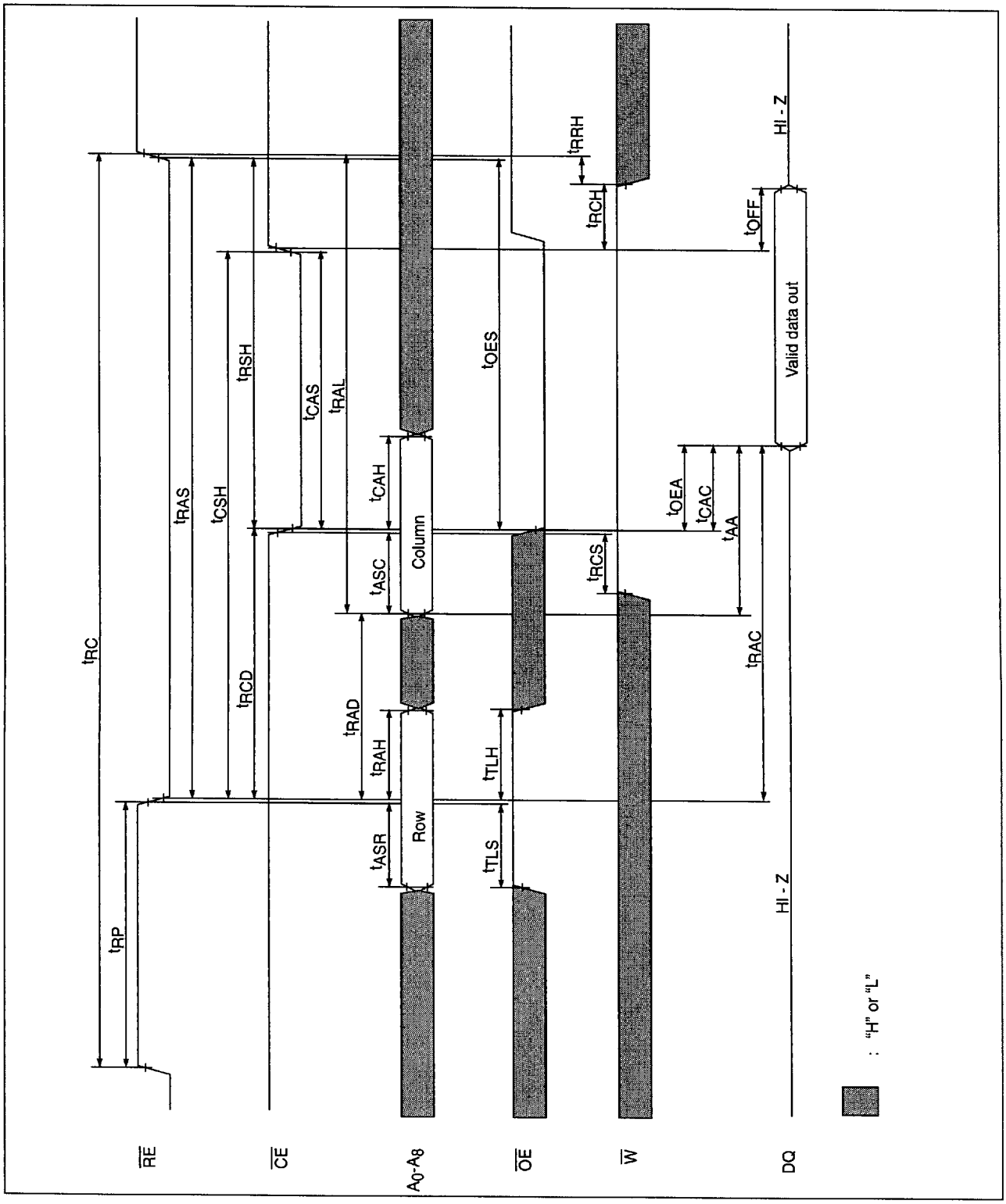
Page Mode Cycle

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{ACP}	Access time from $\overline{CE}$ precharge		20		25	—	30	ns	
t_{HPC}	Extended data out cycle time	15		20		25	—	ns	
t_{PC}	Fast page mode cycle time	20		25		30	—	ns	

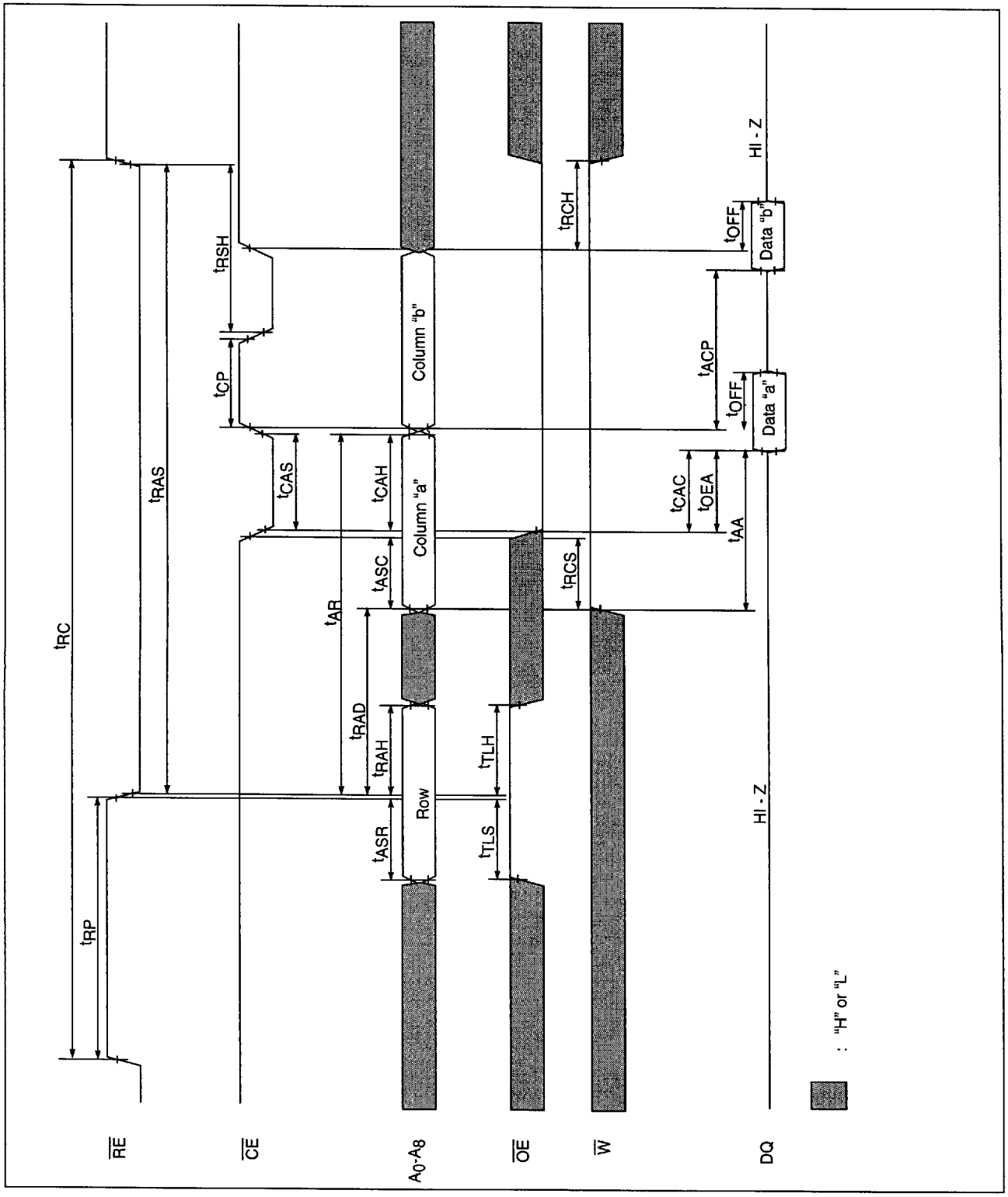
Refresh Cycle

Symbol	Parameter	-40		-50		-60		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{CHR}	$\overline{CE}$ held low after $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	12		14		15	—	ns	
t_{CSR}	$\overline{CE}$ low setup before $\overline{RE}$ low ($\overline{CE}$ before $\overline{RE}$ refresh)	5		5		7	—	ns	
t_{REF}	Refresh period		32		32	—	32	ms	
t_{RPC}	$\overline{RE}$ high to $\overline{CE}$ low precharge	0		0		0	—	ns	

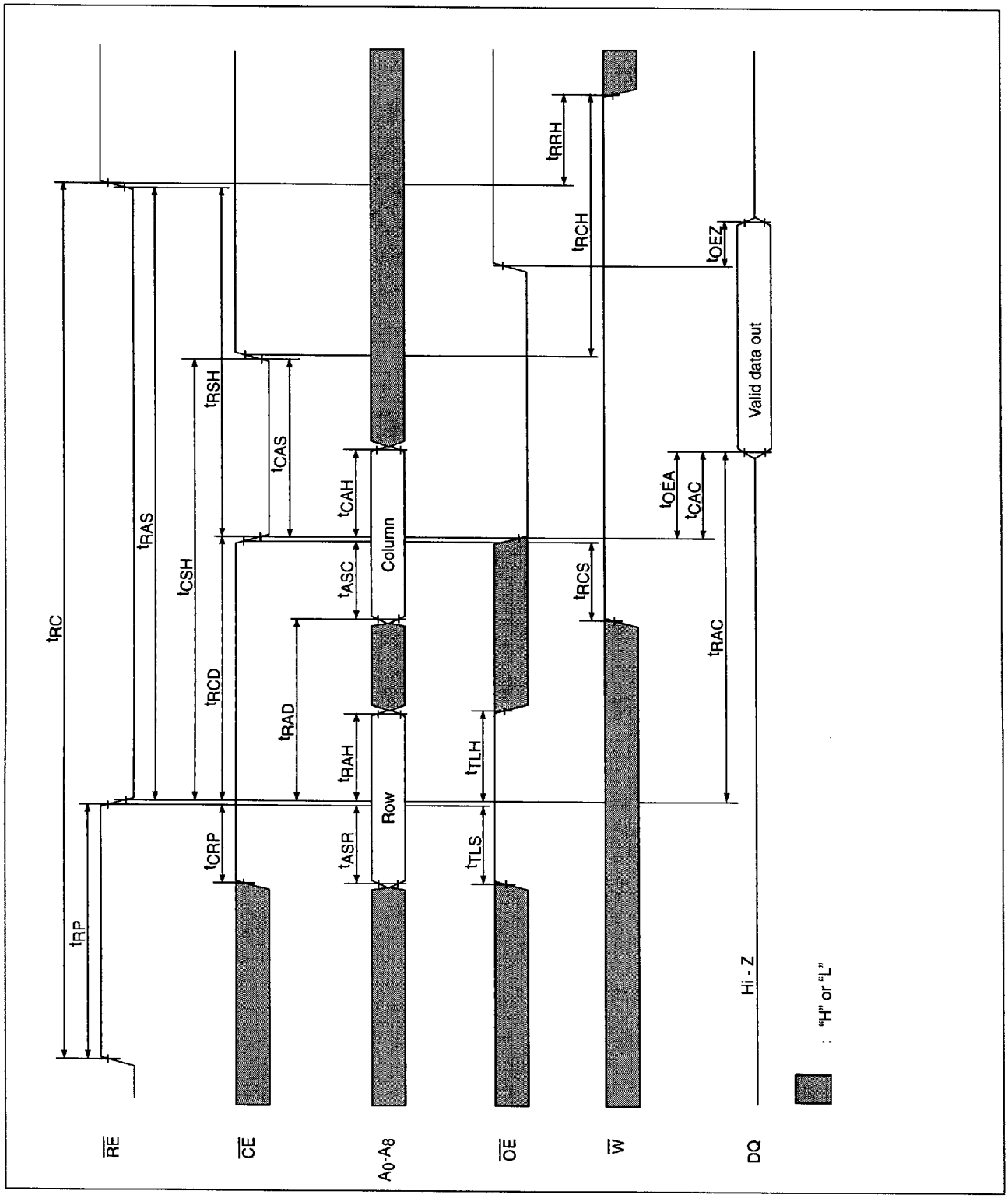
Fast Page (FP) Read Cycle



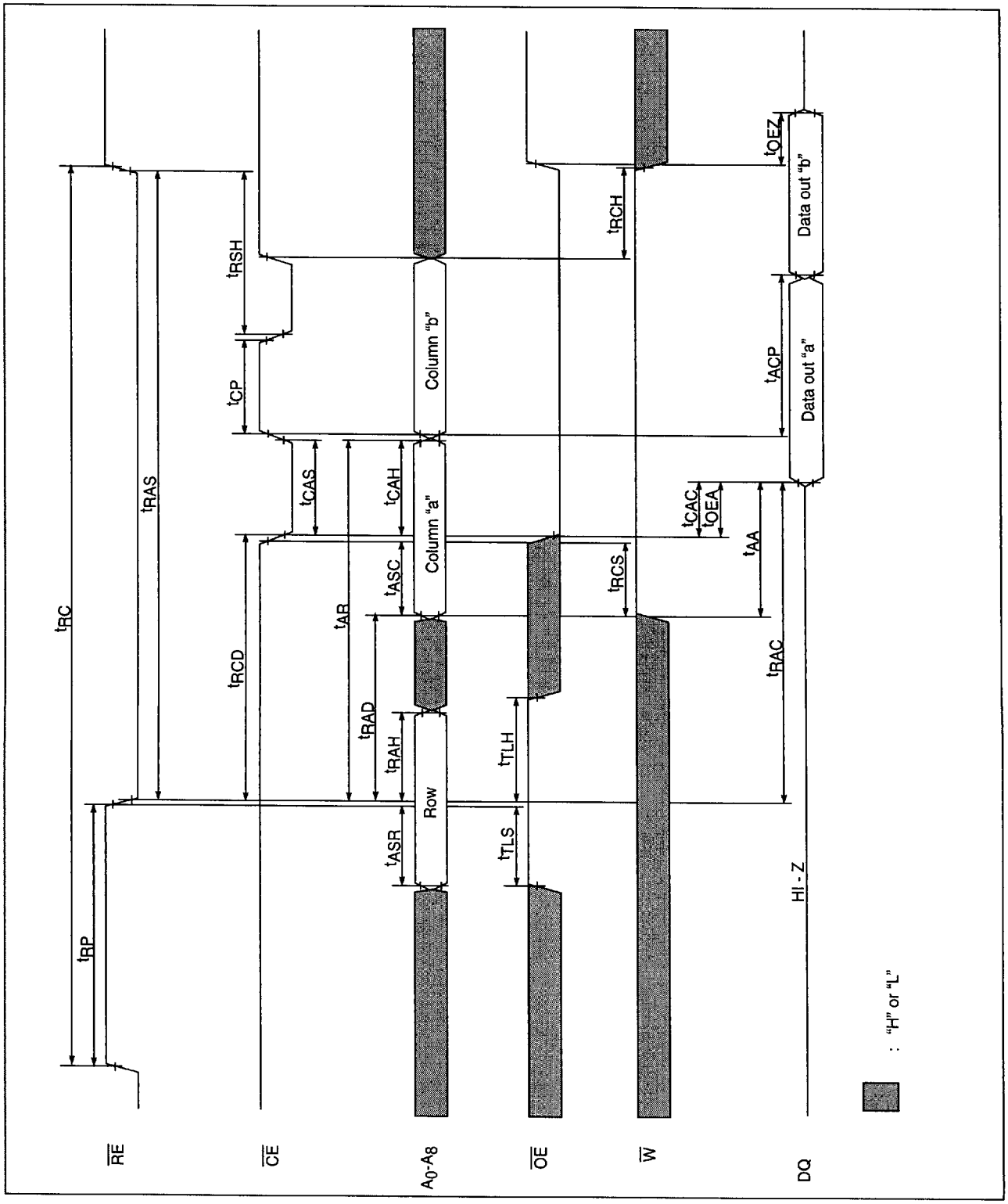
Fast Page Read Operation



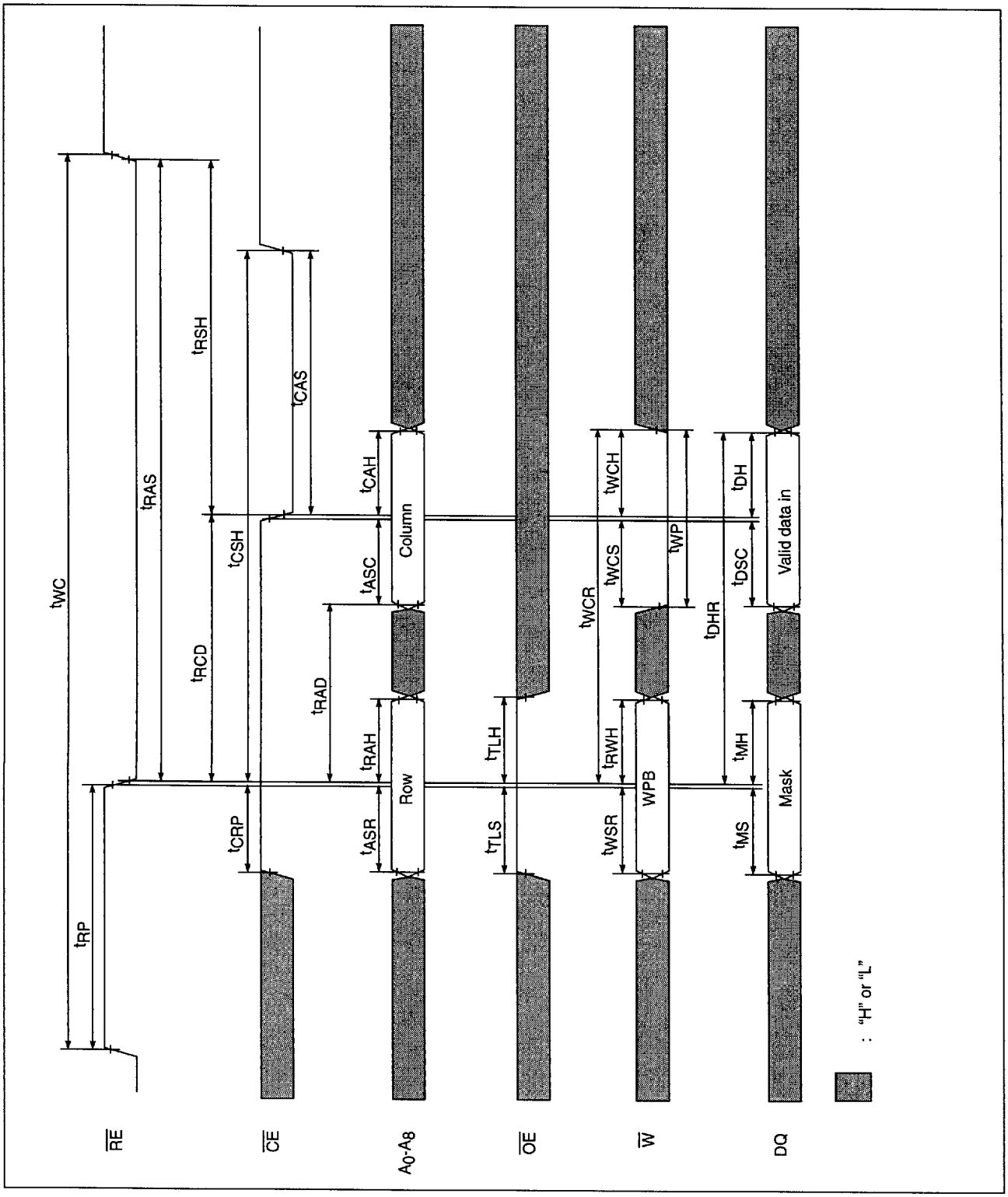
EDO Page Read Cycle



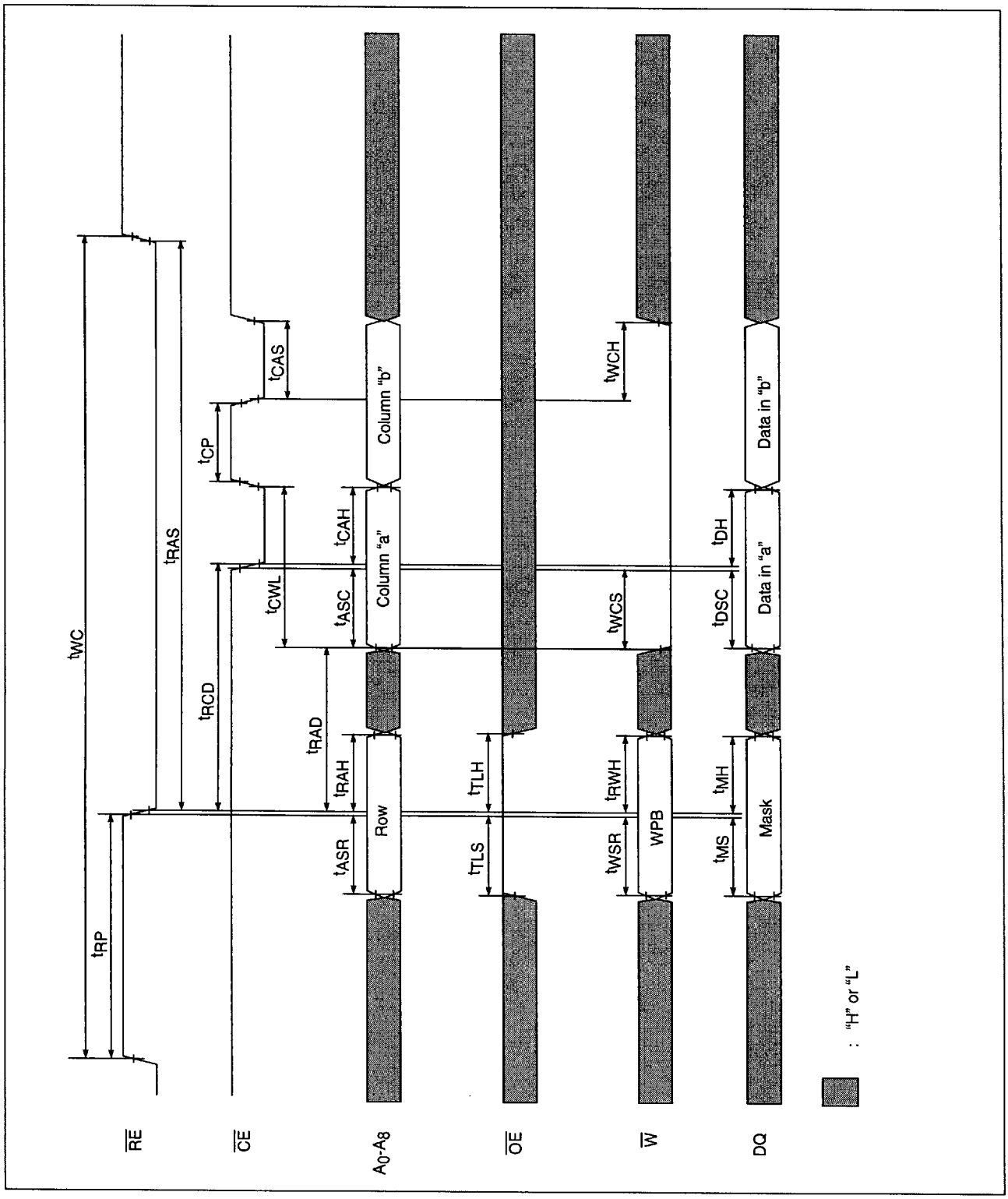
EDO Page Read Operation



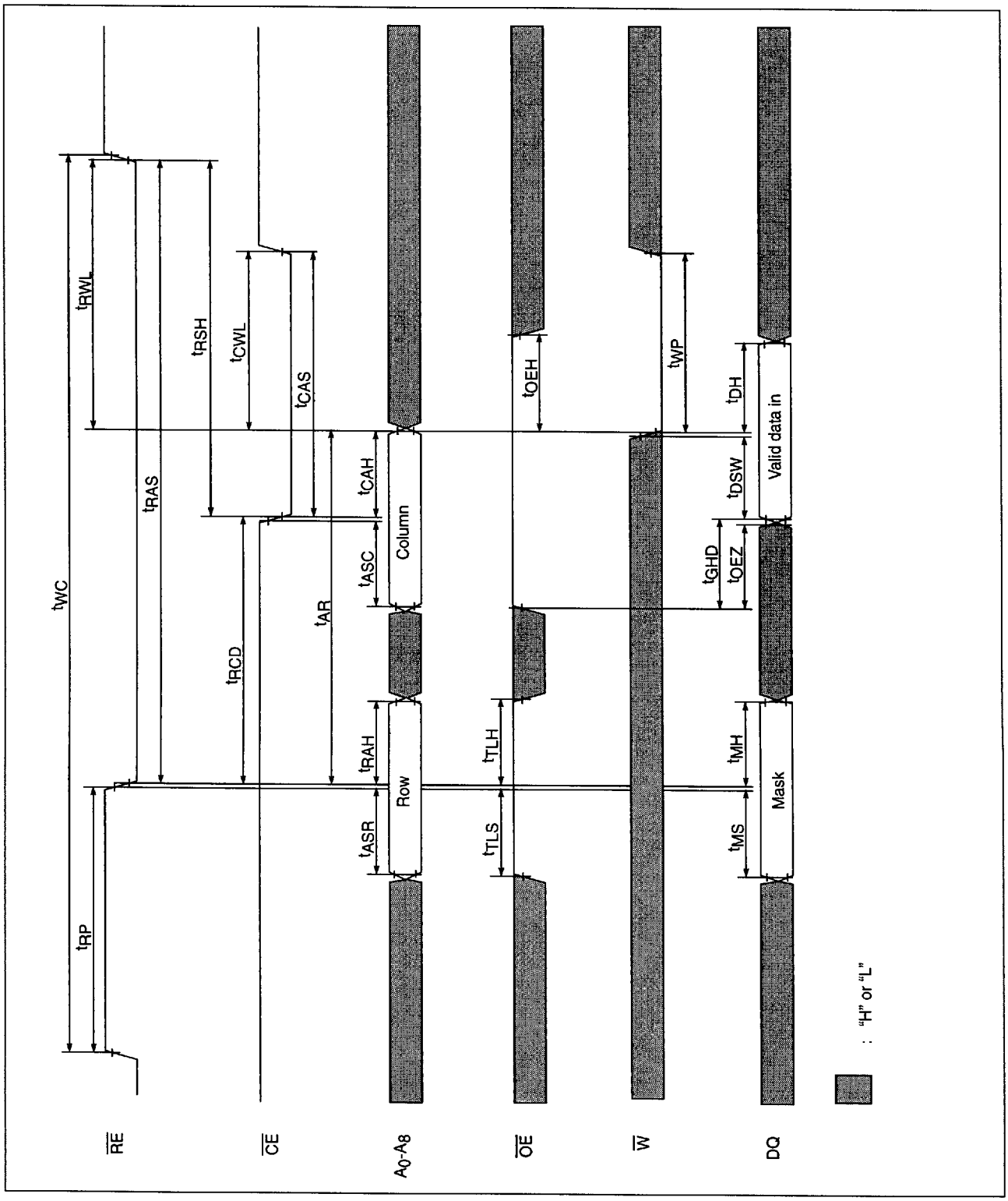
Write Cycle (Early Write)



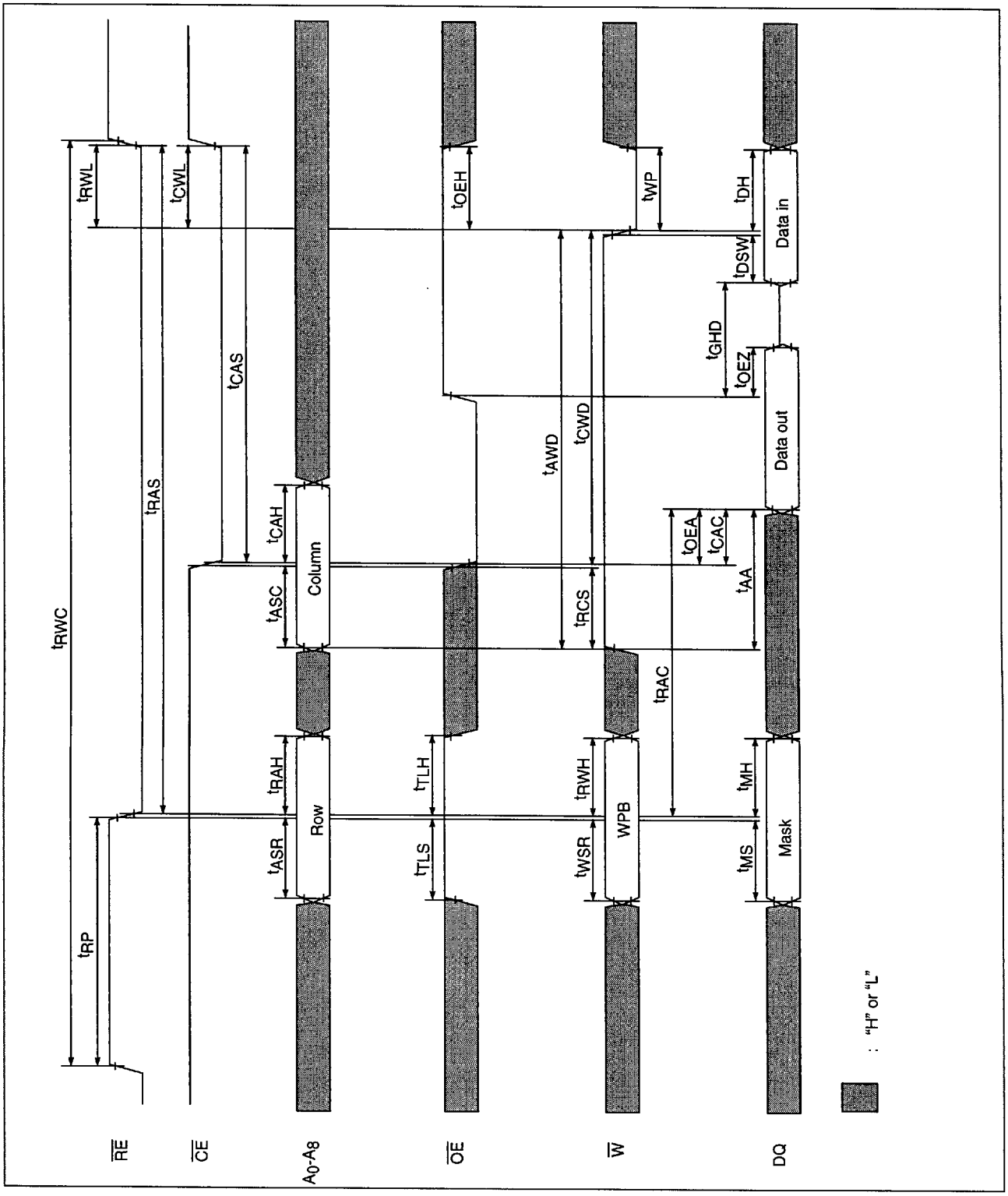
Fast Page Mode (Early Write)



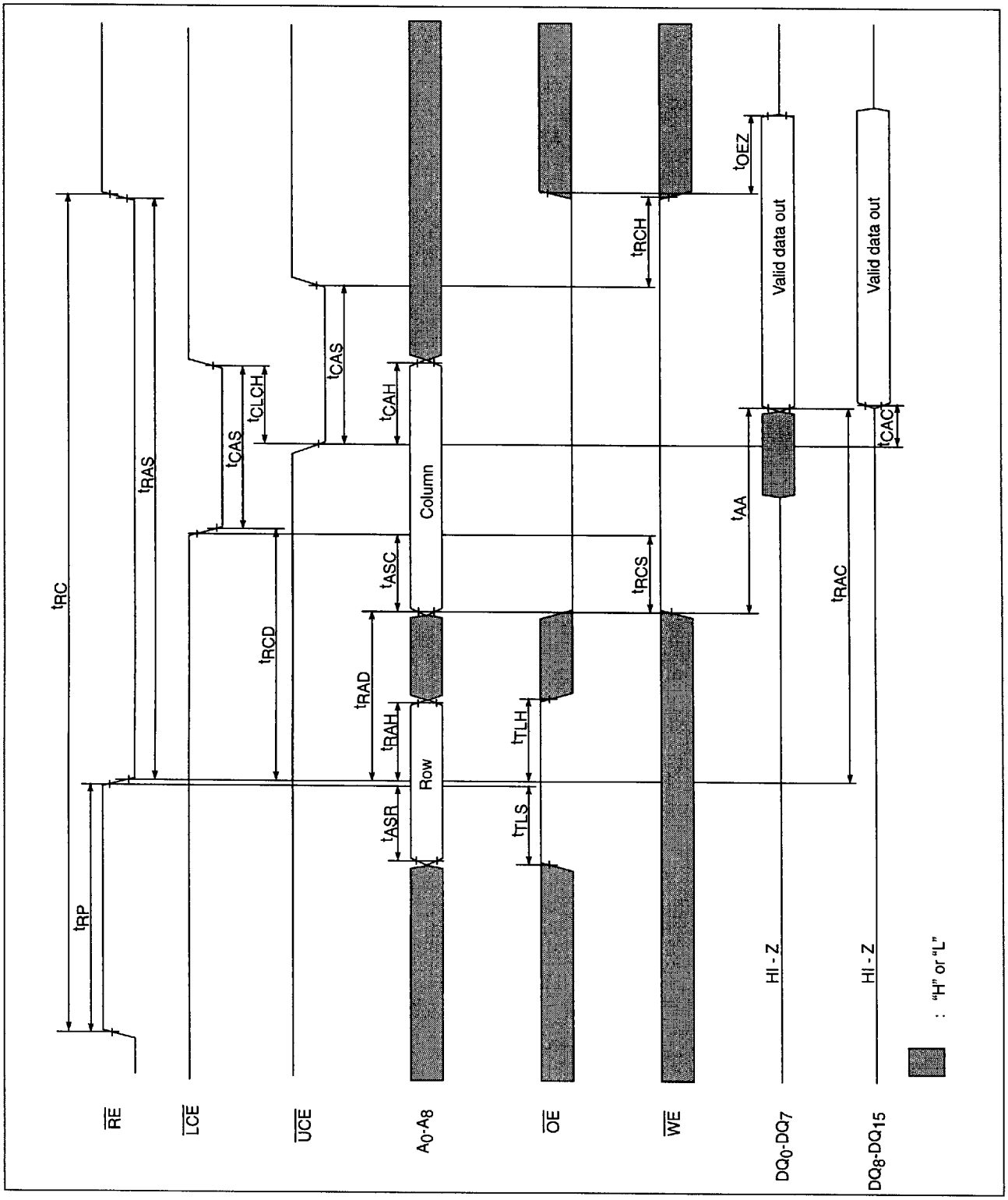
Write Cycle (Late Write)



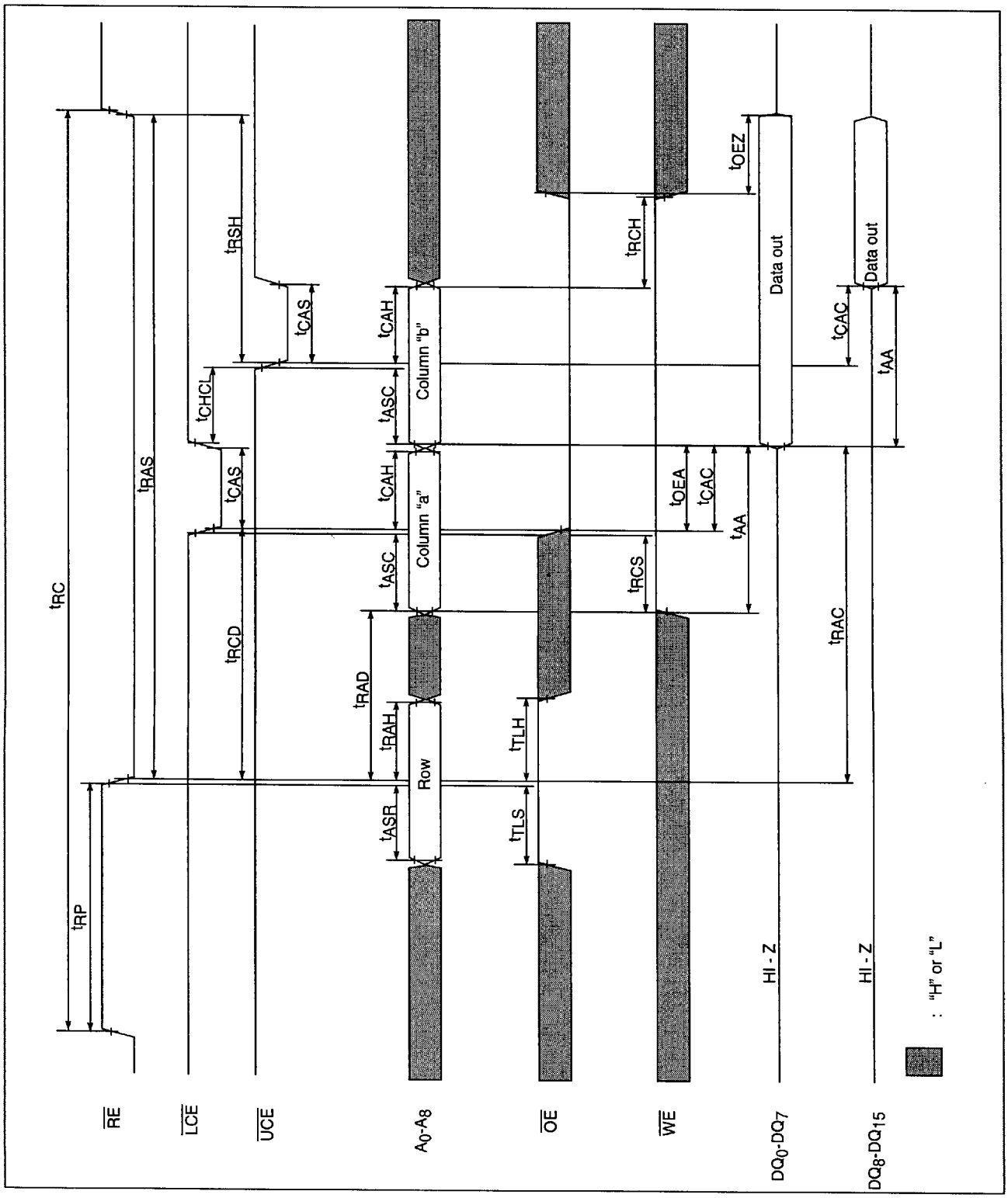
Read-Modify-Write Cycle



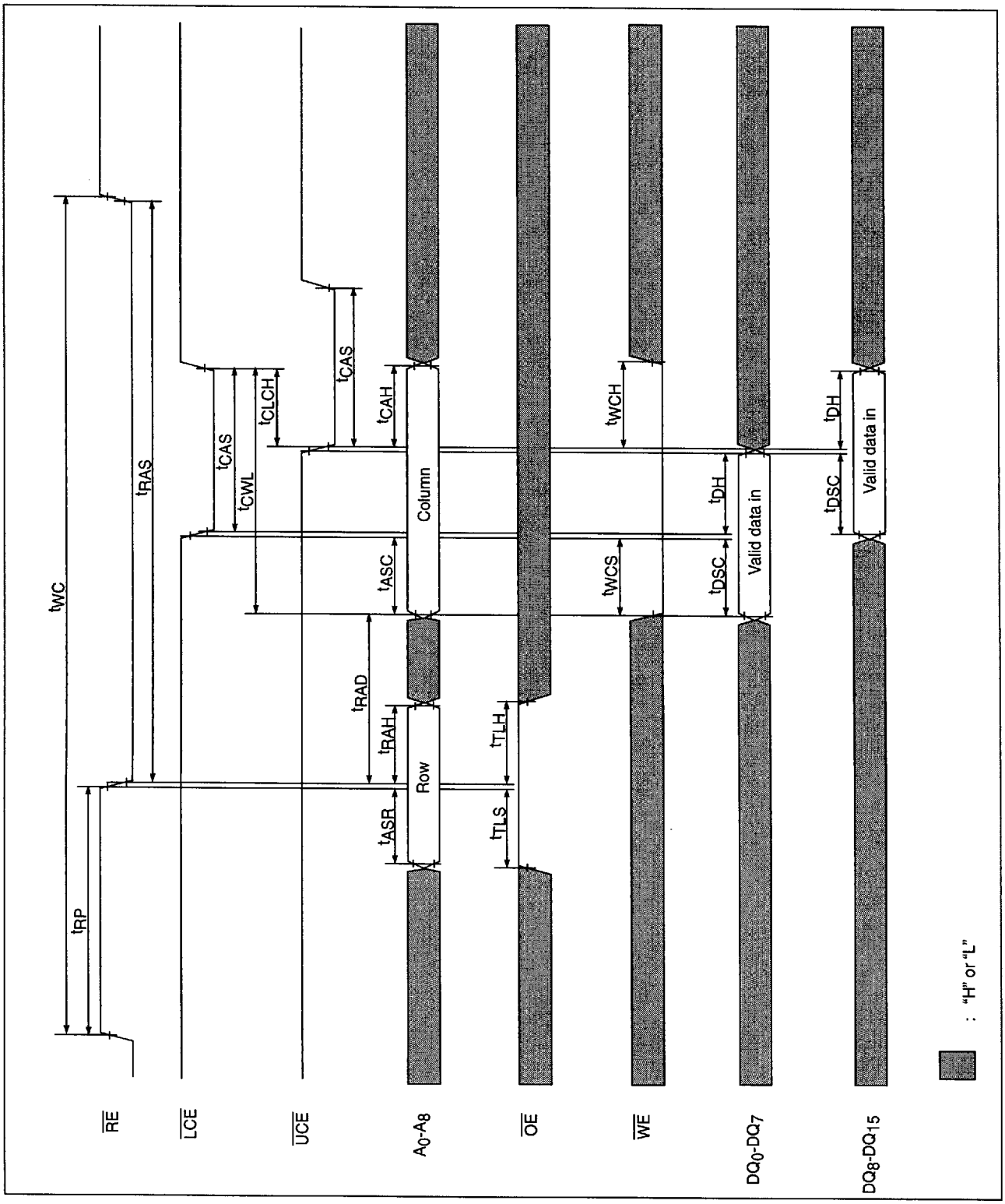
Skewed $\overline{CE}$ (Overlapping $\overline{CE}$) EDO Read Operation



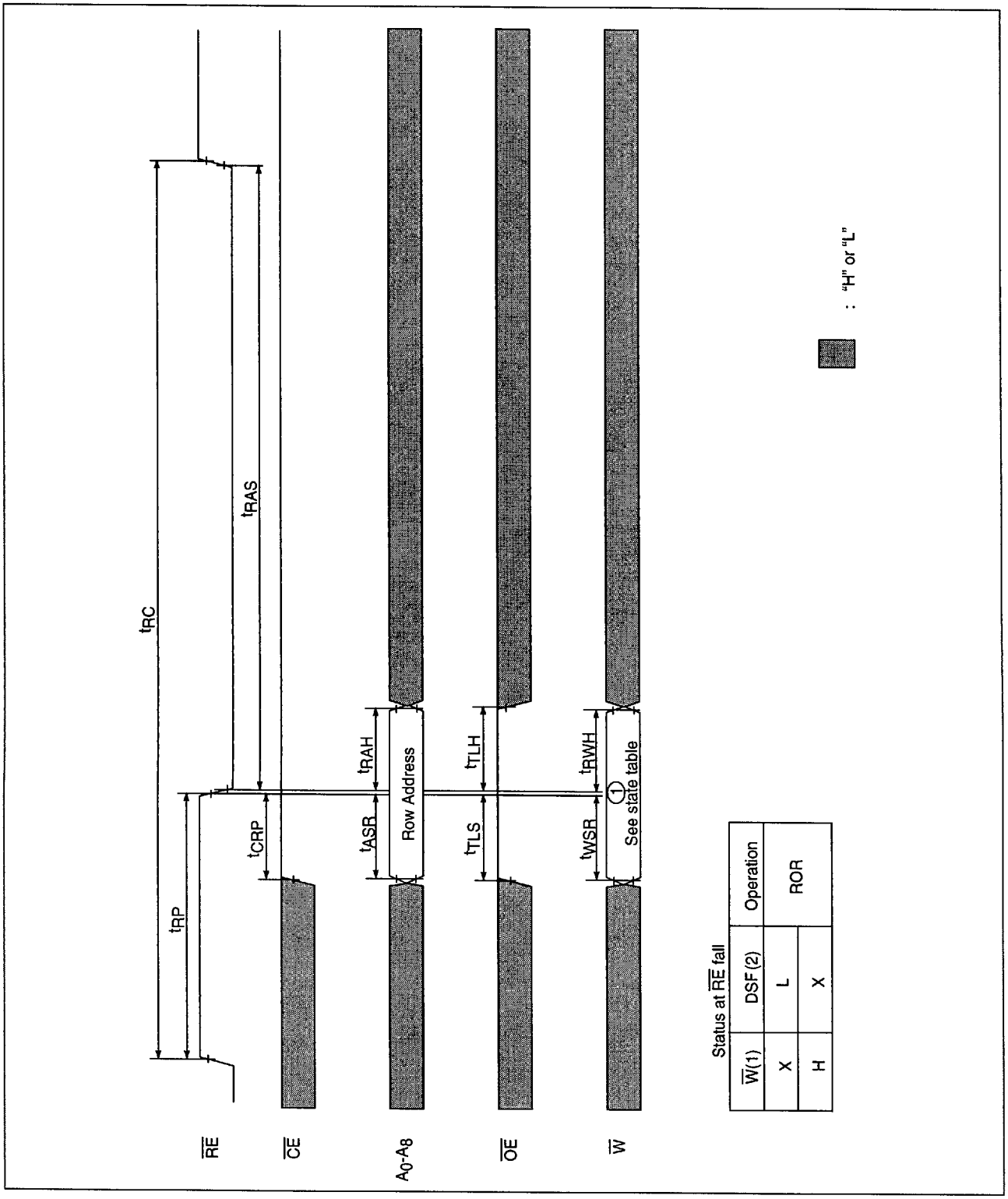
Skewed $\overline{CE}$ (Non-Overlapping $\overline{CE}$) EDO Read Operation



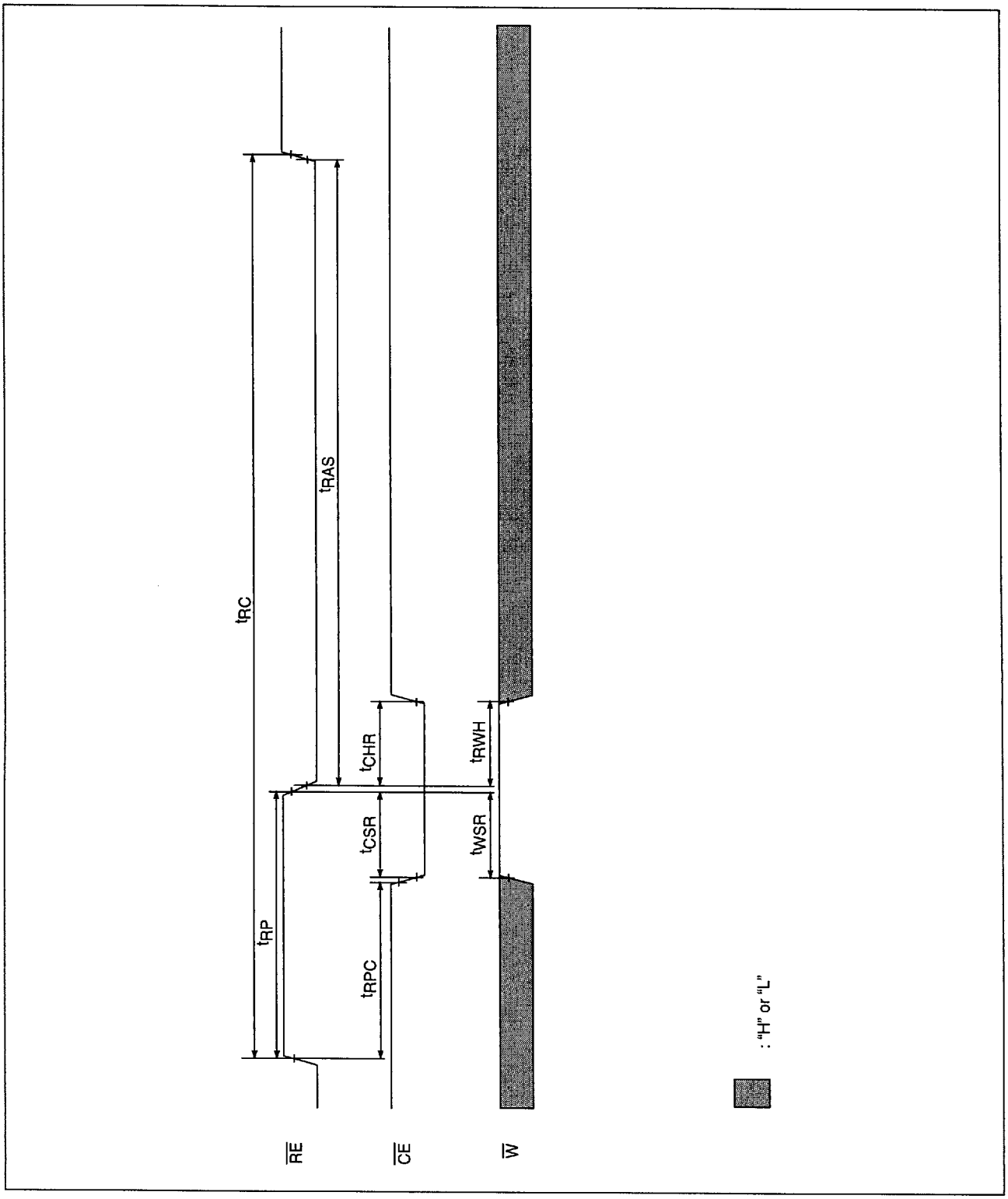
2 $\overline{CE}$ Byte Write Operation ($\overline{CE}$ Overlapping)



$\overline{RE}$ Only Refresh (ROR)



$\overline{CE}$ Before $\overline{RE}$ Refresh (CBR-With Mode Reset)



Functional Description

The DRAM array is organized as 512 rows x 512 columns x 16 bit wide. The device is capable of performing normal Read/Write operations.

Power Up or DRAM Initialize Process

After V_{cc} has reached its regulated value, allow at least 100µs for build up of N-well voltage inside the chip. Perform at least 8 $\overline{CAS}$-Before-$\overline{RAS}$ (CBR) refresh cycles to reset unwanted mode(s) which may be set during power up.

DRAM Refresh Operation

DRAM array consists of volatile cells, therefore, these cells need to be refreshed periodically. The minimum rate for DRAM is 512 refresh cycles every 8ms. Every cell therefore gets a chance to be refreshed every 8ms.

The following refresh modes are available in IBM's 4-Mb DRAM:

$\overline{RE}$ Only Refresh (ROR)

A cycle having only $\overline{RE}$ active refreshes all cells in one row of the storage array. A high $\overline{CE}$ is maintained while $\overline{RE}$ is active to keep DQs in high impedance. This method is preferred for refreshing, especially when the host system consists of multiple rows of random access devices. The data outputs may be OR-tied with no bus contention when $\overline{RE}$ only refresh cycles are executed.

Note that the row address for refresh is supplied by the user. ***$\overline{RE}$ only Refresh mode will not clear any unknown modes at powerup. Therefore, CBR cycles at powerup must be performed to clear any unknown modes***. The timing diagram on page 21 shows a $\overline{RE}$ only Refresh mode.

$\overline{CE}$ before $\overline{RE}$ Refresh (CBR)

The CBR Refresh mode is selected by bringing the $\overline{CE}$ low before $\overline{RE}$ is brought low as shown in the timing diagram on page 22. An internal address counter selects the row to be refreshed. Note that DQs are in high-Z state during CBR cycle.

Recommended CBR Cycle

To ensure that the device has not entered unwanted register modes at power up, at least ***eight CBR cycles must be executed before normal operation of the device is resumed***. A CBR after each vertical retrace is recommended. This fail-safe routine is for cases where a system misoperation causes entry into an unwanted mode.

Byte Control

The 4-Mb DRAM is available with Dual $\overline{CE}$. A dual $\overline{CE}$ part has lower and upper byte control. The $\overline{LCE}$ controls the DQ_0 -DQ_7 while $\overline{UCE}$ controls DQ_8 - DQ_{15}. Individual byte control can be applied during read and write operations on the primary port.

Read Cycle

A Read cycle is executed by activating $\overline{RE}$, $\overline{CE}$, and $\overline{OE}$ and by maintaining $\overline{W}$ high while $\overline{CE}$ is active. The DQs remain in high-Z until valid data appears at the output at access time. Device access time, t_{ACC}, will be the longest of the four calculated intervals:

- t_{RAC}- Access time from $\overline{RE}$ falling edge
- t_{RCD} ($\overline{RE}$ to $\overline{CE}$ delay) + t_{CAC} (Access time from $\overline{CE}$ falling edge)
- t_{RAD} ($\overline{RE}$ to Column Address delay) + t_{AA} (Access time from column Address)
- $\overline{RE}$ to $\overline{OE}$ delay + t_{OEA} (Access time from $\overline{OE}$)

Device dependent parameters are: t_{RAC}, t_{CAC}, t_{AA} and t_{OEA}. System dependent parameters are: t_{RCD}, t_{RAD} and $\overline{RE}$ to $\overline{OE}$ delay. Output becomes valid after the access time has elapsed. It remains valid while $\overline{CE}$ and $\overline{OE}$ are low (Fast Page parts only). It remains valid while $\overline{OE}$ is low (EDO parts only). Either $\overline{CE}$ or $\overline{OE}$ high returns the output pins to high-Z (Fast Page parts only). $\overline{OE}$ high returns the output pins to high-Z (EDO parts).

Write Cycle

A Write cycle is executed by bringing $\overline{W}$ low during $\overline{RE}$/$\overline{CE}$ cycle. The falling edge of $\overline{CE}$ or $\overline{W}$ whichever occurs later strobes the data on DQ pins into the on-chip data latch.

Early Write Cycle

An early Write cycle is executed by bringing $\overline{W}$ low before $\overline{CE}$ falls. Data is strobed by $\overline{CE}$ with setup and hold times referenced to this signal. This is the mode that is generally used for graphics applications. $\overline{OE}$ can be in any state while $\overline{W}$ is active.

Late Write Cycle

A late Write is executed by bringing $\overline{W}$ low after $\overline{CE}$ goes low. The input data is strobed by $\overline{W}$ with setup and hold times referenced to $\overline{W}$ signal. The late Write cycle is used for Read-Modify-Write operations.

Write-Per-Bit Mask (WPBM) Cycle

A Write-Per-Bit cycle uses an I/O mask function to allow the system designer the flexibility of writing or not writing any combinations of DQ_0 through DQ_{15}.

- ***Non-persistent Mask or New mask***

  Note: This mask has to be loaded at each $\overline{RE}$ fall time as shown in the timing diagram on page 14. $\overline{W}$ must be low as $\overline{RE}$ falls. The DQs latched at $\overline{RE}$ fall time are used as mask bits for Write cycle(s) for the particular $\overline{RE}$ cycle. If mask bit is "1", the corresponding DQ input bit is written. If mask bit is "0", the corresponding DQ input is not written.

Read-Write/Read-Modify-Write Cycle

A Read-Modify-Write is performed by first performing a normal Read, then tri-stating the DQ pins with $\overline{OE}$, placing data to be written on the DQ pins, and then executing a Write operation. A WPBM can be loaded at the falling edge of $\overline{RE}$. The input data is strobed in reference to $\overline{W}$. This operation is illustrated in the timing diagram on page 17.

Fast Page Cycle Operation

Fast page mode cycles allow faster memory access by using the same row address while successive column addresses are strobed onto the chip. The $\overline{RE}$ signal is kept low while successive $\overline{CE}$ cycles are executed. The data rate is faster because row addresses are maintained internally and do not have to be reapplied. In fast page mode operation, Read, Write, Read - modify - Write cycles may be executed. During a fast-page read cycle, the DQ pins stay in high-Z until valid data appears at the output pins at access time. The access time in this cycle will be the longest of the following intervals.

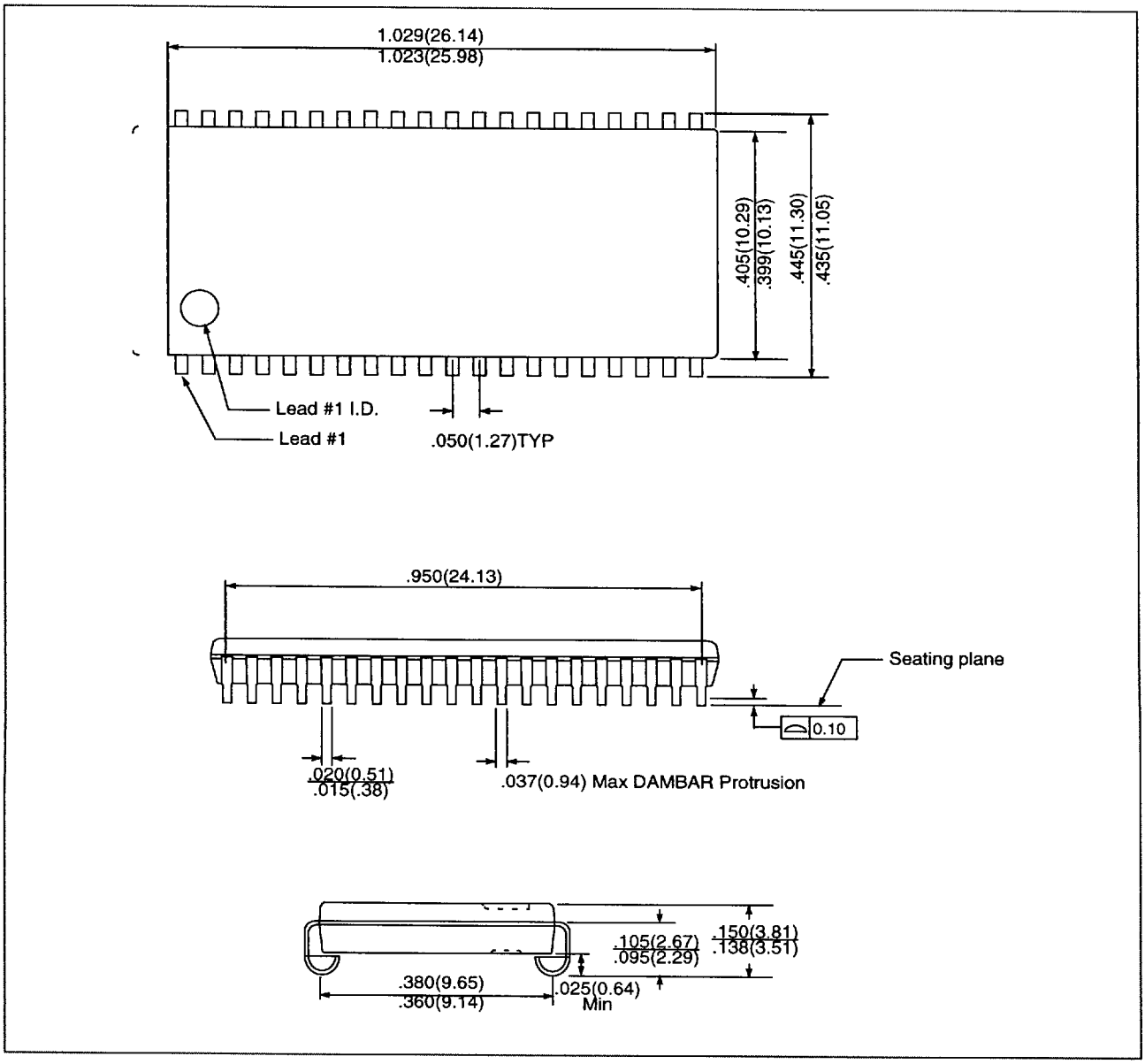
t_{ACP} = Access time from start of column precharge
$t_{CP} + t_T + t_{CAC}$= Column precharge time + transition time
+ Access time from $\overline{CE}$ fall time
= $\overline{CE}$ high to column address delay + t_{AA}

Extended Data Out (EDO)

In extended data out mode, the primary port output drivers are not turned off by the rising edge of $\overline{CE}$. As rising edge of $\overline{CE}$ does not turn off the data, the resulting longer data valid time allows speed up of the fast page cycle time. ***Fast page mode applications that try to run at minimum cycle times find that timing skews and propagation delays make the data valid time so narrow that reliable sampling is impossible.*** EDO solves this problem by providing longer data valid time. The device access time is the longest of the following intervals:

- t_{ACP}
- t_{AA}
- t_{CAC}

Package Diagram



Revision Log

Rev	Contents of Modification
11/95	Initial Release
04/96	Major revision. Added -40 and -50 options. Removed -6H and -70 options.