

Features

- 4,194,304 word by 16 bit organization
- Single $3.3 \pm 0.3V$ power supply
- Extended Data Out (Hyper Page Mode)
- \overline{CAS} before \overline{RAS} Refresh
 - 4096 cycles/retention Time
- \overline{RAS} only Refresh
 - 4096 cycles/Retention Time
- 64ms Standard Power (SP) Retention Time
- 128ms Low Power (LP) Retention Time
- Hidden Refresh
- Self Refresh (400 μA) - LP Version Only
- Read-Modify-Write

- Dual \overline{CAS} Byte Read/Write
- Performance:

| | | -50 | -60 |
|-----------|----------------------------------|------|-------|
| t_{RAC} | \overline{RAS} Access Time | 50ns | 60ns |
| t_{CAC} | \overline{CAS} Access Time | 13ns | 15ns |
| t_{AA} | Column Address Access Time | 25ns | 30ns |
| t_{RC} | Cycle Time | 84ns | 104ns |
| t_{HPC} | EDO (Hyper Page) Mode Cycle Time | 20ns | 25ns |

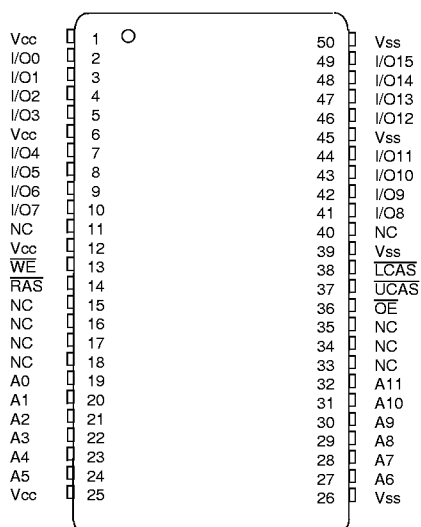
- Max. Power Dissipation (-50)
 - Active: 504mW
 - Standby (SP version): 2.0 mA
 - Standby (LP version): 0.2 mA
- Package: TSOP-50 (400milx825mil)

Description

The IBM0165165B/P is a dynamic RAM organized 4,194,304 words by 16 bits. This device is fabricated in IBM's most advanced CMOS silicon gate process technology. The circuit and process design allow this DRAM to achieve high performance and low power dissipation. The IBM0165165B/P operates with a single $3.3 \pm 0.3V$ power supply, and interfaces directly with either TTL or CMOS levels. The 22 addresses required to access any bit of data are

multiplexed (12 are strobed with \overline{RAS} , 10 are strobed with \overline{CAS}). They are packaged in a 50 pin plastic TSOP type II (400milx825mil). The IBM0165165P parts are low power devices supporting Self Refresh and a 256ms retention time.

Pin Assignments (Top View)



Pin Description

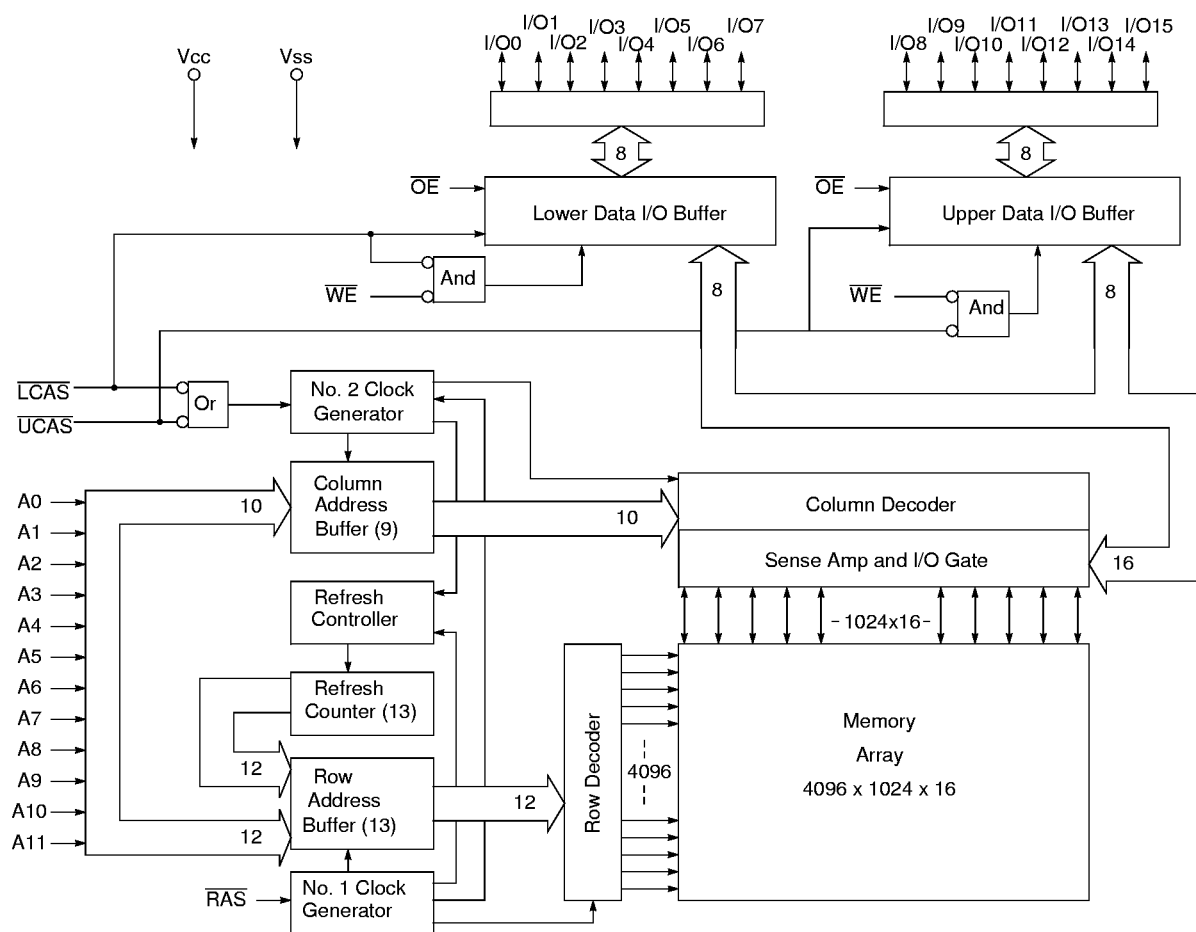
| | |
|-------------------------------------|-----------------------|
| \overline{RAS} | Row Address Strobe |
| $\overline{LCAS} / \overline{UCAS}$ | Column Address Strobe |
| \overline{WE} | Read/write Input |
| A0 - A11 | Address Inputs |
| \overline{OE} | Output Enable |
| I/O0 - I/O15 | Data Input/output |
| V_{CC} | Power (+3.3V) |
| V_{SS} | Ground |

Ordering Information

| Part Number | Power | Self Refresh | Power Supply | Speed | Package | Notes |
|-------------------|-------|--------------|--------------|-------|----------------|-------|
| IBM0165165BT3C-50 | SP | No | 3.3V | 50ns | 400mil TSOP 50 | 1 |
| IBM0165165BT3C-60 | SP | No | 3.3V | 60ns | 400mil TSOP 50 | 1 |
| IBM0165165PT3C-50 | LP | Yes | 3.3V | 50ns | 400mil TSOP 50 | 1 |
| IBM0165165PT3C-60 | LP | Yes | 3.3V | 60ns | 400mil TSOP 50 | 1 |

1. SP = Standard Power version (IBM0165165B); LP = Low Power version (IBM0165165P)

Block Diagram





Truth Table

| Function | | $\overline{\text{RAS}}$ | $\overline{\text{LCAS}}$ | $\overline{\text{UCAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Row Address | Column Address | I/O0 - I/O15 |
|--|-----------|-------------------------|--------------------------|--------------------------|------------------------|------------------------|-------------|----------------|--|
| Standby | | H | H→X | H→X | X | X | X | X | High Impedance |
| Read: Word | | L | L | L | H | L | Row | Col | Data Out |
| Read: Lower Byte | | L | L | H | H | L | Row | Col | Lower Byte: Data Out Upper Byte: High-Z |
| Read: Upper Byte | | L | H | L | H | L | Row | Col | Lower Byte: High-Z Upper Byte: Data Out |
| Write: Word Early-Write | | L | L | L | L | X | Row | Col | Data In |
| Write: Lower Byte Early-Write | | L | L | H | L | X | Row | Col | Lower Byte: Data In Upper Byte: High-Z |
| Write: Upper Byte Early-Write | | L | H | L | L | X | Row | Col | Lower Byte: High-Z Upper Byte: Data In |
| Read-Modify-Write | | L | L | L | H→L | L→H | Row | Col | Data Out, Data In |
| EDO (Hyper Page) Mode Read | 1st Cycle | L | H→L | H→L | H | L | Row | Col | Data Out |
| | 2nd Cycle | L | H→L | H→L | H | L | N/A | Col | Data Out |
| EDO (Hyper Page) Mode Write | 1st Cycle | L | H→L | H→L | L | X | Row | Col | Data In |
| | 2nd Cycle | L | H→L | H→L | L | X | N/A | Col | Data In |
| EDO (Hyper Page) Mode Read-Modify-Write | 1st Cycle | L | H→L | H→L | H→L | L→H | Row | Col | Data Out, Data In |
| | 2nd Cycle | L | H→L | H→L | H→L | L→H | N/A | Col | Data Out, Data In |
| $\overline{\text{RAS}}$ -Only Refresh | | L | H | H | X | X | Row | N/A | High Impedance |
| $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh | | H→L | L | L | H | X | X | N/A | High Impedance |
| Hidden Refresh | Read | L→H→L | L | L | H | L | Row | Col | Data Out |
| | Write | L→H→L | L | L | L→H | X | Row | Col | Data In |
| Self Refresh (LP version only) | | H→L | L | L | H | X | X | X | High Impedance |

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|-----------|------------------------------|-----------------------------------|-------|-------|
| V_{CC} | Power Supply Voltage | -0.5 to 4.6 | V | 1 |
| V_{IN} | Input Voltage | -0.5 to min ($V_{CC}+0.5$, 4.6) | V | 1 |
| V_{OUT} | Output Voltage | -0.5 to min ($V_{CC}+0.5$, 4.6) | V | 1 |
| T_{OPR} | Operating Temperature | 0 to +70 | °C | 1 |
| T_{STG} | Storage Temperature | -55 to +150 | °C | 1 |
| P_D | Power Dissipation | 1.0 | W | 1 |
| I_{OUT} | Short Circuit Output Current | 50 | mA | 1 |

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions ($T_A=0$ to 70°C)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Notes |
|----------|--------------------|------|------|----------------|-------|-------|
| V_{CC} | Supply Voltage | 3.0 | 3.3 | 3.6 | V | 1 |
| V_{IH} | Input High Voltage | 2.0 | — | $V_{CC} + 0.3$ | V | 1,2 |
| V_{IL} | Input Low Voltage | -0.3 | — | 0.8 | V | 1,2 |

1. All voltages referenced to V_{SS} .
 2. V_{IH} may overshoot to $V_{CC} + 2.0\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ with 3.3 Volt. V_{IL} may undershoot to -2.0V for pulse widths $\leq 4.0\text{ns}$ with 3.3 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference

Capacitance ($T_A=0$ to $+70^{\circ}\text{C}$, $V_{CC}=3.3 \pm 0.3\text{V}$, $f=1\text{MHz}$)

| Symbol | Parameter | Min. | Max. | Units | Notes |
|----------|---|------|------|-------|-------|
| C_{I1} | Input Capacitance (A0 - A11) | — | 5 | pF | |
| C_{I2} | Input Capacitance ($\overline{\text{RAS}}$, $\overline{\text{LCAS}}$, $\overline{\text{UCAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$) | — | 7 | pF | |
| C_{I3} | Data I/O Capacitance (I/O0 - I/15) | — | 7 | pF | |



DC Electrical Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \pm 0.3\text{V}$)

| Symbol | Parameter | | Min. | Max. | Units | Notes |
|---|---|------------|------|------|---------------|---------|
| I_{CC1} | Operating Current Average Power Supply Operating Current (RAS, CAS, Address Cycling: $t_{RC} = t_{RC \min}$) | -50 | — | 140 | mA | 1, 2, 3 |
| | | -60 | — | 115 | | |
| I_{CC2} | Standby Current (TTL) Power Supply Standby Current (RAS = CAS = V_{IH}) | | — | 2 | mA | |
| I_{CC3} | RAS Only Refresh Current Average Power Supply Current, RAS Only Mode (RAS Cycling, CAS = V_{IH} ; $t_{RC} = t_{RC \min}$) | -50 | | 140 | mA | 1, 3 |
| | | -60 | — | 115 | | |
| I_{CC4} | EDO (Hyper Page) Mode Current Average Power Supply Current, Hyper Page Mode (RAS = V_{IL} , CAS, Address Cycling: $t_{PC} = t_{PC \min}$) | -50 | — | 105 | mA | 1, 2, 3 |
| | | -60 | — | 85 | | |
| I_{CC5} | Standby Current (CMOS) Power Supply Standby Current (RAS = CAS = $V_{CC} - 0.2\text{V}$) | LP version | — | 200 | μA | |
| | | SP version | — | 1 | mA | |
| I_{CC6} | CAS Before RAS Refresh Current Average Power Supply Current, CAS Before RAS Mode (RAS, CAS, Cycling: $t_{RC} = t_{RC \min}$) | -50 | — | 140 | mA | 1, 2 |
| | | -60 | — | 115 | | |
| I_{CC7} | Self Refresh Current (LP version only) Average Power Supply Current during Self Refresh CBR cycle with RAS $\geq t_{RASS}$ (min); CAS held low; WE = $V_{CC} - 0.2\text{V}$; Addresses and $D_{IN} = V_{CC} - 0.2\text{V}$ or 0.2V . | | — | 400 | μA | |
| $I_{I(L)}$ | Input Leakage Current Input Leakage Current, any input ($0.0 \geq V_{IN} \geq V_{CC}$), All Other Pins Not Under Test = 0V | | -2 | +2 | μA | |
| $I_{O(L)}$ | Output Leakage Current (D_{OUT} is disabled, $0.0 \geq V_{OUT} \geq V_{CC}$) | | -2 | +2 | μA | |
| V_{OH} | Output High Level (TTL) Output "H" Level Voltage ($I_{OUT} = -2\text{mA}$) | | 2.4 | — | V | |
| V_{OL} | Output Low Level (TTL) Output "L" Level Voltage ($I_{OUT} = +2\text{mA}$) | | — | 0.4 | V | |
| <p>1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate. 2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open. 3. Column address can be changed once or less while RAS = V_{IL} and CAS = V_{IH}.</p> | | | | | | |

AC Characteristics ($T_A=0$ to $+70^\circ\text{C}$, $V_{CC}=3.3 \pm 0.3\text{V}$)

1. An initial pause of 100 μs is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
2. AC measurements assume $t_T=2\text{ns}$.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. Valid column addresses are only A0 through A9.

Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|-----------|---|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{RC} | Random Read or Write Cycle Time | 84 | — | 104 | — | ns | 1 |
| t_{RP} | $\overline{\text{RAS}}$ Precharge Time | 30 | — | 40 | — | ns | |
| t_{CP} | $\overline{\text{CAS}}$ Precharge Time | 8 | — | 10 | — | ns | |
| t_{RAS} | $\overline{\text{RAS}}$ Pulse Width | 50 | 100k | 60 | 100k | ns | 1 |
| t_{CAS} | $\overline{\text{CAS}}$ Pulse Width | 8 | 100k | 10 | 100k | ns | 1 |
| t_{ASR} | Row Address Setup Time | 0 | — | 0 | — | ns | |
| t_{RAH} | Row Address Hold Time | 7 | — | 10 | — | ns | |
| t_{ASC} | Column Address Setup Time | 0 | — | 0 | — | ns | |
| t_{CAH} | Column Address Hold Time | 7 | — | 10 | — | ns | |
| t_{RCD} | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time | 11 | 37 | 14 | 45 | ns | 2 |
| t_{RAD} | $\overline{\text{RAS}}$ to Col. Address Delay Time | 9 | 25 | 12 | 30 | ns | 3 |
| t_{RSH} | $\overline{\text{RAS}}$ Hold Time | 8 | — | 10 | — | ns | |
| t_{CSH} | $\overline{\text{CAS}}$ Hold Time | 40 | — | 50 | — | ns | 1 |
| t_{CRP} | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 5 | — | 5 | — | ns | 1 |
| t_{DZO} | $\overline{\text{OE}}$ Delay Time From D_{IN} | 0 | — | 0 | — | ns | 4 |
| t_{DZC} | $\overline{\text{CAS}}$ Delay Time From D_{IN} | 0 | — | 0 | — | ns | 4 |
| t_T | Transition Time (Rise and Fall) | 1 | 50 | 1 | 50 | ns | 5 |

1. In a Test Mode Read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
3. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
4. Either t_{DZC} or t_{DZO} must be satisfied.
5. AC measurements assume $t_T = 2\text{ns}$.



Write Cycle

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|-----------|---|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{WCS} | Write Command Set Up Time | 0 | — | 0 | — | ns | 1 |
| t_{WCH} | Write Command Hold Time | 7 | — | 10 | — | ns | |
| t_{WP} | Write Command Pulse Width | 7 | — | 10 | — | ns | |
| t_{RWL} | Write Command to \overline{RAS} Lead Time | 8 | — | 10 | — | ns | |
| t_{CWL} | Write Command to \overline{CAS} Lead Time | 8 | — | 10 | — | ns | |
| t_{OED} | \overline{OE} to D_{IN} Delay Time | 13 | — | 15 | — | ns | 2 |
| t_{DS} | D_{IN} Setup Time | 0 | — | 0 | — | ns | 3 |
| t_{DH} | D_{IN} Hold Time | 7 | — | 10 | — | ns | 3 |

1. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}(\text{min.})$, the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}(\text{min.})$, $t_{CWD} \geq t_{CWD}(\text{min.})$, $t_{AWD} \geq t_{AWD}(\text{min.})$, and $t_{CPWD} \geq t_{CPWD}(\text{min.})$ (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
2. Either t_{CDD} or t_{OED} must be satisfied.
3. These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in Read-Modify-Write cycles.

Read Cycle

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|-----------|---|------|------|------|------|-------|------------|
| | | Min. | Max. | Min. | Max. | | |
| t_{RAC} | Access Time from \overline{RAS} | — | 50 | — | 60 | ns | 1, 2, 3, 5 |
| t_{CAC} | Access Time from \overline{CAS} | — | 13 | — | 15 | ns | 1, 2, 5 |
| t_{AA} | Access Time from Address | — | 25 | — | 30 | ns | 1, 2, 5 |
| t_{OEA} | Access Time From \overline{OE} | — | 13 | — | 15 | ns | 1, 5 |
| t_{RCS} | Read Command Setup Time | 0 | — | 0 | — | ns | |
| t_{RCH} | Read Command Hold Time to \overline{CAS} | 0 | — | 0 | — | ns | 6 |
| t_{RRH} | Read Command Hold Time to \overline{RAS} | 0 | — | 0 | — | ns | |
| t_{RAL} | Column Address to \overline{RAS} Lead Time | 25 | — | 30 | — | ns | 1 |
| t_{CLZ} | \overline{CAS} to Output in Low-Z | 0 | — | 0 | — | ns | 5 |
| t_{OEZ} | Output Buffer Turn-Off Delay From \overline{OE} | 0 | 13 | 0 | 15 | ns | 7 |
| t_{CDD} | \overline{CAS} to D_{IN} Delay Time | 13 | — | 15 | — | ns | 4 |
| t_{OFF} | Output Buffer Turn-Off Delay | 0 | 13 | 0 | 15 | ns | 7 |
| t_{OES} | \overline{OE} Setup Time Prior to \overline{CAS} | 5 | — | 5 | — | ns | |
| t_{ORD} | \overline{OE} Setup Time Prior to \overline{RAS} (Hidden Refresh) | 0 | — | 0 | — | ns | |

1. In a Test Mode Read cycle, the value of t_{RAC} , t_{AA} , t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the $t_{RCD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RCD}(\text{max.})$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\text{max.})$ limit, then access time is controlled by t_{CAC} .
3. Operation within the $t_{RAD}(\text{max.})$ limit ensures that $t_{RAC}(\text{max.})$ can be met. $t_{RAD}(\text{max.})$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\text{max.})$ limit, then access time is controlled by t_{AA} .
4. Either t_{CDD} or t_{OED} must be satisfied.
5. Measured with the specified current load and 100pF.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. $t_{OFF}(\text{max.})$ and $t_{OEZ}(\text{max.})$ define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

Read-Modify-Write Cycle

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|------------------|---|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{RWC} | Read-Modify-Write Cycle Time | 109 | — | 135 | — | ns | |
| t_{RWD} | RAS to WE Delay Time | 65 | — | 79 | — | ns | 1 |
| t_{CWD} | CAS to WE Delay Time | 28 | — | 34 | — | ns | 1 |
| t_{AWD} | Column Address to $\overline{\text{WE}}$ Delay Time | 40 | — | 49 | — | ns | 1 |
| t_{OEH} | $\overline{\text{OE}}$ Command Hold Time | 7 | — | 10 | — | ns | |

1. t_{WCS} , t_{RWD} , t_{CWD} , t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min.})$, the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min.})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min.})$, $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min.})$, and $t_{\text{CPWD}} \geq t_{\text{CPWD}}(\text{min.})$ (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

Extended Data Out (Hyper Page) Mode Cycle

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|--------------------|--|------|------|------|------|-------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{HCAS} | CAS Pulse Width (Hyper Page Mode) | 8 | 100K | 10 | 10K | ns | |
| t_{HPC} | Hyper Page Mode Cycle Time (Read/Write) | 20 | — | 25 | — | ns | |
| t_{HPRWC} | Hyper Page Mode Read Modify Write Cycle Time | 54 | — | 66 | — | ns | |
| t_{DOH} | Data-out Hold Time from CAS | 5 | — | 5 | — | ns | |
| t_{WHZ} | Output buffer Turn-Off Delay from $\overline{\text{WE}}$ | 0 | 10 | 0 | 10 | ns | |
| t_{WPZ} | $\overline{\text{WE}}$ Pulse Width to Output Disable at $\overline{\text{CAS}}$ High | 7 | — | 10 | — | ns | |
| t_{CPRH} | RAS Hold Time from $\overline{\text{CAS}}$ Precharge | 27 | — | 35 | — | ns | |
| t_{CPA} | Access Time from $\overline{\text{CAS}}$ Precharge | — | 27 | — | 35 | ns | 1 |
| t_{RASP} | Hyper Page Mode RAS Pulse Width | 50 | 200K | 60 | 200K | ns | |
| t_{OEP} | $\overline{\text{OE}}$ High Pulse Width | 5 | — | 10 | — | ns | |
| t_{OEHC} | $\overline{\text{OE}}$ High Hold Time from $\overline{\text{CAS}}$ High | 5 | — | 10 | — | ns | |

1. Measured with the specified current load and 100pF at $V_{\text{OL}} = 0.8\text{V}$ and $V_{\text{OH}} = 2.0\text{V}$.

Self Refresh Cycle - Low Power Version Only

| Symbol | Parameter | -50 | | -60 | | Units | Notes |
|---|---|------|------|------|------|---------------|-------|
| | | Min. | Max. | Min. | Max. | | |
| t_{RASS} | RAS Pulse Width During Self Refresh Cycle | 100 | — | 100 | — | μs | 1 |
| t_{RPS} | RAS Precharge Time During Self Refresh Cycle | 84 | — | 104 | — | ns | 1 |
| t_{CHS} | CAS Hold Time During Self Refresh Cycle | -50 | — | -50 | — | ns | 1 |
| 1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in an EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR- Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh. | | | | | | | |

Refresh Cycle

| Symbol | Parameter | | -50 | | -60 | | Units | Notes |
|---|--|------------|------|------|------|------|-------|-------|
| | | | Min. | Max. | Min. | Max. | | |
| t _{CSR} | CAS Setup Time (CAS before RAS Refresh Cycle) | | 5 | — | 5 | — | ns | |
| t _{CHR} | CAS Hold Time (CAS before RAS Refresh Cycle) | | 5 | — | 10 | — | ns | |
| t _{WRP} | WE Setup Time (CAS before RAS Refresh Cycle) | | 5 | — | 10 | — | ns | |
| t _{WRH} | WE Hold Time (CAS before RAS Refresh Cycle) | | 5 | — | 10 | — | ns | |
| t _{RPC} | RAS Precharge to CAS Hold Time | | 5 | — | 5 | — | ns | |
| t _{REF} | Refresh Period | SP version | — | 64 | — | 64 | ms | 1 |
| | | LP version | — | 128 | — | 128 | | |
| 1. 8192 cycles for RAS Only Refresh; 4096 cycles for CBR Refresh. | | | | | | | | |

The diagram illustrates the timing relationships between several digital signals during memory access operations:

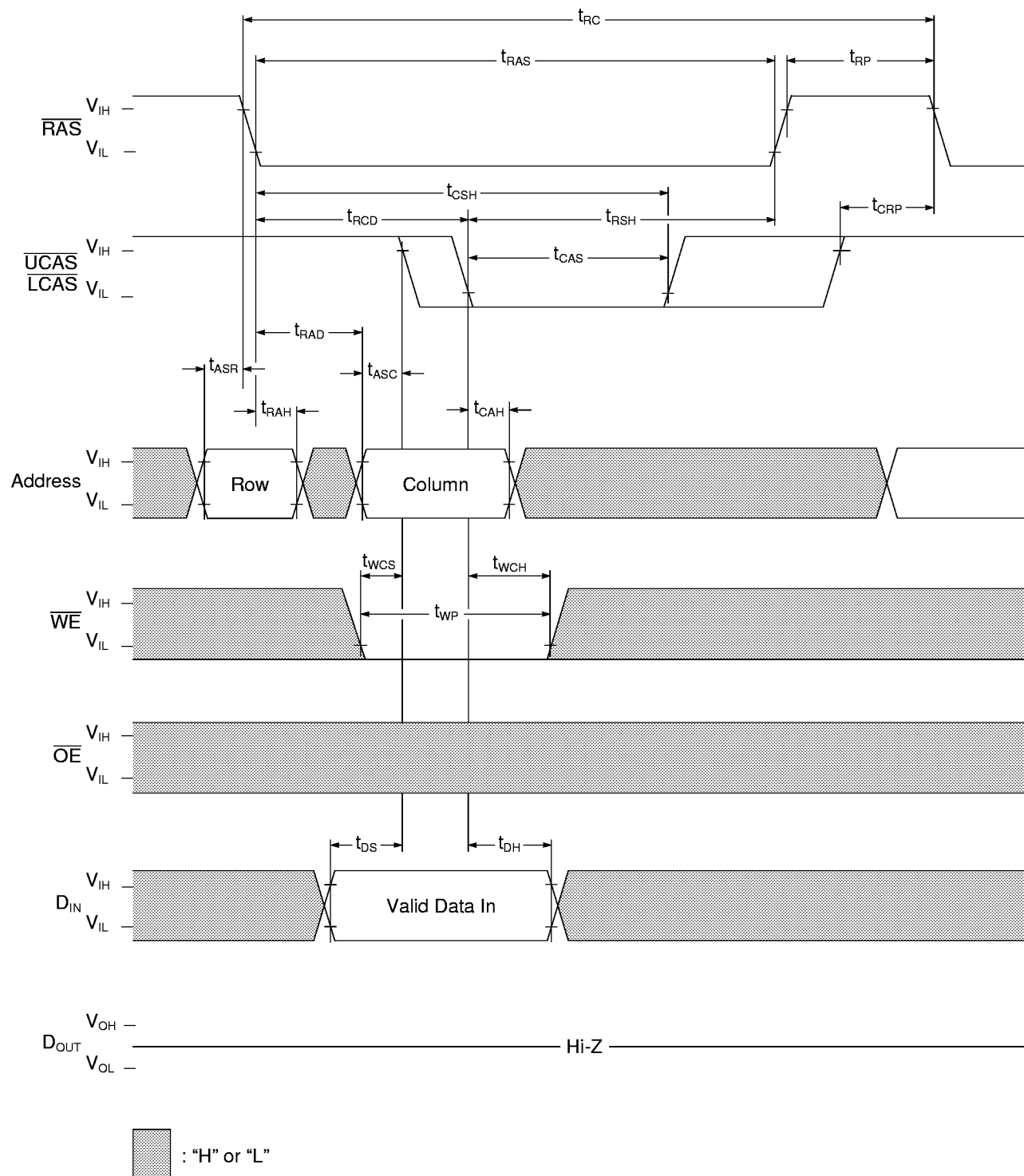
- RAS**: Row Address Strobe signal.
- UCAS / LCAS**: Column Address Strobe / Local Column Address Strobe signal.
- Address**: Memory address bus, divided into Row and Column phases.
- WE**: Write Enable signal.
- OE**: Output Enable signal.
- D_{IN}**: Data Input signal.
- D_{OUT}**: Data Output signal, shown as Valid Data Out.

Key timing parameters labeled include:

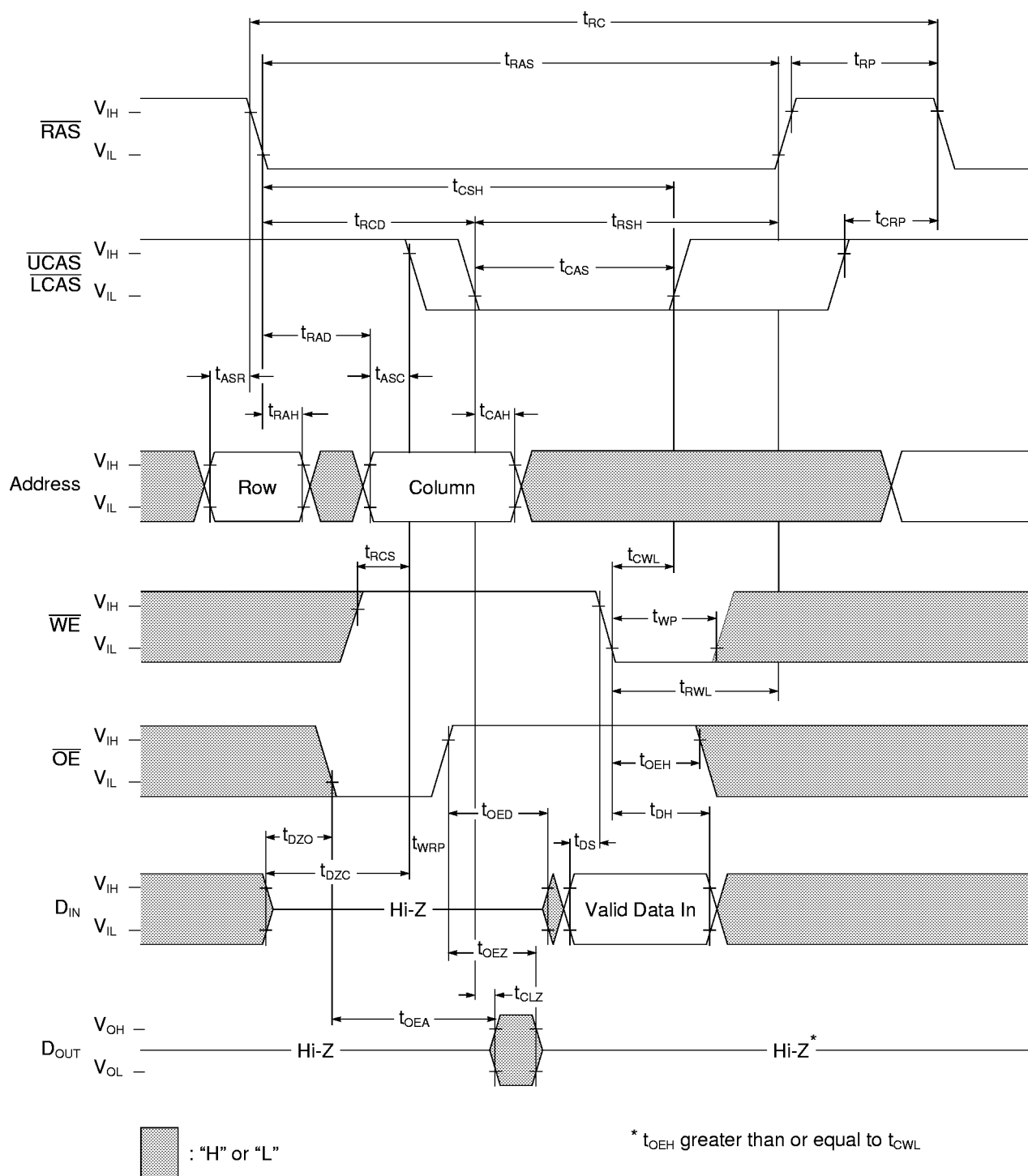
- t_{RC} , t_{RAS} , t_{RP}
- t_{CSH} , t_{RCD} , t_{RSH} , t_{CRP}
- t_{CAS} , t_{RAD} , t_{RAL}
- t_{ASR} , t_{RAH} , t_{ASC} , t_{CAH}
- t_{RCH} , t_{RRH}
- t_{AA} , t_{OES} , t_{OEZ}
- t_{DZO} , t_{CAC} , t_{CLZ}
- t_{DZC} , t_{OFF} , t_{OD}
- t_{CDD} , t_{OEZ}
- t_{RAC}

A legend indicates that shaded areas represent "H": or "L".

Write Cycle (Early Write)



Write Cycle (Delayed Write)



The diagram illustrates the timing relationships for a 2D array memory access sequence. The signals shown are:

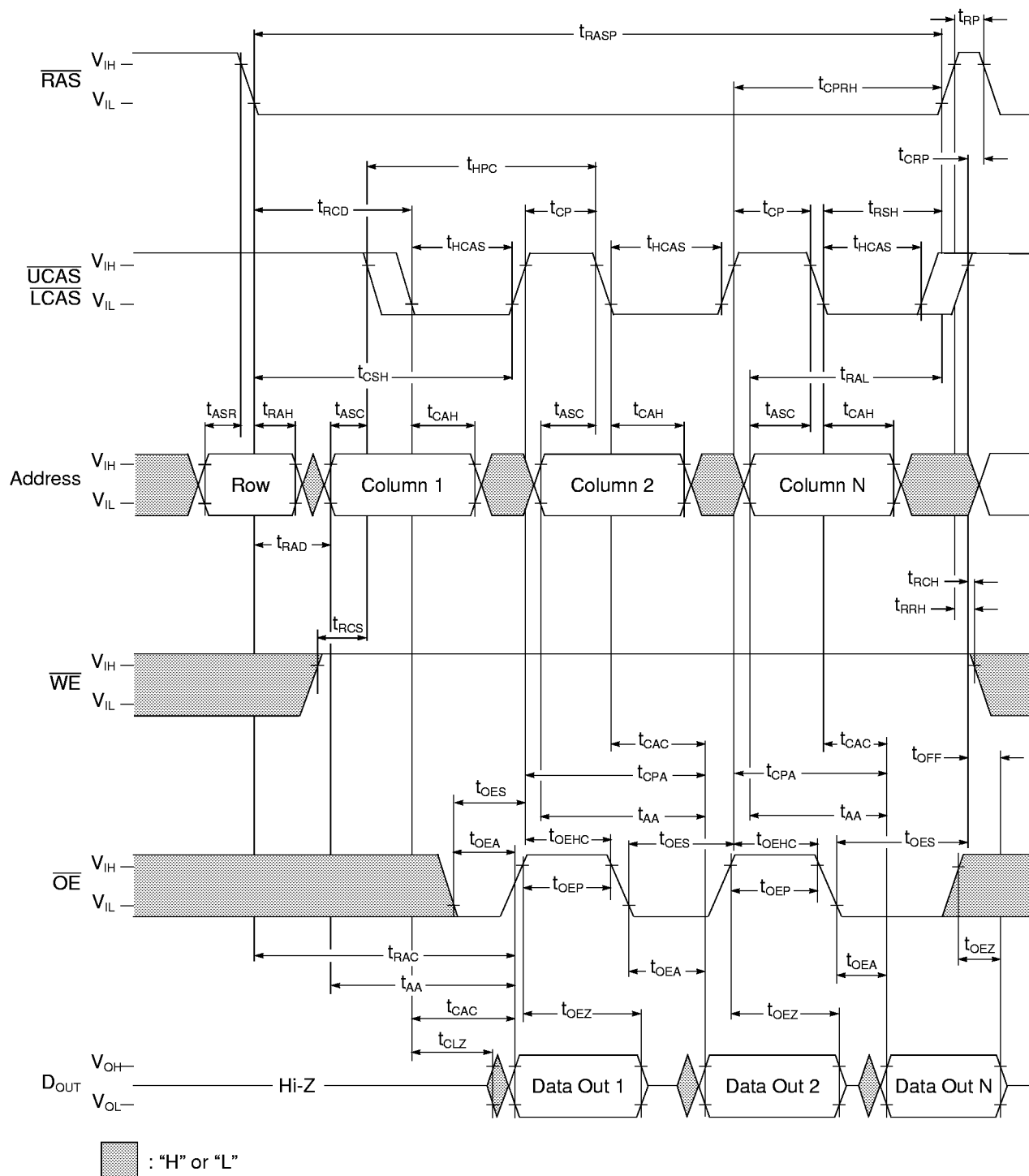
- $\overline{\text{RAS}}$** : Row Address Strobe, active low.
- $\overline{\text{UCAS/LCAS}}$** : Column Address Strobe/Latch Enable, active low.
- Address**: The address bus, showing the sequence of Row, Column 1, Column 2, and Column N.
- $\overline{\text{WE}}$** : Write Enable, active low.
- $\overline{\text{OE}}$** : Output Enable, active low.
- D_{OUT}** : Data bus, showing Data Out 1, Data Out 2, and Data Out N.

Key timing parameters are indicated by arrows:

- t_{RASP} : Row Address Strobe pulse width.
- t_{CPRH} : Column Address Strobe pulse width.
- t_{CRP} : Column Address Strobe pulse delay.
- t_{HPC} : Horizontal Period.
- t_{RCD} : Row to Column Delay.
- t_{HCAS} : Horizontal Column Address Strobe.
- t_{CP} : Column Period.
- t_{RSH} : Row to Column Delay.
- t_{CSH} : Column Strobe Hold.
- t_{ASC} : Address to Column Delay.
- t_{CAH} : Column Address Hold.
- t_{ASR} : Address to Row Delay.
- t_{RAH} : Row Address Hold.
- t_{RAD} : Row Address Delay.
- t_{RCS} : Row to Column Delay.
- t_{CAC} : Column Address to Column Address Delay.
- t_{CPA} : Column Period to Column Address Delay.
- t_{AA} : Address to Address Delay.
- t_{OES} : Output Enable to Output Delay.
- t_{OEA} : Output Enable to Address Delay.
- t_{RAC} : Row Address to Row Address Delay.
- t_{AA} : Address to Address Delay.
- t_{CLZ} : Column Latch to Column Address Delay.
- t_{DOH} : Data Output Hold.
- t_{OEZ} : Output Enable to Output Delay.
- t_{RCH} : Row to Column Delay.
- t_{RRH} : Row to Row Delay.
- t_{WP} : Write Pulse.
- t_{OFF} : Output Delay.

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EDO (Hyper Page) Mode Read Cycle ($\overline{\text{OE}}$ Control)



The diagram illustrates the timing relationships for a memory device. The signals shown are:

- RAS**: Row Address Strobe, with levels V_{IH} and V_{IL} .
- UCAS/LCAS**: Column Address Strobe/Latch Enable, with levels V_{IH} and V_{IL} .
- Address**: Row and Column addresses, with levels V_{IH} and V_{IL} .
- WE**: Write Enable, with levels V_{IH} and V_{IL} .
- OE**: Output Enable, with levels V_{IH} and V_{IL} .
- Data Out**: Data bus output, with levels V_{OH} and V_{OL} .

The diagram shows the sequence of operations for reading and writing data. Key timing parameters are indicated by arrows:

- t_{RASP} : RAS pulse width.
- t_{CPRH} : UCAS/LCAS pulse width.
- t_{CRP} : UCAS/LCAS setup time before RAS.
- t_{RCD} : RAS to column address delay.
- t_{HPC} : RAS to column address delay.
- t_{CP} : Column address pulse width.
- t_{HCAS} : Column address setup and hold times.
- t_{CSH} : Column address setup and hold times.
- t_{ASC} : Column address setup and hold times.
- t_{CAH} : Column address hold times.
- t_{RAD} : Row address delay.
- t_{RCH} : Row address delay.
- t_{RCS} : Row address delay.
- t_{WPHZ} : Write Enable pulse width.
- t_{CAC} : Column address delay.
- t_{CPA} : Column address delay.
- t_{OEZ} : Output Enable delay.
- t_{WHZ} : Write Enable delay.
- t_{CLZ} : Column address delay.
- t_{RAC} : Row address delay.
- t_{AA} : Address delay.
- t_{OES} : Output Enable delay.
- t_{OEZ} : Output Enable delay.
- t_{OFF} : Output Enable delay.

Legend: V_{IH} : "H" or "L"

The diagram illustrates the timing relationships between several control and data signals during memory access operations. The signals shown are:

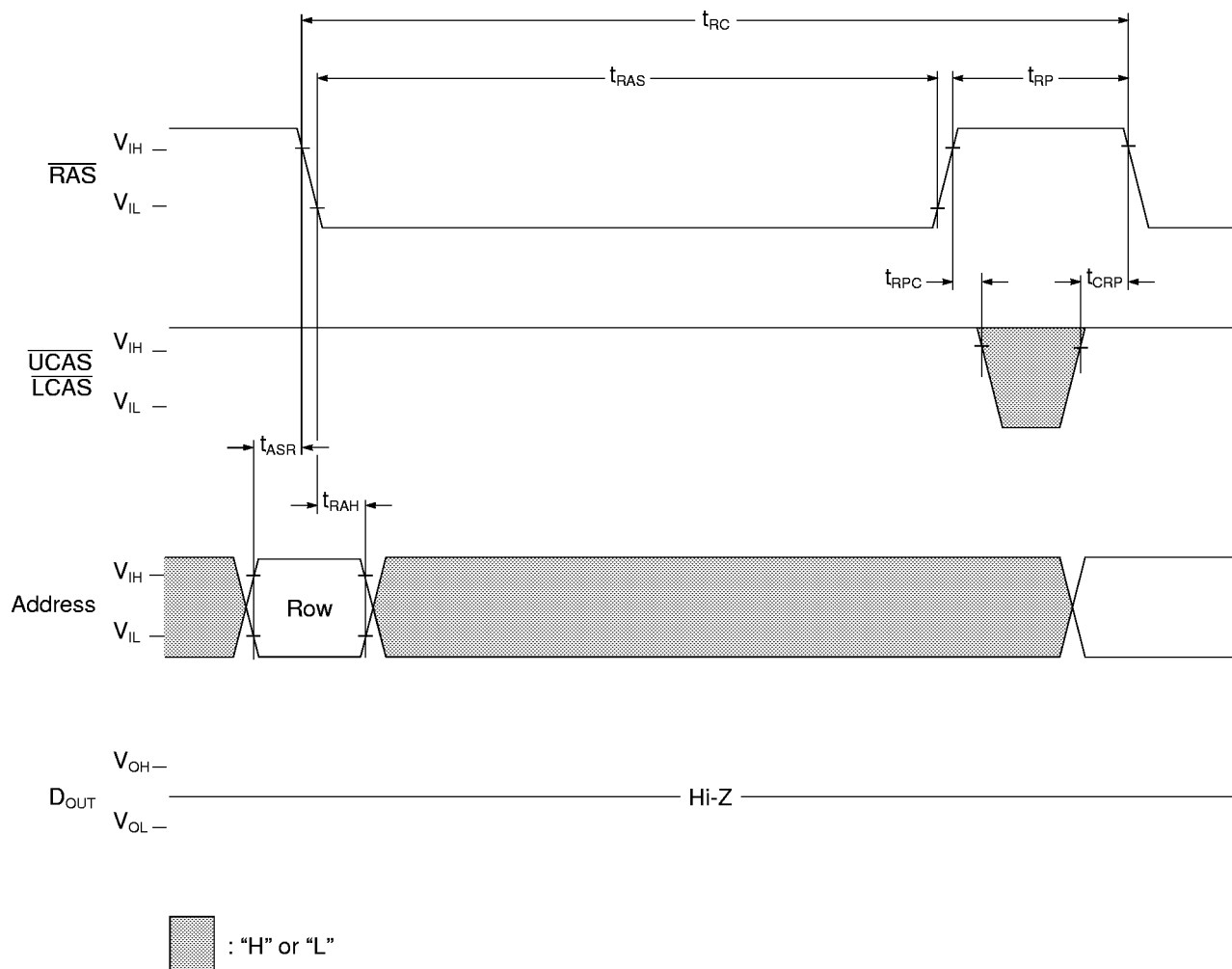
- RAS**: Row Address Strobe, active low.
- UCAS/LCAS**: Column Address Strobe / Local Column Address Strobe, active low.
- Address**: Memory address bus, showing Row, Column 1, Column 2, ..., Column N.
- WE**: Write Enable, active low.
- OE**: Output Enable, active low.
- D_{IN}**: Data Input bus, showing Hi-Z (High Impedance) and Data In 1, Data In 2, ..., Data In N.

Key timing parameters indicated by arrows include:

- t_{RASP} : RAS pulse width.
- t_{RCD} : RAS-to-Column Delay.
- t_{HPC} : Horizontal Pulse Width.
- t_{CP} : Column Pulse Width.
- t_{CRP} : Column Refresh Pulse Width.
- t_{HCAS} : Horizontal Column Address Strobe.
- t_{RAD} : Row Address Delay.
- t_{CSH} : Column Strobe Hold.
- t_{ASC} : Address Setup.
- t_{CAH} : Column Address Hold.
- t_{ASR} : Address Setup before RAS.
- t_{RAH} : Row Address Hold.
- t_{CWL} : Column Write Latency.
- t_{RCS} : Row to Column Setup.
- t_{WP} : Write Pulse Width.
- t_{OEH} : Output Enable Hold.
- t_{DSD} : Data Setup before Data In.
- t_{DH} : Data Hold after Data In.
- t_{OED} : Output Enable Delay.

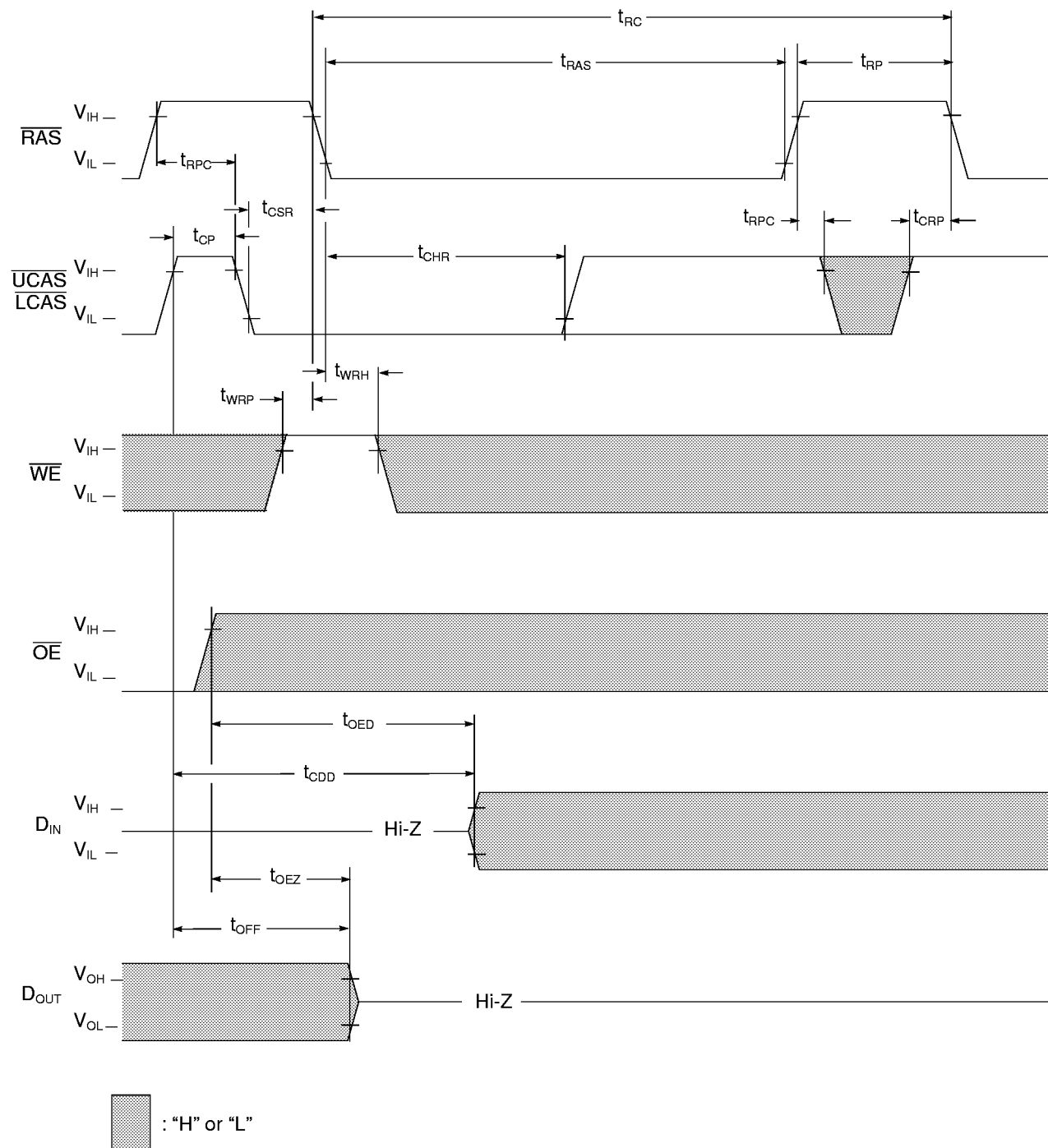
A legend at the bottom indicates that shaded areas represent "H" or "L" levels.

RAS Only Refresh Cycle



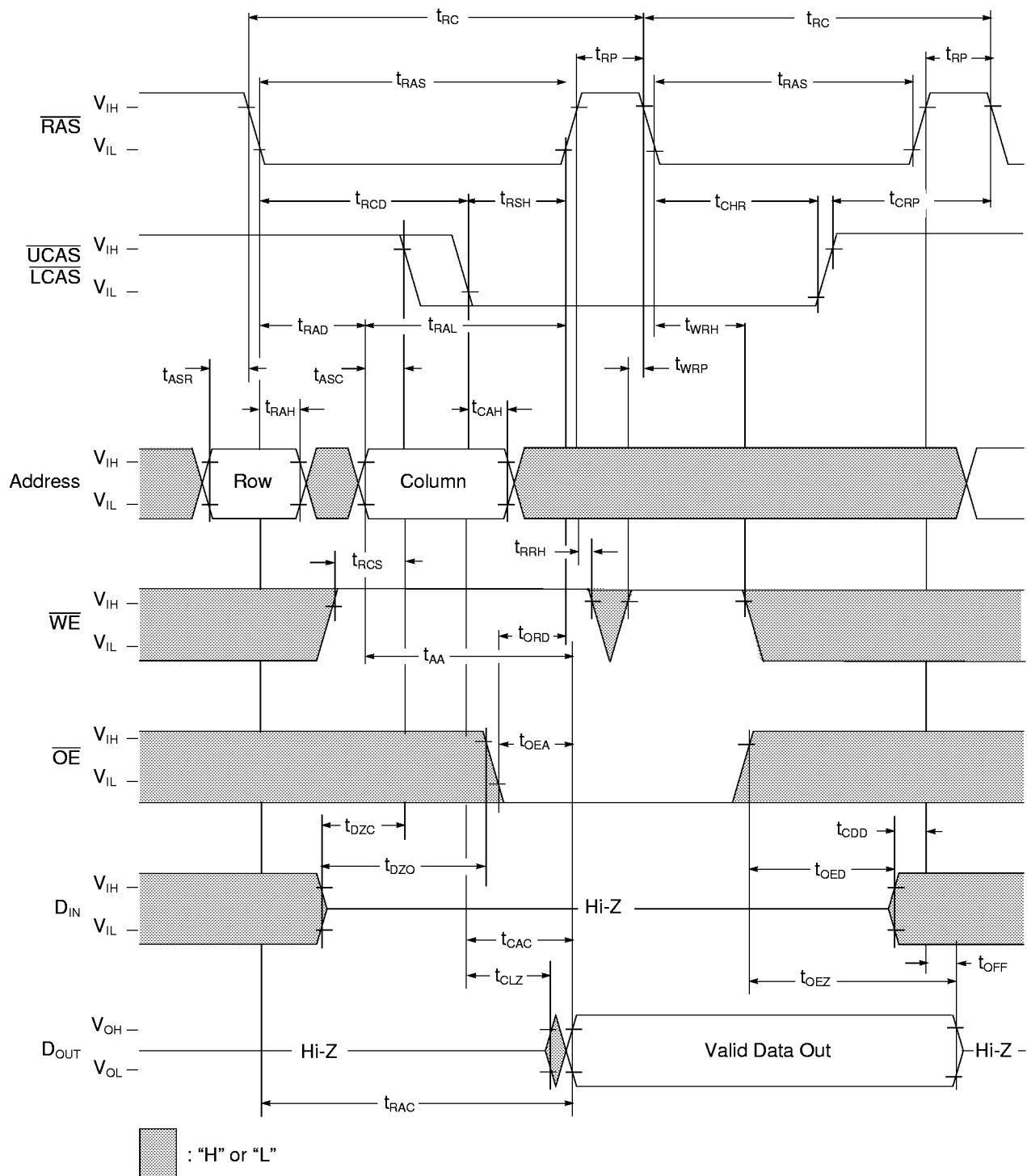
NOTE: \overline{WE} , \overline{OE} and D_{IN} are "H" or "L"

CAS Before RAS Refresh Cycle

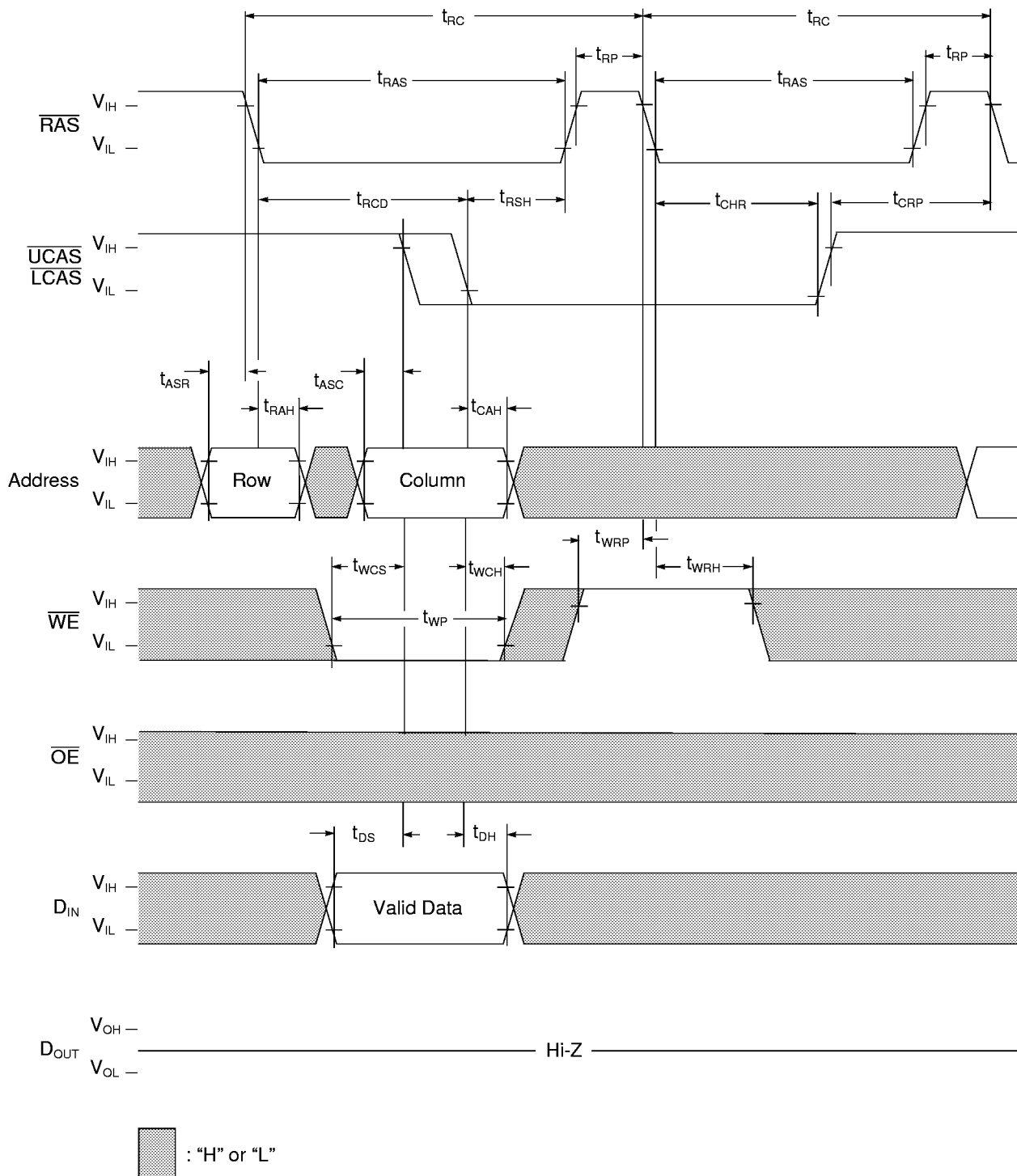


NOTE: Address is "H" or "L"

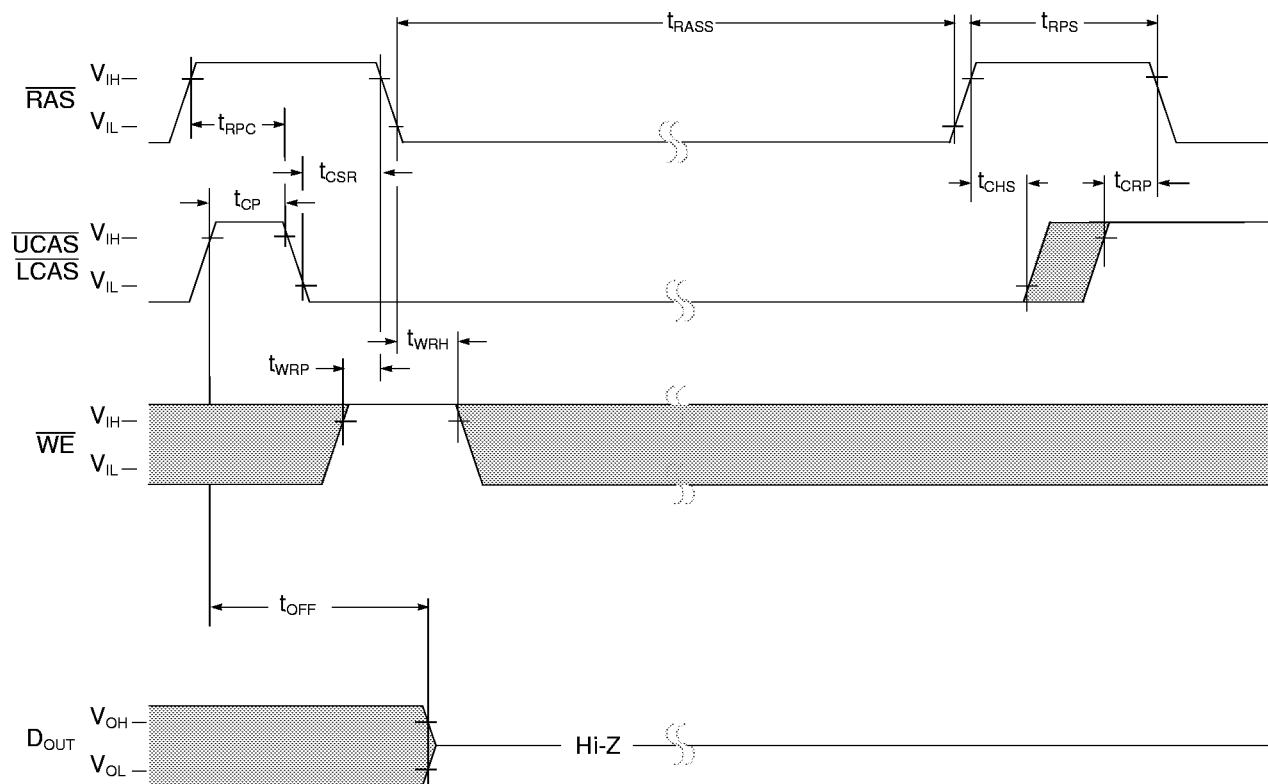
Hidden Refresh Cycle (Read)




Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode) - Low Power version only

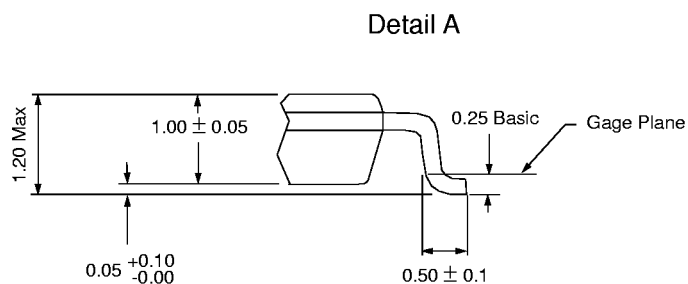
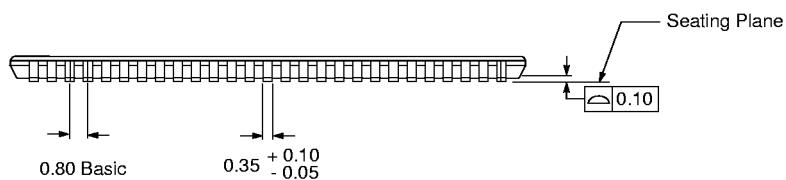
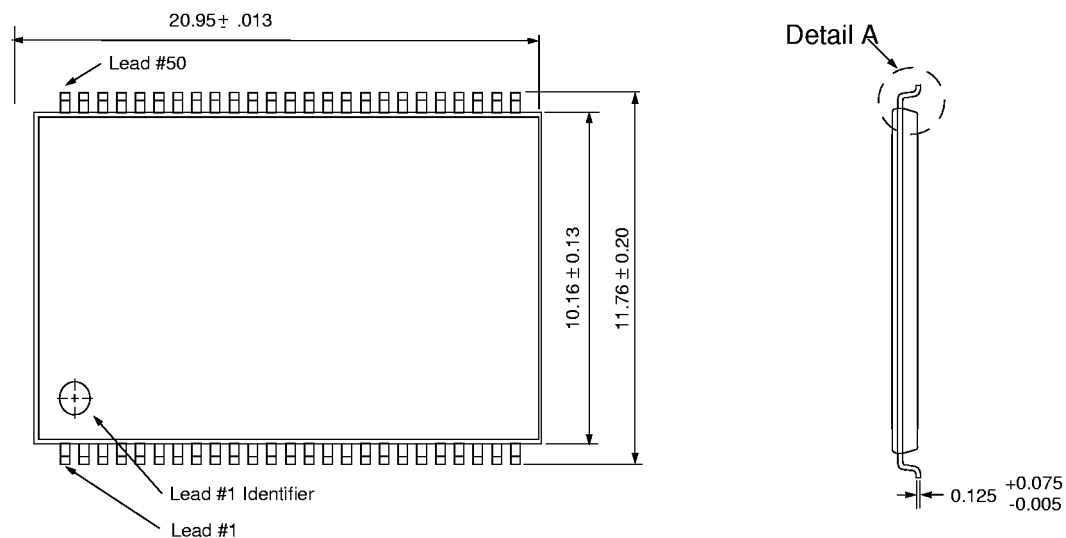


 : "H" or "L"

NOTE: Address and OE are "H" or "L"

Once t_{RASS} (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

Package Dimensions (400mil; 50 lead; Thin Small Outline Package)



NOTE: All dimensions are in millimeters. Reference JEDEC Standard MS-024



Revision Log

| Revision | Contents of Modification |
|----------|--|
| 1/2/97 | Initial specification release. |
| 03/19/97 | <ol style="list-style-type: none">1. \overline{WE} for the Hidden Refresh Write cycle in the Truth Table was changed from "H" to "L→H".2. t_{OED} was moved from the Common Parameters table to the Write Cycle Parameters Table.3. The note "Implementing \overline{WE} at \overline{RAS} time during a Read or Write cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs." was removed from all of the Read and Write timing diagrams.4. t_{ODD} was changed to t_{OED} in notes in the Write Cycle and Read Cycle Parameters tables.5. "Hyper Page Mode" was changed to "EDO (Hyper Page) Mode" in the timing diagram titles.6. Removed the Test Mode parameters and timing diagrams.7. LVTTTL/LVCMOS changed to TTL/CMOS.8. LVCMOS currents were removed.9. Power numbers on the spec cover were recalculated. |
| 11/97 | <ol style="list-style-type: none">1. Changed Retention Time from 256ms to 128ms on Low Power DRAMs. |



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