16M x 4 12/12 DRAM

Features

- 16,777,216 word by 4 bit organization
- Single 3.3 ± 0.3V power supply
- Fast Page Mode
- $\overline{CAS}$ before $\overline{RAS}$ Refresh
  - 4096 cycles/Retention Time
- $\overline{RAS}$ only Refresh
  - 4096 cycles/Retention Time
- 64ms Standard Power (SP) Retention Time
- Hidden Refresh
- Read-Modify-Write
- Performance:

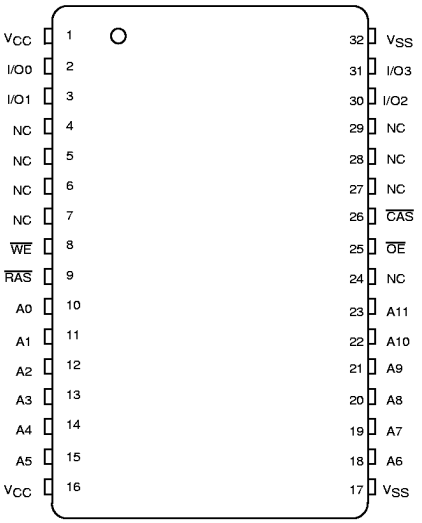
		-50	-60
t_{RAC}	$\overline{RAS}$ Access Time	50ns	60ns
t_{CAC}	$\overline{CAS}$ Access Time	13ns	15ns
t_{AA}	Column Address Access Time	25ns	30ns
t_{RC}	Cycle Time	90ns	110ns
t_{PC}	Fast Page Mode Cycle Time	35ns	40ns

- Max. Power Dissipation (-50)
  - Active: 522mW
  - Standby (SP version): 2.0 mA
- Package: SOJ-32(400mil), TSOP-32(400mil)

Description

The IBM0165400B is a dynamic RAM organized 16,777,216 words by 4 bits. This device is fabricated in IBM's most advanced CMOS silicon gate process technology. The circuit and process design allow this DRAM to achieve high performance and low power dissipation. The IBM0165400B operates with a single 3.3 ± 0.3V power supply, and interfaces directly with either TTL or CMOS levels. The 24 addresses required to access any bit of data are multiplexed (12 are strobed with $\overline{RAS}$, 12 are strobed with $\overline{CAS}$). They are packaged in a 32 pin plastic SOJ (400mil×825mil), and a 32 pin plastic TSOP type II (400mil×825mil).

Pin Assignments (Top View)



Pin Description

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A11	Address Inputs
$\overline{OE}$	Output Enable
I/O0 - I/O3	Data Input/output
V_{CC}	Power (+3.3V)
V_{SS}	Ground

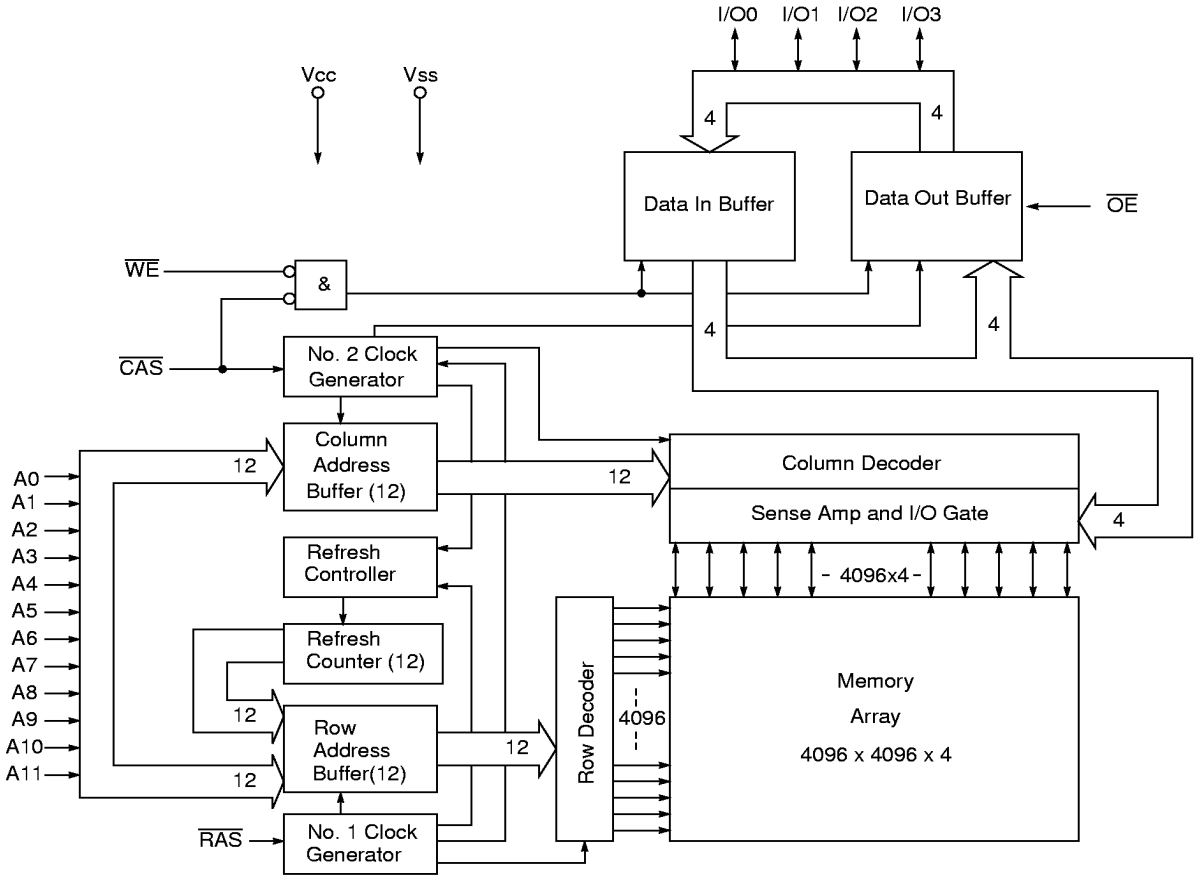
88H2005
GA15-5142-00
Revised 4/97

Ordering Information

Part Number	Power	Self Refresh	Power Supply	Speed	Package	Notes
IBM0165400BJ3-50	SP	No	3.3V	50ns	400mil SOJ 32	1
IBM0165400BJ3-60	SP	No	3.3V	60ns	400mil SOJ 32	1
IBM0165400BT3-50	SP	No	3.3V	50ns	400mil TSOP 32	1
IBM0165400BT3-60	SP	No	3.3V	60ns	400mil TSOP 32	1

1. SP = Standard Power version

Block Diagram



Truth Table

Function		$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	$\overline{OE}$	Row Address	Column Address	I/O0 - I/O3
Standby		H	H→X	X	X	X	X	High Impedance
Read		L	L	H	L	Row	Col.	Data Out
Early-Write		L	L	L	X	Row	Col.	Data In
Delayed-Write		L	L	H→L	H	Row	Col.	Data In
Read-Modify-Write		L	L	H→L	L→H	Row	Col.	Data Out, Data In
Fast Page Mode Read	1st Cycle	L	H→L	H	L	Row	Col.	Data Out
	2nd Cycle	L	H→L	H	L	N/A	Col.	Data Out
Fast Page Mode Write	1st Cycle	L	H→L	L	X	Row	Col.	Data In
	2nd Cycle	L	H→L	L	X	N/A	Col.	Data In
Fast Page Mode Read-Modify-Write	1st Cycle	L	H→L	H→L	L→H	Row	Col.	Data Out, Data In
	2nd Cycle	L	H→L	H→L	L→H	N/A	Col.	Data Out, Data In
$\overline{RAS}$-Only Refresh		L	H	X	X	Row	N/A	High Impedance
$\overline{CAS}$-Before-$\overline{RAS}$ Refresh		H→L	L	H	X	X	N/A	High Impedance
Hidden Refresh	Read	L→H→L	L	H	L	Row	Col.	Data Out
	Write	L→H→L	L	L→H	X	Row	Col.	Data In

Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Notes
V_{CC}	Power Supply Voltage	-0.5 to 4.6	V	1
V_{IN}	Input Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	V	1
V_{OUT}	Output Voltage	-0.5 to min (V_{CC}+0.5, 4.6)	V	1
T_{OPR}	Operating Temperature	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	°C	1
P_D	Power Dissipation	1.0	W	1
I_{OUT}	Short Circuit Output Current	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1,2
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1,2

1. All voltages referenced to V_{SS}.
2. V_{IH} may overshoot to V_{CC} + 2.0V for pulse widths of ≤ 4.0ns with 3.3 Volt. V_{IL} may undershoot to -2.0V for pulse widths ≤ 4.0ns with 3.3 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference

Capacitance (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V, f=1MHz)

Symbol	Parameter	Min.	Max.	Units	Notes
C_{I1}	Input Capacitance (A0 - A11)	—	5	pF	
C_{I2}	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$)	—	7	pF	
C_{I3}	Data I/O Capacitance (I/O0 - I/O3)	—	7	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 ± 0.3V)

Symbol	Parameter		Min.	Max.	Units	Notes
I_{CC1}	Operating Current Average Power Supply Operating Current ($\overline{RAS}$, $\overline{CAS}$, Address Cycling: t_{RC} = t_{RC} min)	-50	—	145	mA	1, 2, 3
		-60	—	130		
I_{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH})		—	2	mA	
I_{CC3}	$\overline{RAS}$ Only Refresh Current Average Power Supply Current, $\overline{RAS}$ Only Mode ($\overline{RAS}$ Cycling, $\overline{CAS}$ = V_{IH}: t_{RC} = t_{RC} min)	-50	—	135	mA	1, 3
		-60	—	110		
I_{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{RAS}$ = V_{IL}, $\overline{CAS}$, Address Cycling: t_{PC} = t_{PC} min)	-50	—	60	mA	1, 2, 3
		-60	—	50		
I_{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} - 0.2V)	SP version	—	900	µA	
I_{CC6}	$\overline{CAS}$ Before $\overline{RAS}$ Refresh Current Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode ($\overline{RAS}$, $\overline{CAS}$, Cycling: t_{RC} = t_{RC} min)	-50	—	145	mA	1, 2
		-60	—	120		
$I_{I(L)}$	Input Leakage Current Input Leakage Current, any input (0.0 ≥ V_{IN} ≥ V_{CC}), All Other Pins Not Under Test = 0V		-2	+2	µA	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0 ≥ V_{OUT} ≥ V_{CC})		-2	+2	µA	
V_{OH}	Output High Level (TTL) Output "H" Level Voltage (I_{OUT} = -2mA)		2.4	—	V	
V_{OL}	Output Low Level (TTL) Output "L" Level Voltage (I_{OUT} = +2mA)		—	0.4	V	

1. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
2. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
3. Column address can be changed once or less while $\overline{RAS}$ =V_{IL} and $\overline{CAS}$ =V_{IH}.

AC Characteristics (T_A=0 to +70°C, V_{CC}=3.3 ± 0.3V)

1. An initial pause of 100µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume t_T=5ns.
3. V_{IH}(min.) and V_{IL}(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL}.
4. Valid column addresses are only A0 through A11.

Read, Write, Read-Modify-Write and Refresh Cycle (Common Parameters)

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RC}	Random Read or Write Cycle Time	90	—	110	—	ns	1
t_{RP}	$\overline{RAS}$ Precharge Time	30	—	40	—	ns	
t_{CP}	$\overline{CAS}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	50	100k	60	100k	ns	1
t_{CAS}	$\overline{CAS}$ Pulse Width	13	100k	15	100k	ns	1
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	7	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	7	—	10	—	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	17	37	20	45	ns	2
t_{RAD}	$\overline{RAS}$ to Col. Address Delay Time	12	25	15	30	ns	3
t_{RSH}	$\overline{RAS}$ Hold Time	13	—	15	—	ns	
t_{CSH}	$\overline{CAS}$ Hold Time	50	—	60	—	ns	1
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5	—	5	—	ns	1
t_{DZO}	$\overline{OE}$ Delay Time From D_{IN}	0	—	0	—	ns	4
t_{DZC}	$\overline{CAS}$ Delay Time From D_{IN}	0	—	0	—	ns	4
t_T	Transition Time (Rise and Fall)	3	50	3	50	ns	6

1. In a Test Mode Read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
4. Either t_{DZC} or t_{DZO} must be satisfied.
5. AC measurements assume t_T=5ns

Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	1
t_{WCH}	Write Command Hold Time	7	—	10	—	ns	
t_{WP}	Write Command Pulse Width	7	—	10	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	13	—	15	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	13	—	15	—	ns	
t_{OED}	$\overline{OE}$ to D_{IN} Delay Time	13	—	15	—	ns	2
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	3
t_{DH}	D_{IN} Hold Time	7	—	10	—	ns	3

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
2. Either t_{CDD} or t_{OED} must be satisfied.
3. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in Read-Modify-Write cycles.

Read Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RAC}	Access Time from $\overline{RAS}$	—	50	—	60	ns	1, 2, 3, 5
t_{CAC}	Access Time from $\overline{CAS}$	—	13	—	15	ns	1, 2, 5
t_{AA}	Access Time from Address	—	25	—	30	ns	1, 2, 5
t_{OEA}	Access Time From $\overline{OE}$	—	13	—	15	ns	1, 5
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	6
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	0	—	0	—	ns	
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	25	—	30	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	25	—	30	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	5
t_{OEZ}	Output Buffer Turn-Off Delay From $\overline{OE}$	0	13	0	15	ns	7
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	13	—	15	—	ns	4
t_{OFF}	Output Buffer Turn-Off Delay	0	13	—	15	ns	7

1. In a Test Mode Read cycle, the value of t_{RAC}, t_{AA}, t_{CAC} and t_{CPA} are delayed by 5ns from the specified value. These parameters must be adjusted in Test Mode cycles by adding 5ns to the specified value. Associated timings must also be adjusted by 5ns.
2. Operation within the t_{RCD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RCD}(max.) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD}(max.) limit, then access time is controlled by t_{CAC}.
3. Operation within the t_{RAD}(max.) limit ensures that t_{RAC}(max.) can be met. t_{RAD}(max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD}(max.) limit, then access time is controlled by t_{AA}.
4. Either t_{CDD} or t_{OED} must be satisfied.
5. Measured with the specified current load and 100pF.
6. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
7. t_{OFF}(max.) and t_{OEZ}(max.) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

Read-Modify-Write Cycle

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{RWC}	Read-Modify-Write Cycle Time	126	—	150	—	ns	
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay Time	68	—	80	—	ns	1
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay Time	31	—	35	—	ns	1
t_{AWD}	Column Address to $\overline{WE}$ Delay Time	43	—	50	—	ns	1
t_{OEH}	$\overline{OE}$ Command Hold Time	7	—	15	—	ns	

1. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$(min.), the cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle. If $t_{RWD} \geq t_{RWD}$(min.), $t_{CWD} \geq t_{CWD}$(min.), $t_{AWD} \geq t_{AWD}$(min.), and $t_{CPWD} \geq t_{CPWD}$(min.)(Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

Fast Page Mode Cycle (Includes Read-Modify-Write)

Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{PC}	Fast Page Mode Cycle Time (Read/Write)	35	—	40	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	50	200K	60	200k	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	28	—	35	ns	1
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	30	—	35	—	ns	
t_{PRWC}	Fast Page Mode Read Modify Write Cycle Time	69	—	80	—	ns	
t_{CPW}	$\overline{WE}$ Delay Time from $\overline{CAS}$ Precharge	43	—	55	—	ns	

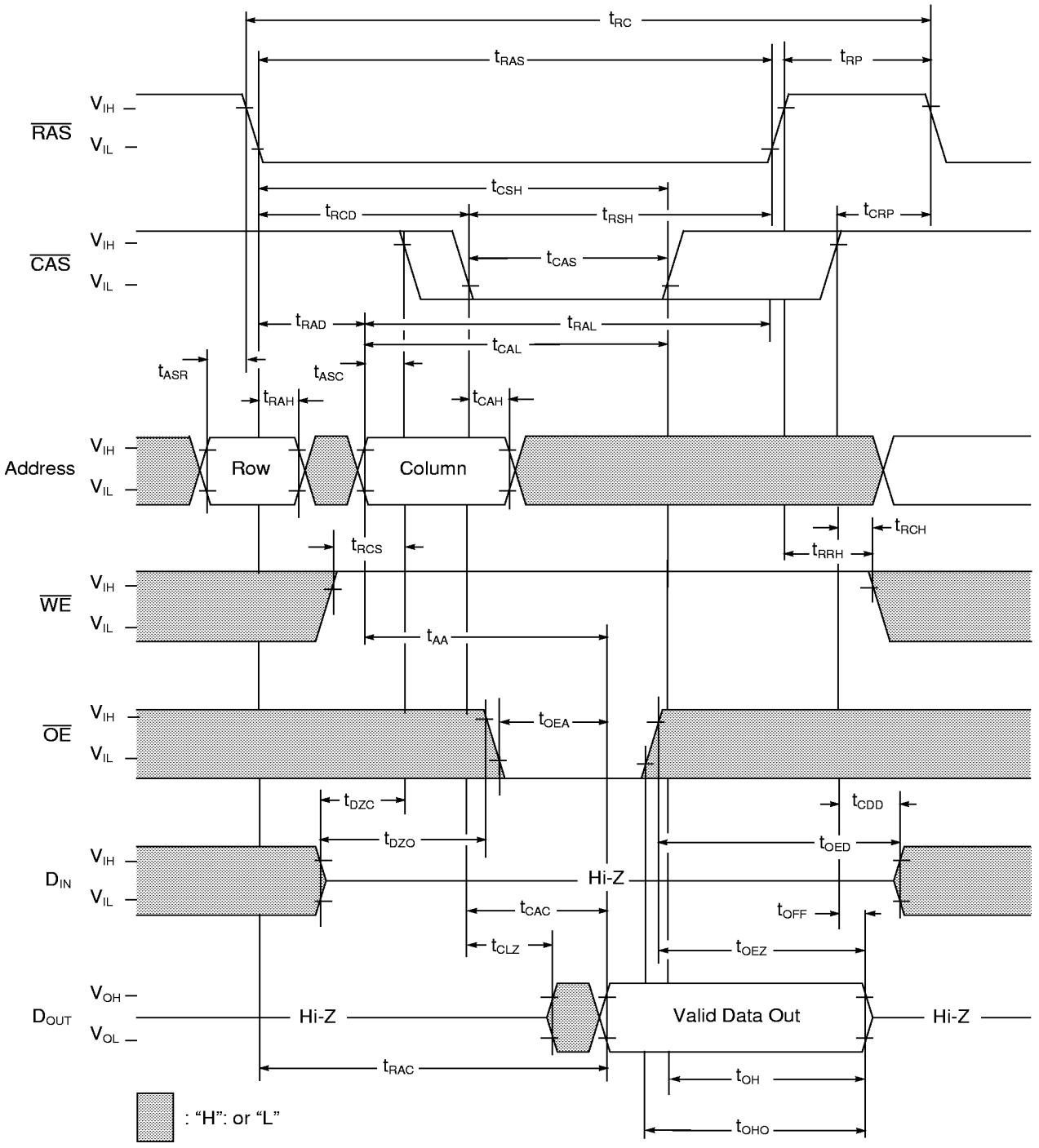
1. Measured with the specified current load and 100pF at V_{OL} = 0.8V and V_{OH} = 2.0V.

Refresh Cycle

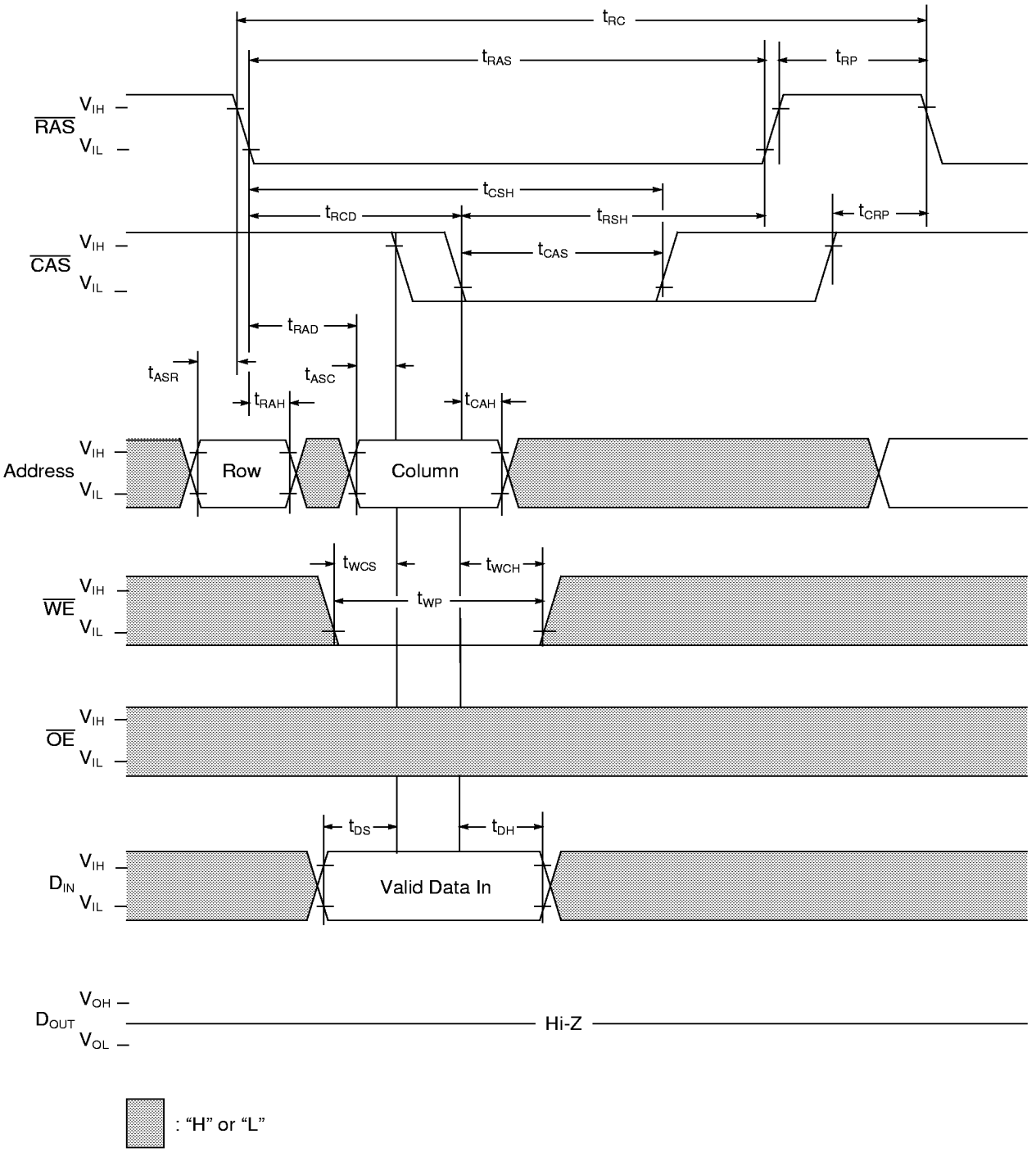
Symbol	Parameter	-50		-60		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	5	—	ns	
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	5	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	64	—	64	ms	1

1. 4096 cycles for RAS Only Refresh; 4096 cycles for CBR Refresh.

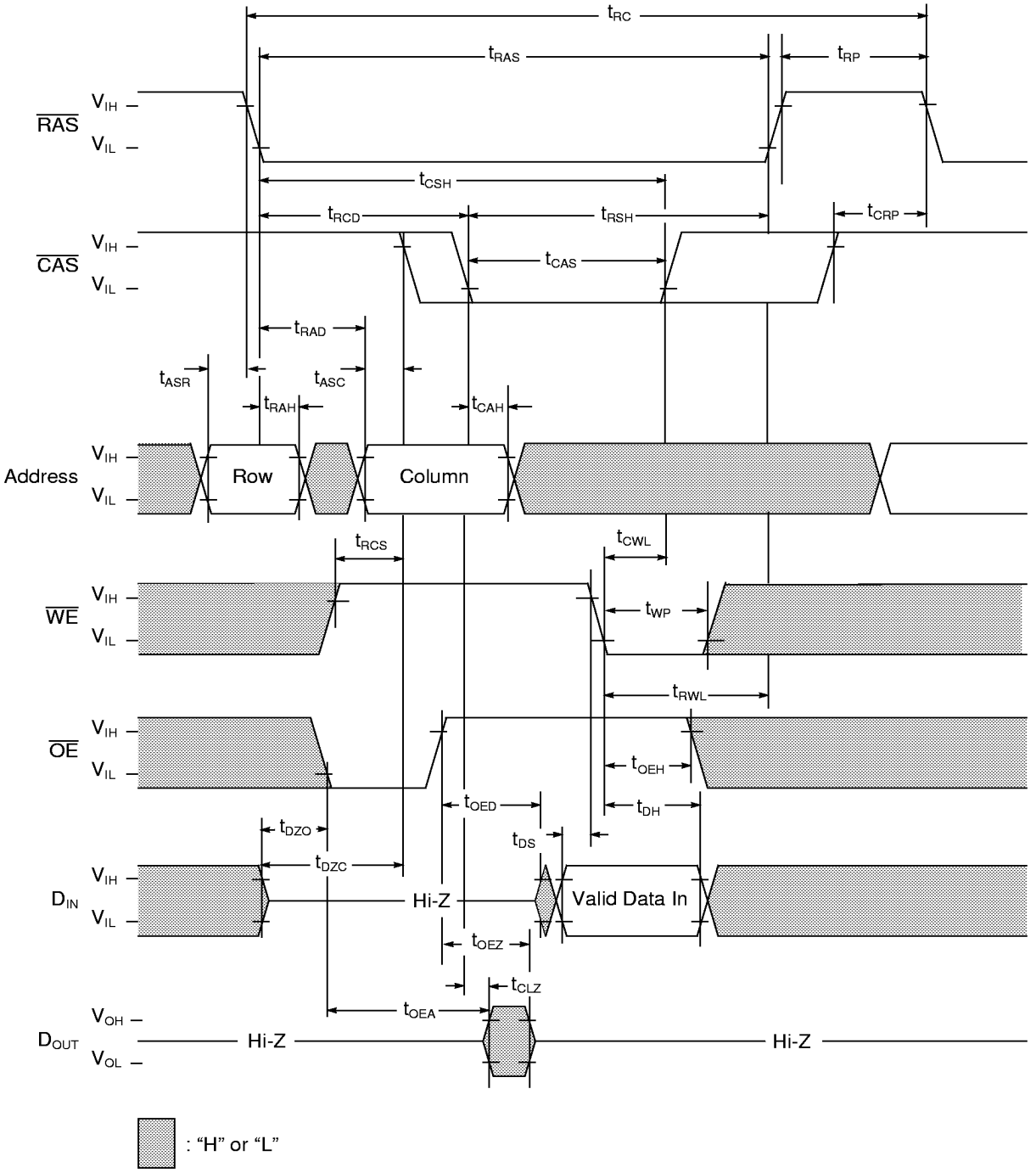
Read Cycle



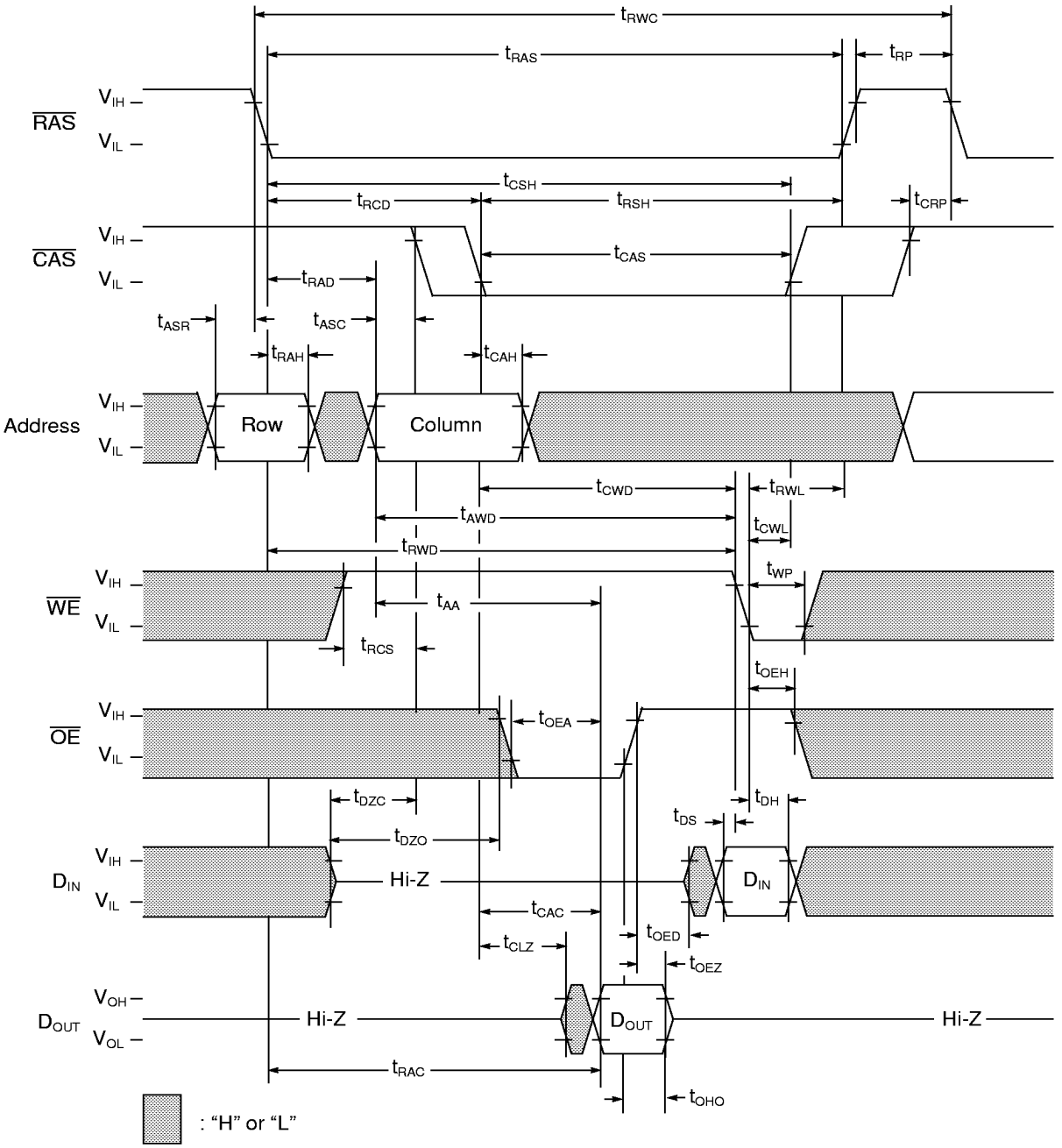
Write Cycle (Early Write)



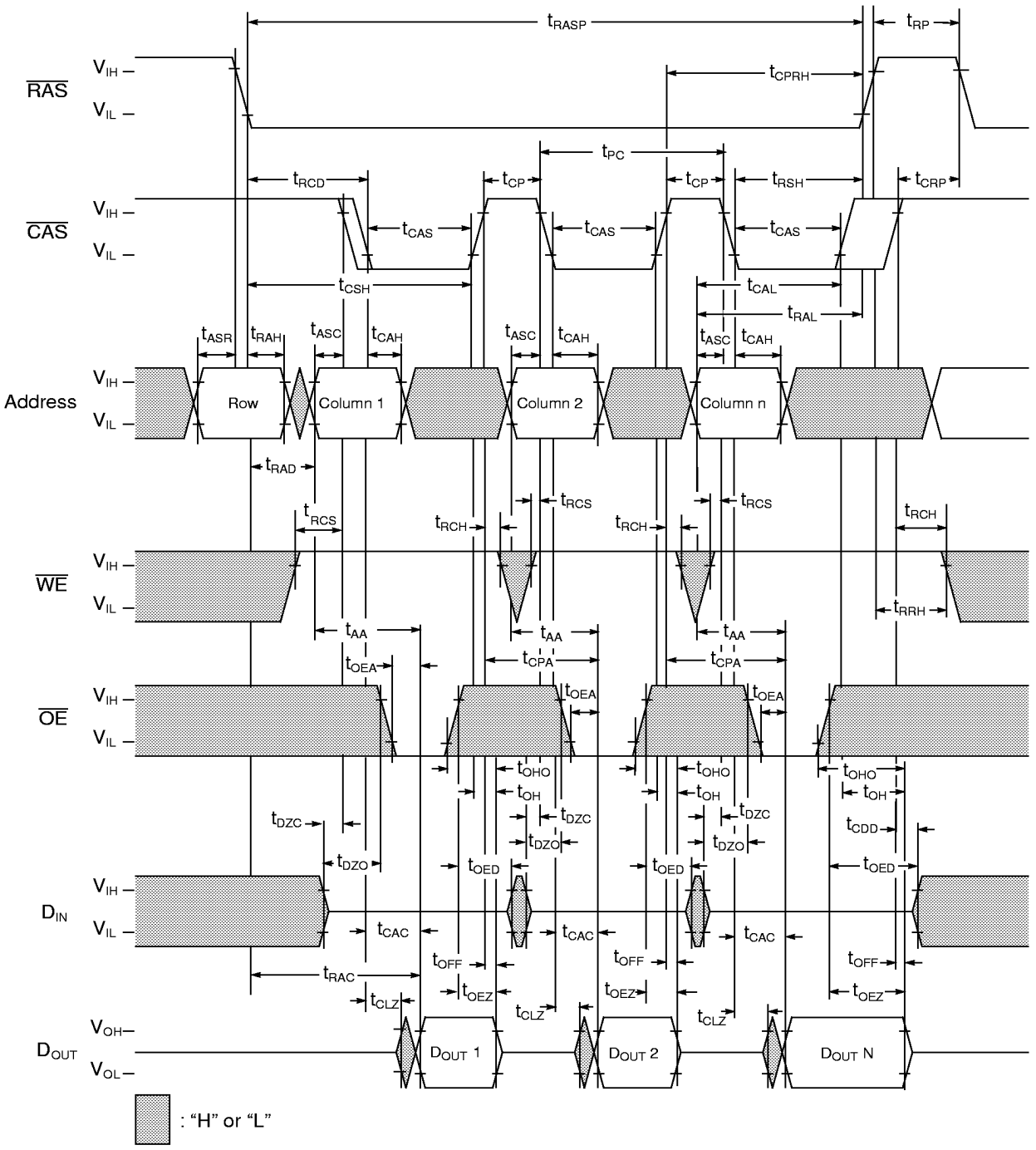
Write Cycle (Delayed Write)



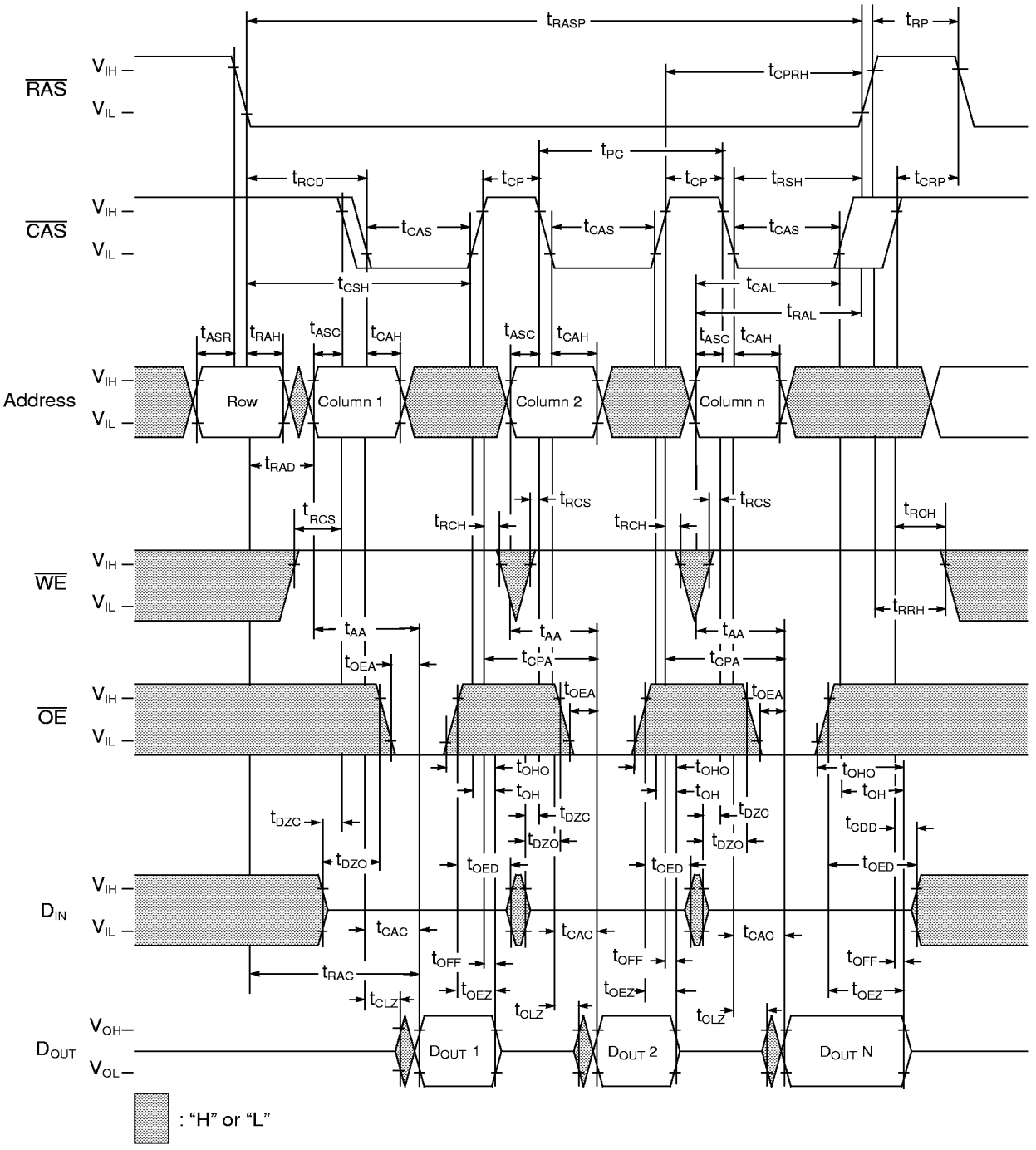
Read-Modify-Write Cycle



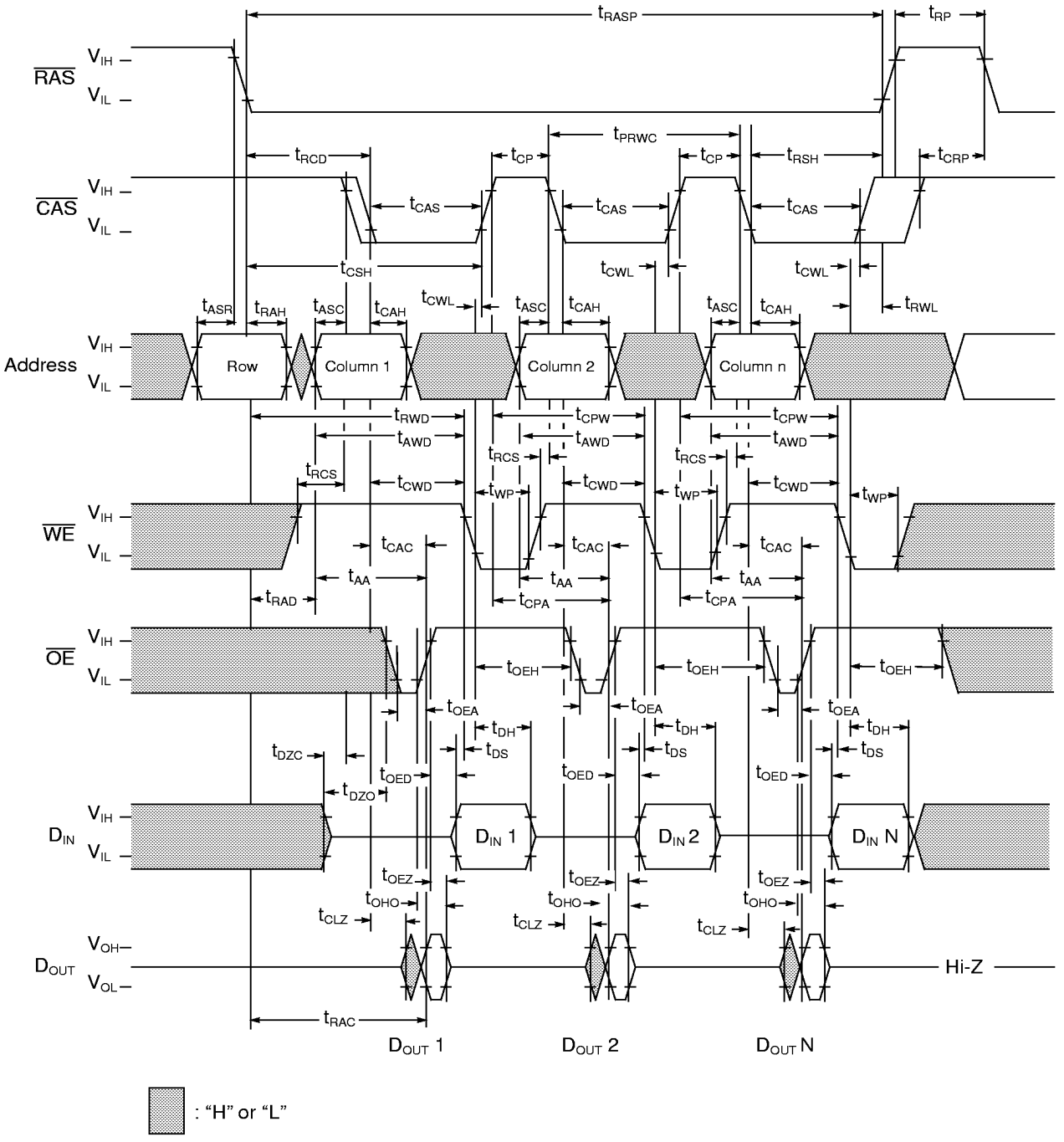
Fast Page Mode Read Cycle



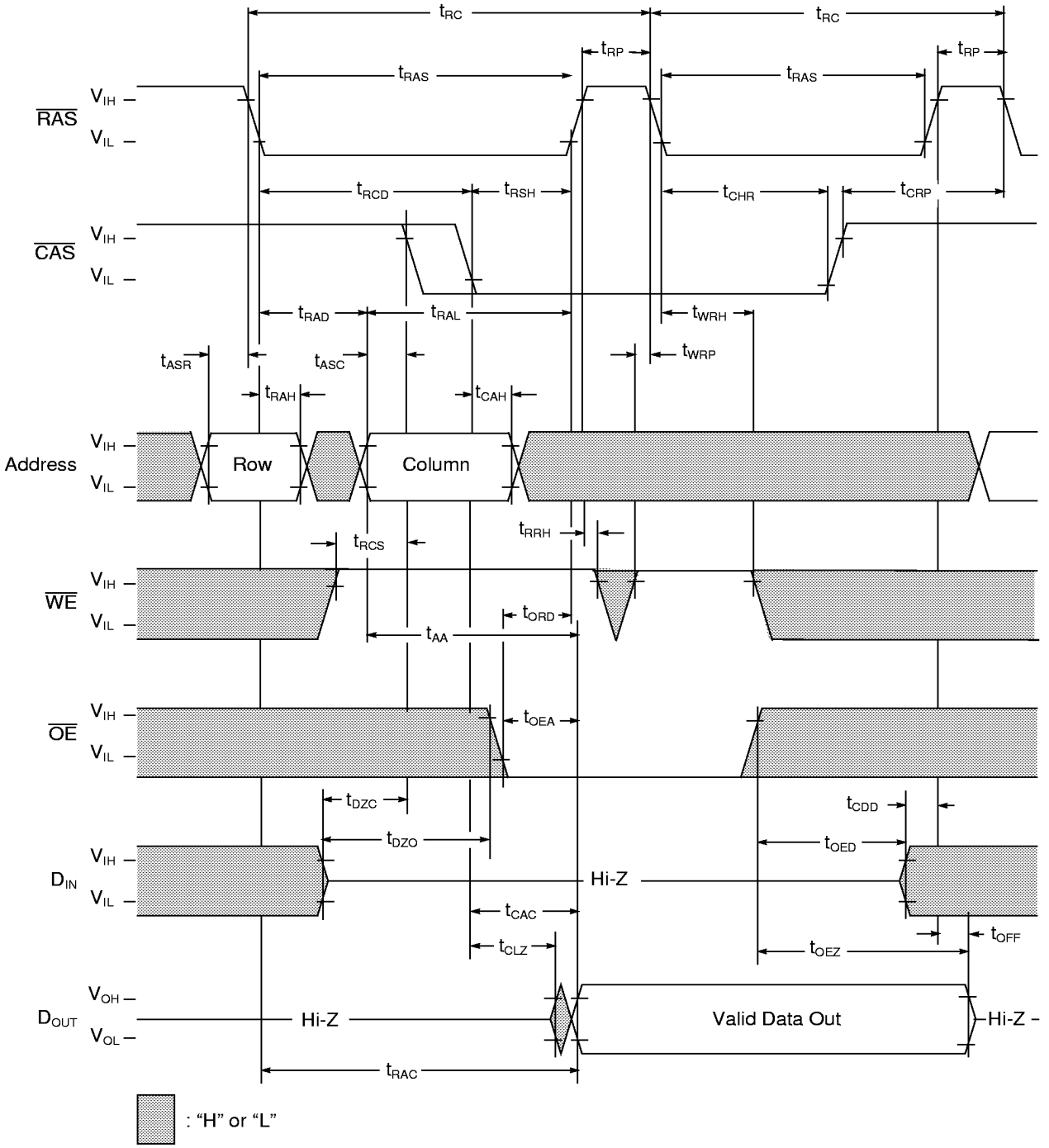
Fast Page Mode Write Cycle



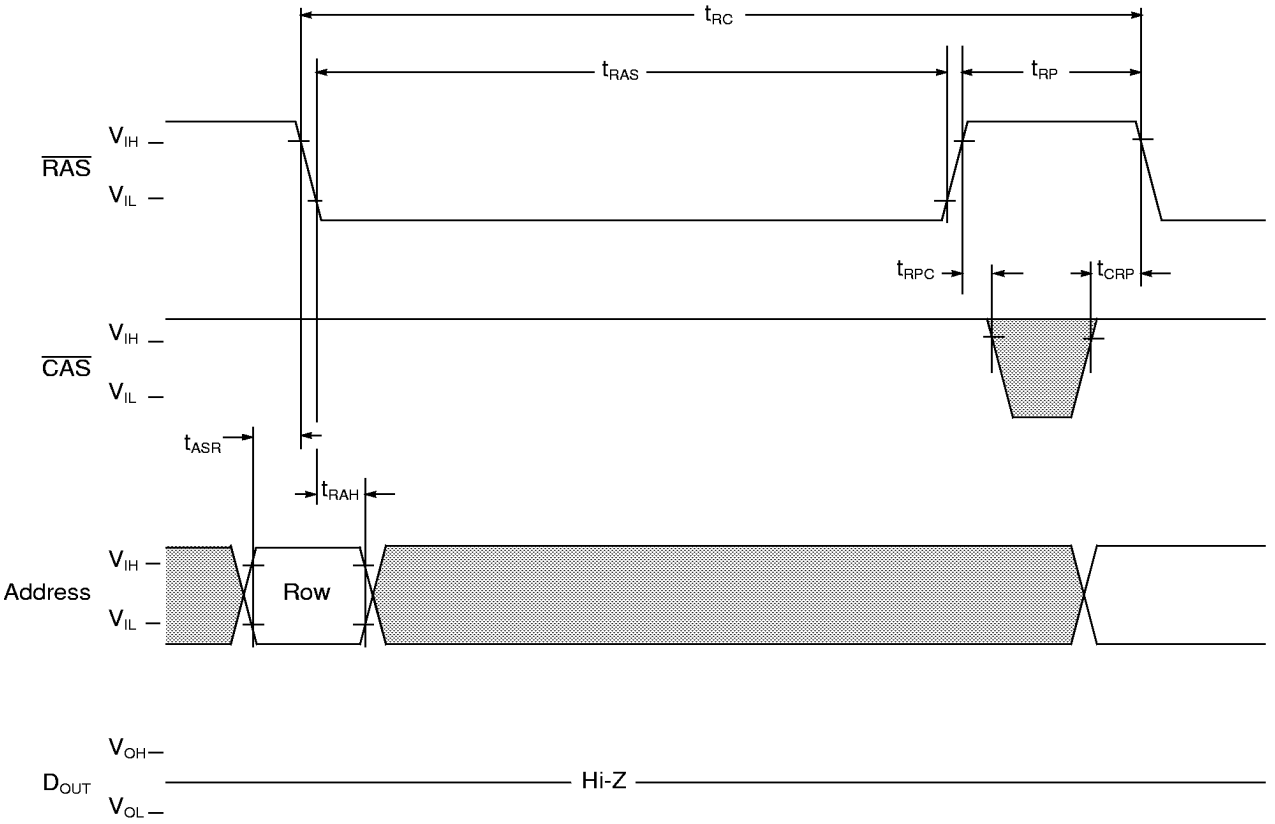
Fast Page Mode Read-Modify-Write Cycle



Hidden Refresh Cycle (Read)



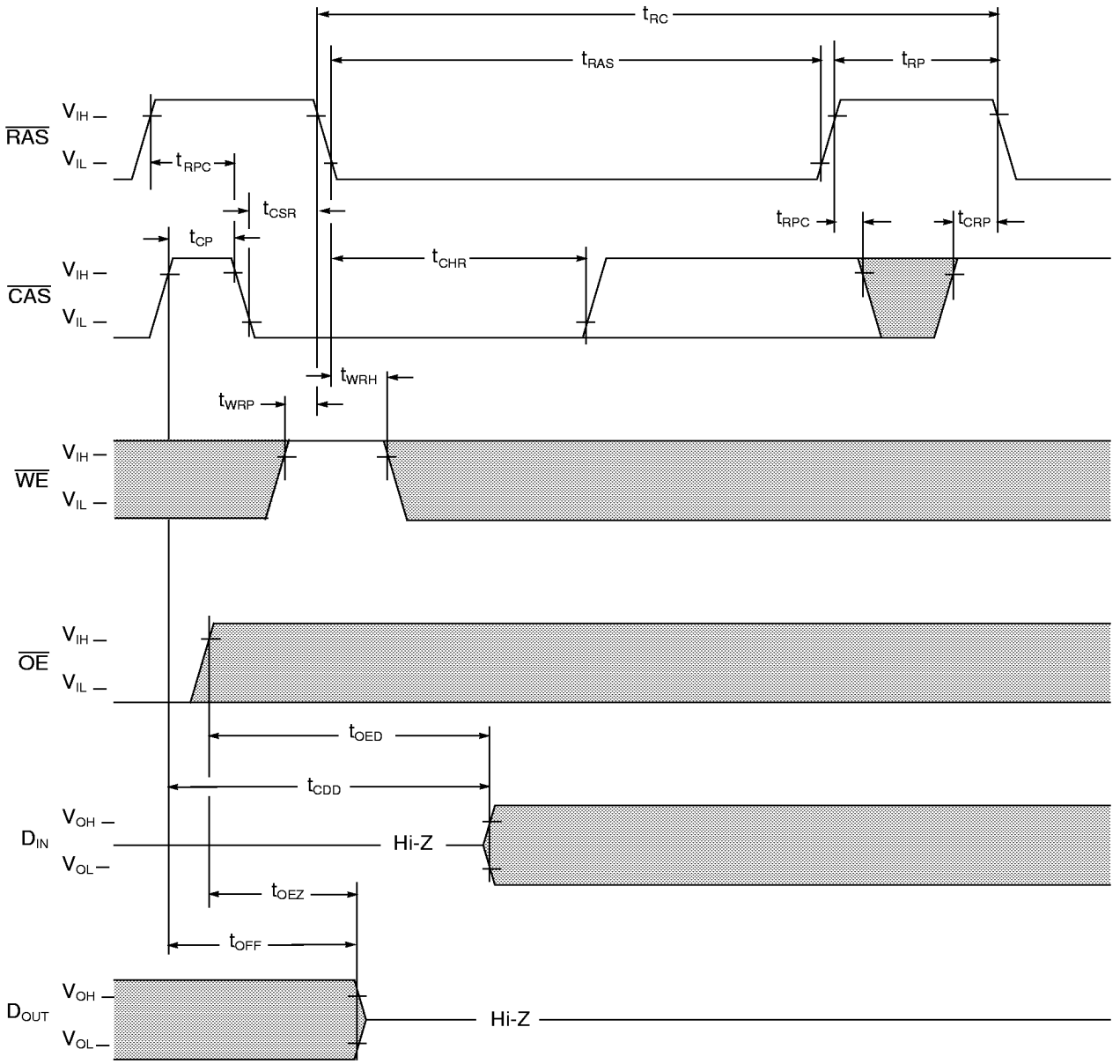
$\overline{RAS}$ Only Refresh Cycle



: "H" or "L"

NOTE: $\overline{WE}$, $\overline{OE}$ and D_{IN} are "H" or "L"

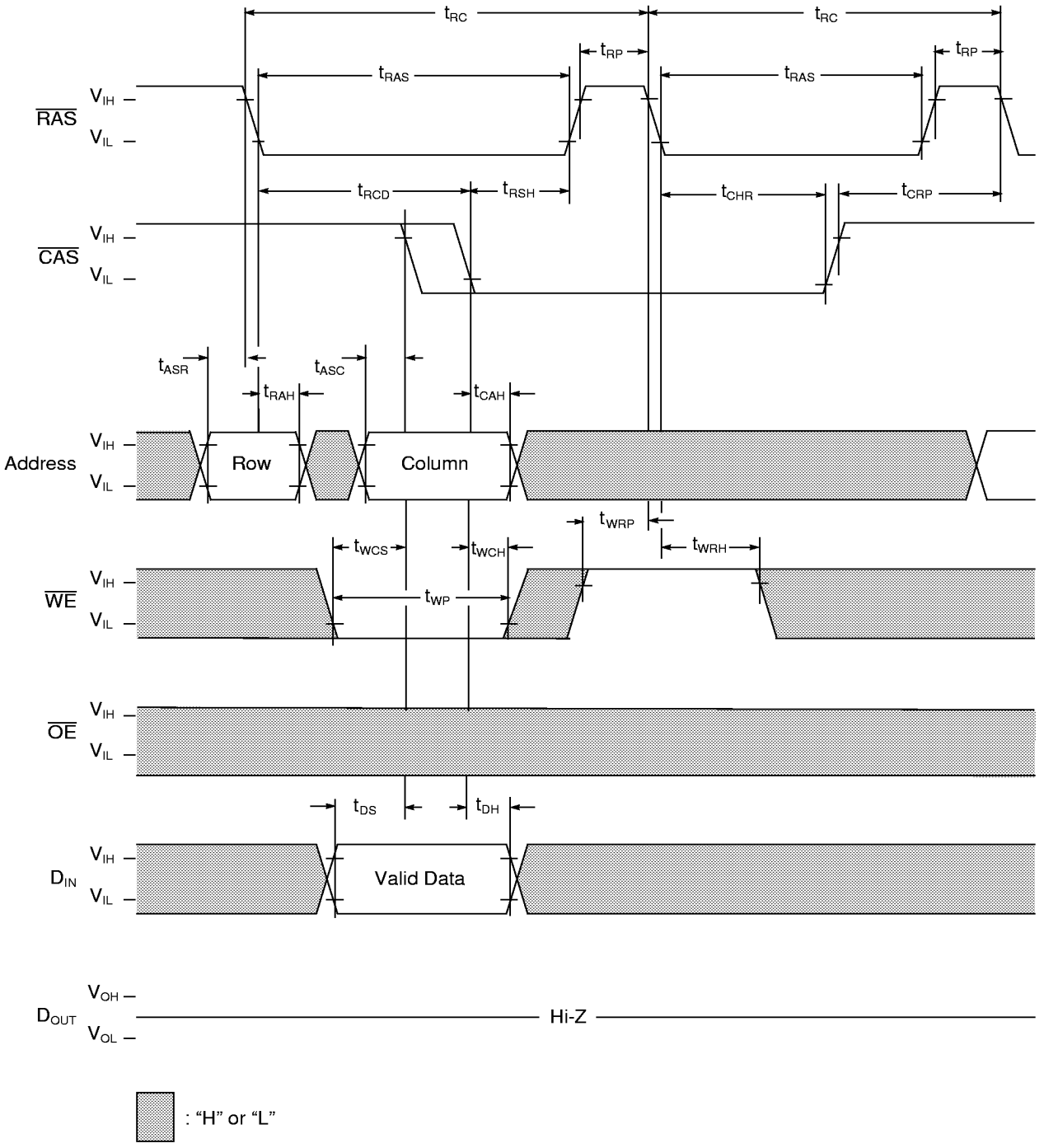
$\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle



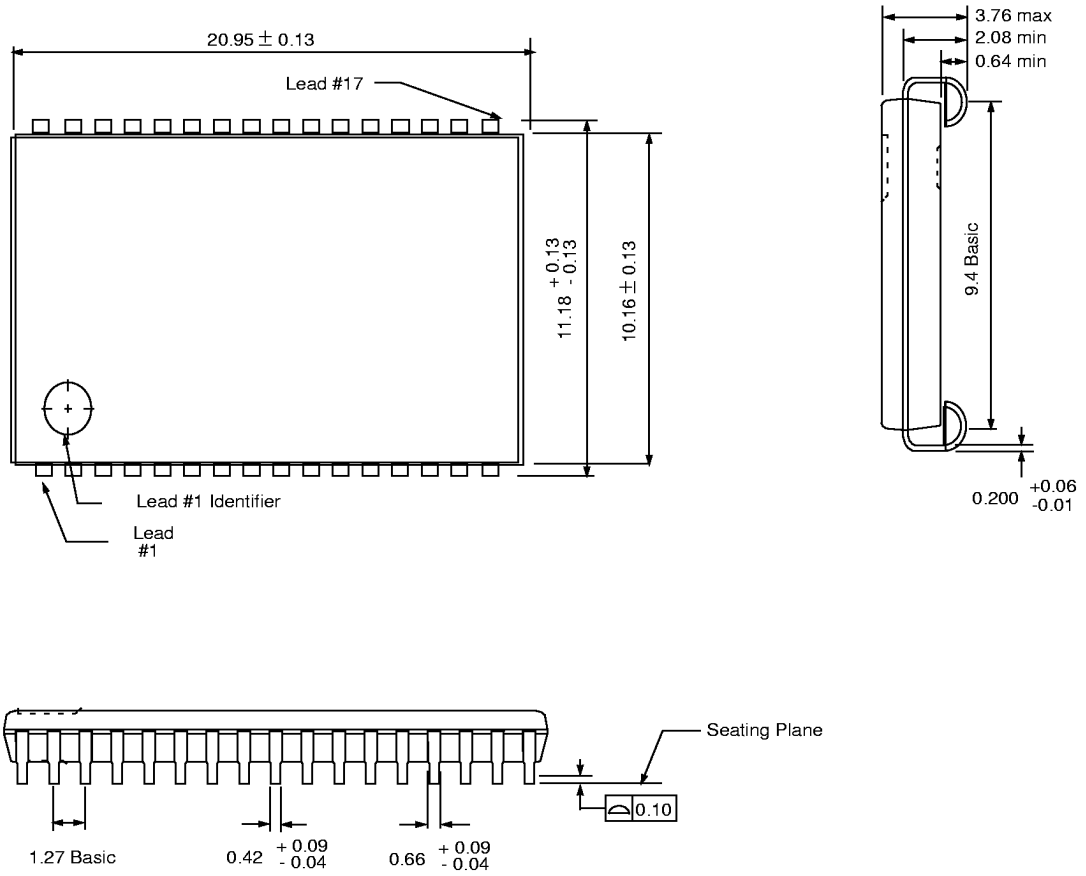
: "H" or "L"

NOTE: Address is "H" or "L"

Hidden Refresh Cycle (Write)

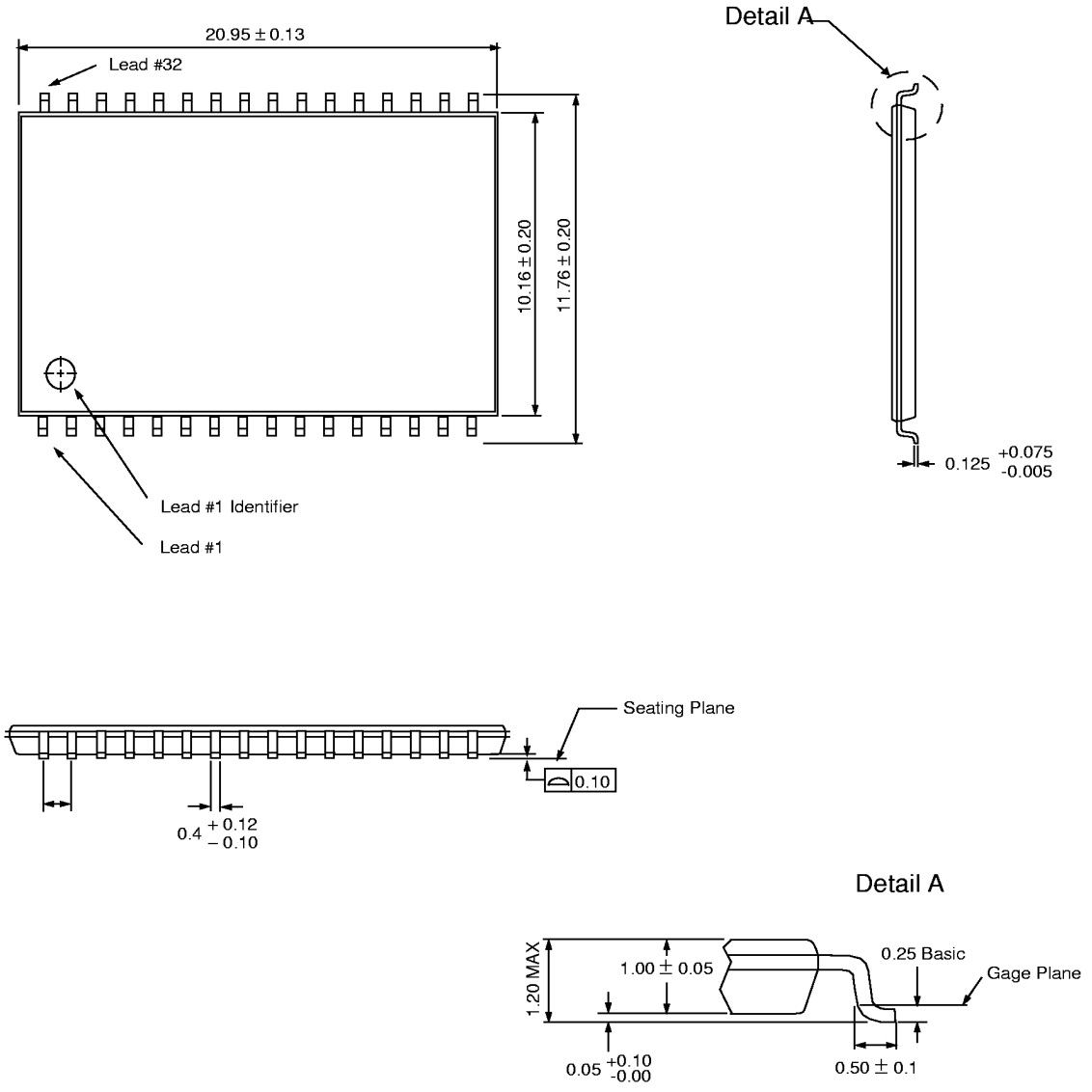


Package Dimensions (400 mil; 32 lead; Small Outline J-Lead)



NOTE: All dimensions are in millimeters. Reference JEDEC Standard MS-27

Package Dimensions (400 mil; 32lead; Thin Small Outline Package)



NOTE: All dimensions are in millimeters. Reference JEDEC Standard MS-24

Revision Log

Revision	Contents of Modification
12/18/96	Initial Release
03/19/97	1. $\overline{WE}$ for the Hidden Refresh Write cycle in the Truth Table was changed from “H” to “L→H”. 2. t_{ODD} was renamed to t_{OED}. 3. t_{OED} was moved from the Common Parameters table to the Write Cycle Parameters Table. 4. All Test Mode parameters and timing diagrams were removed. 5. LVTTL/LVCMOS changed to TTL/CMOS. 6. LVCMOS currents were removed. 7. Power numbers on the spec cover were recalculated.