

## 1M x 72 DRAM MODULE

### Features

- 168 Pin JEDEC Standard, 8 Byte Dual In-line Memory Module
- 1Mx72 Fast Page Mode DIMM
- Performance:
 

|           |                              | -60   | -70   |
|-----------|------------------------------|-------|-------|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 60ns  | 70ns  |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 20ns  | 25ns  |
| $t_{AA}$  | Access Time From Address     | 35ns  | 40ns  |
| $t_{RC}$  | Cycle Time                   | 110ns | 130ns |
| $t_{PC}$  | Fast Page Mode Cycle Time    | 40ns  | 45ns  |
- All inputs and outputs are LVTTTL (3.3V) or TTL (5.0V) compatible
- Single 3.3V  $\pm$  0.3V or 5.0V  $\pm$  0.5V Power Supply
- Au contacts

- Optimized for ECC applications
- System Performance Benefits:
  - Buffered inputs (except  $\overline{RAS}$ , Data)
  - Reduced noise (32  $V_{SS}/V_{CC}$  pins)
  - 4 Byte Interleave enabled
  - Buffered PDs
- Fast Page Mode, Read-Modify-Write Cycles
- Refresh Modes:  $\overline{RAS}$ -Only, CBR and Hidden Refresh
- 1024 refresh cycles distributed across 16ms
- 10/10 addressing (Row/Column)
- Card Size:
  - 5.25" x 1.0" x 0.354" (SOJ)
  - 5.25" x 1.0" x 0.157" (TSOP)
- DRAMS in SOJ or TSOP Packages

### Description

IBM11M1730B is an industry standard 168-pin 8-byte Dual In-line Memory Module (DIMM) which is organized as a 1Mx72 high speed memory array for ECC applications. The DIMM uses 18 1Mx4 DRAMs in SOJ or TSOP packages.

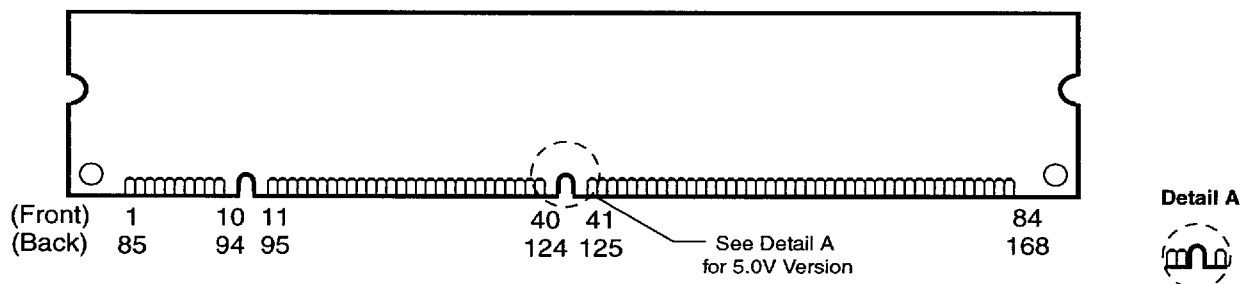
Improved system performance is provided by the on-DIMM buffering of selected input signals. The specified timings include all buffer, net and skew delays, which simplifies the memory subsystem design analysis. The data and RAS signals are not buffered, which preserves the DRAM access specifications of 60ns and 70ns.

Presence Detect (PD) and Identification Detect (ID) bits provide information about the DIMM density,

addressing, performance and features. PD bits can be dotted at the system level and activated for each DIMM position using the PD enable ( $\overline{PDE}$ ) signal. ID bits also allow detection of card features, and may be dot-or'd at the system level to provide information for the entire DIMM bank. For example, the system will determine that ECC DIMMs are installed if PD8 is low (0). ID0 need not be sensed since both x72 and x80 ECC DIMMs will function in a x72 bank.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products are the x64 and x72 parity (5V) DIMMs and ECC DIMMs (5V and 3.3V).

### Card Outline 3.3V



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## Pin Description

|                                    |                                  |                  |                             |
|------------------------------------|----------------------------------|------------------|-----------------------------|
| $\overline{RAS}0, \overline{RAS}2$ | Row Address Strobe               | $V_{CC}$         | Power (3.3V or 5.0V)        |
| $\overline{CAS}0, \overline{CAS}4$ | Column Address Strobe (Buffered) | $V_{SS}$         | Ground                      |
| $\overline{WE}0, \overline{WE}2$   | Read/write Input (Buffered)      | NC               | No Connect                  |
| $\overline{OE}0, \overline{OE}2$   | Output Enable (Buffered)         | PD1 - PD8        | Presence Detects (Buffered) |
| A0, B0, A1 - A9                    | Address Inputs (Buffered)        | $\overline{PDE}$ | Presence Detect Enable      |
| DQx                                | Data Input/Output                | ID0 - ID1        | ID Bits                     |

## Pinout

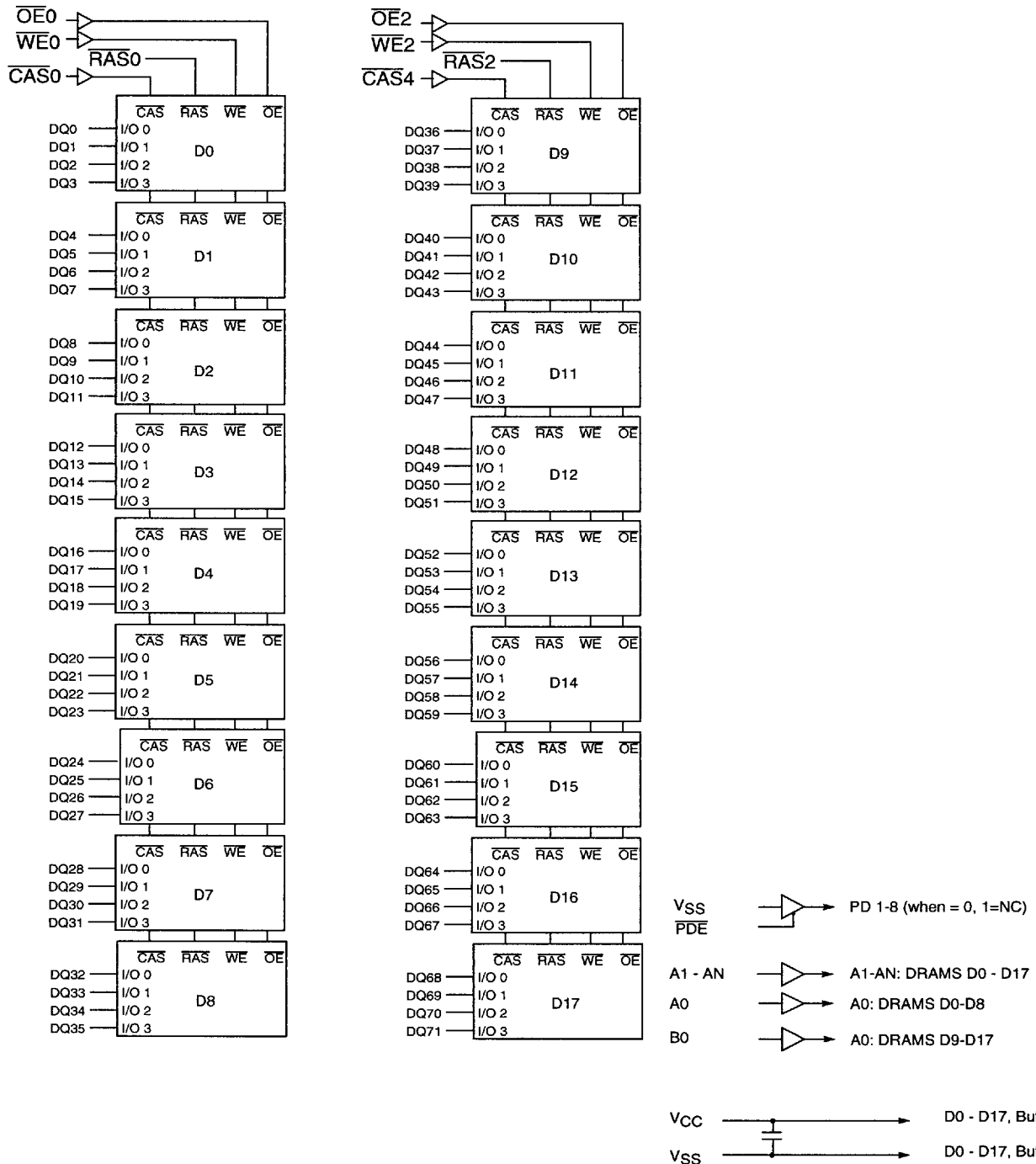
| Pin# | Front Side | Pin# | Back Side | Pin# | Front Side        | Pin# | Back Side | Pin# | Front Side        | Pin# | Back Side        | Pin# | Front Side | Pin# | Back Side |
|------|------------|------|-----------|------|-------------------|------|-----------|------|-------------------|------|------------------|------|------------|------|-----------|
| 1    | $V_{SS}$   | 85   | $V_{SS}$  | 22   | DQ17              | 106  | DQ53      | 43   | $V_{SS}$          | 127  | $V_{SS}$         | 64   | NC         | 148  | NC        |
| 2    | DQ0        | 86   | DQ36      | 23   | $V_{SS}$          | 107  | $V_{SS}$  | 44   | $\overline{OE}2$  | 128  | NC               | 65   | DQ25       | 149  | DQ61      |
| 3    | DQ1        | 87   | DQ37      | 24   | NC                | 108  | NC        | 45   | $\overline{RAS}2$ | 129  | NC               | 66   | DQ26       | 150  | DQ62      |
| 4    | DQ2        | 88   | DQ38      | 25   | NC                | 109  | NC        | 46   | $\overline{CAS}4$ | 130  | NC               | 67   | DQ27       | 151  | DQ63      |
| 5    | DQ3        | 89   | DQ39      | 26   | $V_{CC}$          | 110  | $V_{CC}$  | 47   | NC                | 131  | NC               | 68   | $V_{SS}$   | 152  | $V_{SS}$  |
| 6    | $V_{CC}$   | 90   | $V_{CC}$  | 27   | $\overline{WE}0$  | 111  | NC        | 48   | $\overline{WE}2$  | 132  | $\overline{PDE}$ | 69   | DQ28       | 153  | DQ64      |
| 7    | DQ4        | 91   | DQ40      | 28   | $\overline{CAS}0$ | 112  | NC        | 49   | $V_{CC}$          | 133  | $V_{CC}$         | 70   | DQ29       | 154  | DQ65      |
| 8    | DQ5        | 92   | DQ41      | 29   | NC                | 113  | NC        | 50   | NC                | 134  | NC               | 71   | DQ30       | 155  | DQ66      |
| 9    | DQ6        | 93   | DQ42      | 30   | $\overline{RAS}0$ | 114  | NC        | 51   | NC                | 135  | NC               | 72   | DQ31       | 156  | DQ67      |
| 10   | DQ7        | 94   | DQ43      | 31   | $\overline{OE}0$  | 115  | NC        | 52   | DQ18              | 136  | DQ54             | 73   | $V_{CC}$   | 157  | $V_{CC}$  |
| 11   | DQ8        | 95   | DQ44      | 32   | $V_{SS}$          | 116  | $V_{SS}$  | 53   | DQ19              | 137  | DQ55             | 74   | DQ32       | 158  | DQ68      |
| 12   | $V_{SS}$   | 96   | $V_{SS}$  | 33   | A0                | 117  | A1        | 54   | $V_{SS}$          | 138  | $V_{SS}$         | 75   | DQ33       | 159  | DQ69      |
| 13   | DQ9        | 97   | DQ45      | 34   | A2                | 118  | A3        | 55   | DQ20              | 139  | DQ56             | 76   | DQ34       | 160  | DQ70      |
| 14   | DQ10       | 98   | DQ46      | 35   | A4                | 119  | A5        | 56   | DQ21              | 140  | DQ57             | 77   | DQ35       | 161  | DQ71      |
| 15   | DQ11       | 99   | DQ47      | 36   | A6                | 120  | A7        | 57   | DQ22              | 141  | DQ58             | 78   | $V_{SS}$   | 162  | $V_{SS}$  |
| 16   | DQ12       | 100  | DQ48      | 37   | A8                | 121  | A9        | 58   | DQ23              | 142  | DQ59             | 79   | PD1        | 163  | PD2       |
| 17   | DQ13       | 101  | DQ49      | 38   | NC                | 122  | NC        | 59   | $V_{CC}$          | 143  | $V_{CC}$         | 80   | PD3        | 164  | PD4       |
| 18   | $V_{CC}$   | 102  | $V_{CC}$  | 39   | NC                | 123  | NC        | 60   | DQ24              | 144  | DQ60             | 81   | PD5        | 165  | PD6       |
| 19   | DQ14       | 103  | DQ50      | 40   | $V_{CC}$          | 124  | $V_{CC}$  | 61   | NC                | 145  | NC               | 82   | PD7        | 166  | PD8       |
| 20   | DQ15       | 104  | DQ51      | 41   | NC                | 125  | NC        | 62   | NC                | 146  | NC               | 83   | ID0        | 167  | ID1       |
| 21   | DQ16       | 105  | DQ52      | 42   | NC                | 126  | B0        | 63   | NC                | 147  | NC               | 84   | $V_{CC}$   | 168  | $V_{CC}$  |

Note: All pin assignments are consistent for all 8 Byte versions.

## Ordering Information

| Part Number      | Organization | Speed | Leads | Dimension          | Power | DRAM Die Revision | Notes |
|------------------|--------------|-------|-------|--------------------|-------|-------------------|-------|
| IBM11M1730BD-60  | 1Mx72        | 60ns  | Au    | 5.25"x1.0"x 0.354" | 5.0V  | E                 |       |
| IBM11M1730BD-70  | 1Mx72        | 70ns  | Au    | 5.25"x1.0"x 0.354" | 5.0V  | E                 |       |
| IBM11M1730BE-60  | 1Mx72        | 60ns  | Au    | 5.25"x1.0"x 0.157" | 5.0V  | E                 |       |
| IBM11M1730BE-70  | 1Mx72        | 70ns  | Au    | 5.25"x1.0"x 0.157" | 5.0V  | E                 |       |
| IBM11M1730BF-60  | 1Mx72        | 60ns  | Au    | 5.25"x1.0"x 0.354" | 5.0V  | F                 |       |
| IBM11M1730BF-70  | 1Mx72        | 70ns  | Au    | 5.25"x1.0"x 0.354" | 5.0V  | F                 |       |
| IBM11M1730BBD-60 | 1Mx72        | 60ns  | Au    | 5.25"x1.0"x 0.354" | 3.3V  | E                 |       |
| IBM11M1730BBD-70 | 1Mx72        | 70ns  | Au    | 5.25"x1.0"x 0.354" | 3.3V  | E                 |       |
| IBM11M1730BBH-60 | 1Mx72        | 60ns  | Au    | 5.25"x1.0"x 0.354" | 3.3V  | F                 |       |
| IBM11M1730BBH-70 | 1Mx72        | 70ns  | Au    | 5.25"x1.0"x 0.354" | 3.3V  | F                 |       |

# Block Diagram



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## Truth Table

| Function                                                         |       | $\overline{\text{RAS}}$ | $\overline{\text{CAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | Row Address | Column Address | $\overline{\text{PDE}}$ | DQx                              |
|------------------------------------------------------------------|-------|-------------------------|-------------------------|------------------------|------------------------|-------------|----------------|-------------------------|----------------------------------|
| Standby                                                          |       | H                       | H→X                     | X                      | X                      | X           | X              | X                       | High Impedance                   |
| Read                                                             |       | L                       | L                       | H                      | L                      | Row         | Col            | X                       | Valid Data Out                   |
| Early-Write                                                      |       | L                       | L                       | L                      | X                      | Row         | Col            | X                       | Valid Data In                    |
| Late-Write / RMW                                                 |       | L                       | L                       | H→L                    | L→H                    | Row         | Col            | X                       | Valid Data Out,<br>Valid Data In |
| Fast Page Mode - Read<br>1st Cycle                               |       | L                       | H→L                     | H                      | L                      | Row         | Col            | X                       | Valid Data Out                   |
| Subsequent Cycles                                                |       | L                       | H→L                     | H                      | L                      | N/A         | Col            | X                       | Valid Data Out                   |
| Fast Page Mode - Write<br>1st Cycle                              |       | L                       | H→L                     | L                      | X                      | Row         | Col            | X                       | Valid Data In                    |
| Subsequent Cycles                                                |       | L                       | H→L                     | L                      | X                      | N/A         | Col            | X                       | Valid Data In                    |
| Fast Page Mode - RMW<br>1st Cycle                                |       | L                       | H→L                     | H→L                    | L→H                    | Row         | Col            | X                       | Valid Data Out,<br>Valid Data In |
| Subsequent Cycles                                                |       | L                       | H→L                     | H→L                    | L→H                    | N/A         | Col            | X                       | Valid Data Out,<br>Valid Data In |
| $\overline{\text{RAS}}$ -Only Refresh                            |       | L                       | H                       | X                      | X                      | Row         | N/A            | X                       | High Impedance                   |
| $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh |       | H→L                     | L                       | H                      | X                      | X           | X              | X                       | High Impedance                   |
| Hidden Refresh                                                   | Read  | L→H→L                   | L                       | H                      | L                      | Row         | Col            | X                       | Data Out                         |
|                                                                  | Write | L→H→L                   | L                       | H                      | X                      | Row         | Col            | X                       | Data In                          |
| Read Presence Detects                                            |       | X                       | X                       | X                      | X                      | X           | X              | L                       | Not Affected<br>(PD Bits Valid)  |

## Presence Detect

| Pin                                                                                                                                                                                                           | -60 | -70 |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|
| PD1 (PD1 - PD4: Addressing/Density)                                                                                                                                                                           | 0   | 0   |
| PD2                                                                                                                                                                                                           | 0   | 0   |
| PD3                                                                                                                                                                                                           | 1   | 1   |
| PD4                                                                                                                                                                                                           | 0   | 0   |
| PD5 (EDO Detection)                                                                                                                                                                                           | 0   | 0   |
| PD6 (PD6 - PD7: Speed)                                                                                                                                                                                        | 1   | 0   |
| PD7                                                                                                                                                                                                           | 1   | 1   |
| PD8 (Parity/ECC Designator)                                                                                                                                                                                   | 0   | 0   |
| ID0 (DIMM Type/Width)                                                                                                                                                                                         | 0   | 0   |
| ID1 (Refresh Mode)                                                                                                                                                                                            | 0   | 0   |
| 1. PD1-8 are buffered outputs (0 = driven to V <sub>OL</sub> , 1 = open)<br>2. ID0-1 are unbuffered outputs (0 = V <sub>SS</sub> , 1 = open)<br>3. PDE should be tied high or low at system level if not used |     |     |

# Absolute Maximum Ratings

| Symbol      | Parameter                         | Rating (3.3V)                       | Rating (5.0V)                       | Units | Notes |
|-------------|-----------------------------------|-------------------------------------|-------------------------------------|-------|-------|
| $V_{CC}$    | Power Supply Voltage              | -0.5 to +4.1                        | -1.0 to +6.0                        | V     | 1     |
| $V_{IN}$    | Input Voltage                     | -0.5 to min ( $V_{CC} + 0.5$ , 4.1) | -0.5 to min ( $V_{CC} + 0.5$ , 6.0) | V     | 1     |
| $V_{OUT}$   | Output Voltage                    | -0.5 to min ( $V_{CC} + 0.5$ , 4.1) | -0.5 to min ( $V_{CC} + 0.5$ , 6.0) | V     | 1     |
| $T_{OPR}$   | Operating Temperature             | 0 to +70                            | 0 to +70                            | °C    | 1     |
| $T_{STG}$   | Storage Temperature               | -55 to +125                         | -55 to +125                         | °C    | 1     |
| $P_D$       | Power Dissipation                 | 6.2                                 | 8.4                                 | W     | 1     |
| $I_{OUT}$   | Short Circuit Output Current      | 50                                  | 50                                  | mA    | 1     |
| $I_{OUTPD}$ | Short Circuit Output Current (PD) | 60                                  | 60                                  | mA    | 1     |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated is not implied. Exposure to absolute maximum rating condition for extended periods may affect reliability.

# Recommended DC Operating Conditions ( $T_A = 0$ to $70^{\circ}\text{C}$ )

| Symbol   | Parameter          | 3.3V |     |                | 5.0V |     |                | Units | Notes |
|----------|--------------------|------|-----|----------------|------|-----|----------------|-------|-------|
|          |                    | Min  | Typ | Max            | Min  | Typ | Max            |       |       |
| $V_{CC}$ | Supply Voltage     | 3.0  | 3.3 | 3.6            | 4.5  | 5.0 | 5.5            | V     | 1     |
| $V_{IH}$ | Input High Voltage | 2.0  | —   | $V_{CC} + 0.3$ | 2.4  | —   | $V_{CC} + 0.5$ | V     | 1, 2  |
| $V_{IL}$ | Input Low Voltage  | -0.3 | —   | 0.8            | -0.5 | —   | 0.8            | V     | 1, 2  |

1. All voltages referenced to  $V_{SS}$ .
2.  $V_{IH}$  may overshoot to  $V_{CC} + 1.2\text{V}$  for pulse widths of  $\leq 4.0\text{ns}$  with 3.3 Volt, or  $V_{CC} + 2.0\text{V}$  for pulse widths of  $\leq 4.0\text{ns}$  (or  $V_{CC} + 1.0\text{V}$  for  $\leq 8.0\text{ns}$ ) with 5.0 Volt. Additionally,  $V_{IL}$  may undershoot to  $-1.2\text{V}$  for pulse widths  $\leq 4.0\text{ns}$  with 3.3 Volt, or to  $-2.0\text{V}$  for pulse widths  $\leq 4.0\text{ns}$  (or  $-1.0\text{V}$  for  $\leq 8.0\text{ns}$ ) with 5.0 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

# Capacitance ( $T_A = 0$ to $+70^{\circ}\text{C}$ , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $5.0\text{V} \pm 0.5\text{V}$ )

| Symbol    | Parameter                                                                                       | Max | Units | Notes |
|-----------|-------------------------------------------------------------------------------------------------|-----|-------|-------|
| $C_{I1}$  | Input Capacitance (A0, B0, A1-A9)                                                               | 13  | pF    |       |
| $C_{I2}$  | Input Capacitance ( $\overline{\text{RAS}}$ )                                                   | 70  | pF    |       |
| $C_{I3}$  | Input Capacitance ( $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$ ) | 13  | pF    |       |
| $C_{I4}$  | Input Capacitance ( $\overline{\text{PDE}}$ )                                                   | 18  | pF    |       |
| $C_{IO1}$ | Input/Output Capacitance (DQx)                                                                  | 15  | pF    |       |
| $C_{O1}$  | Output Capacitance (PD)                                                                         | 15  | pF    |       |
| $C_{O2}$  | Output Capacitance (ID)                                                                         | 5   | pF    |       |

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DC Electrical Characteristics ( $T_A = 0$  to  $+70^\circ\text{C}$ ,  $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$  or  $V_{CC} = 5.0\text{V} \pm 0.5\text{V}$ )

| Symbol     | Parameter                                                                                                                                                                                                                                                              |                                 | 3.3 Volt |      | 5.0 Volt |          | Units         | Notes   |
|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------|----------|------|----------|----------|---------------|---------|
|            |                                                                                                                                                                                                                                                                        |                                 | Min.     | Max. | Min.     | Max.     |               |         |
| $I_{CC1}$  | Operating Current<br>Average Power Supply Operating Current<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{RC} = t_{RC \text{ min.}}$ )                                                                                                 | -60                             | —        | 1710 | —        | 1530     | mA            | 1, 2, 3 |
|            |                                                                                                                                                                                                                                                                        | -70                             | —        | 1440 | —        | 1260     |               |         |
| $I_{CC2}$  | Standby Current (TTL)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{IH}$ )                                                                                                                                                  |                                 | —        | 36   | —        | 36       | mA            |         |
| $I_{CC3}$  | $\overline{\text{RAS}}$ Only Refresh Current<br>Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode<br>( $\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} = V_{IH}$ ; $t_{RC} = t_{RC \text{ min.}}$ )                                              | -60                             | —        | 1710 | —        | 1530     | mA            | 1, 3    |
|            |                                                                                                                                                                                                                                                                        | -70                             | —        | 1440 | —        | 1260     |               |         |
| $I_{CC4}$  | Fast Page Mode Current<br>Average Power Supply Current, Hyper Page Mode<br>( $\overline{\text{RAS}} = V_{IL}$ , $\overline{\text{CAS}}$ , Address Cycling: $t_{PC} = t_{PC \text{ min.}}$ )                                                                            | -60                             | —        | 1170 | —        | 1080     | mA            | 1, 2, 3 |
|            |                                                                                                                                                                                                                                                                        | -70                             | —        | 1170 | —        | 1080     |               |         |
| $I_{CC5}$  | Standby Current (CMOS)<br>Power Supply Standby Current<br>( $\overline{\text{RAS}} = \overline{\text{CAS}} = V_{CC} - 0.2\text{V}$ )                                                                                                                                   |                                 | —        | 18   | —        | 18       | mA            |         |
| $I_{CC6}$  | $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current<br>Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode<br>( $\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , Cycling: $t_{RC} = t_{RC \text{ min.}}$ ) | -60                             | —        | 1710 | —        | 1530     | mA            | 1, 3    |
|            |                                                                                                                                                                                                                                                                        | -70                             | —        | 1440 | —        | 1260     |               |         |
| $I_{I(L)}$ | Input Leakage Current<br>Input Leakage Current, any input<br>( $0.0 \leq V_{IN} \leq (V_{CC} + 0.3\text{V})$ ), All Other Pins Not Under Test = 0V                                                                                                                     | All but $\overline{\text{RAS}}$ | -10      | +10  | -10      | +10      | $\mu\text{A}$ |         |
|            |                                                                                                                                                                                                                                                                        | $\overline{\text{RAS}}$         | -90      | +90  | -90      | +90      |               |         |
| $I_{O(L)}$ | Output Leakage Current<br>( $D_{OUT}$ is disabled, $0.0 \leq V_{OUT} \leq V_{CC}$ )                                                                                                                                                                                    |                                 | -10      | +10  | -10      | +10      | $\mu\text{A}$ |         |
| $V_{OH}$   | Output Level (TTL)<br>Output "H" Level Voltage<br>( $I_{OUT} = -2\text{mA}$ for 3.3V, or $I_{OUT} = -5\text{mA}$ for 5.0V)                                                                                                                                             |                                 | 2.4      | —    | 2.4      | $V_{CC}$ | V             |         |
| $V_{OL}$   | Output Level (TTL)<br>Output "L" Level Voltage<br>( $I_{OUT} = +2\text{mA}$ for 3.3V, or $I_{OUT} = +4.2\text{mA}$ for 5.0V)                                                                                                                                           |                                 | —        | 0.4  | —        | 0.4      | V             |         |

1.  $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC6}$  depend on cycle rate.  
 2.  $I_{CC1}$  and  $I_{CC4}$  depend on output loading. Specified values are obtained with the output open.  
 3. Address can be changed once or less while  $\overline{\text{RAS}} = V_{IL}$ . In the case of  $I_{CC4}$ , it can be changed once or less when  $\overline{\text{CAS}} = V_{IH}$ .

## AC Characteristics ( $T_A = 0$ to $+70^\circ\text{C}$ , $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$ or $5.0\text{V} \pm 0.5\text{V}$ )

- $V_{IH}$  (min) and  $V_{IL}$  (max) are reference levels for measuring timing of input signals. Transition times are measured between  $V_{IH}$  and  $V_{IL}$ .
- An initial pause of 200 $\mu\text{s}$  is required after power-up followed by 8  $\overline{\text{RAS}}$  only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 CAS before  $\overline{\text{RAS}}$  refresh cycles instead of 8  $\overline{\text{RAS}}$  only refresh cycles is required.
- The specified timings include buffer, loading and skew delay adders: 2ns minimum, 5ns maximum delay, no pulse shrinkage to the DRAM device timings. The data and  $\overline{\text{RAS}}$  signals are not buffered, which preserves the DRAMs access specifications of 60ns and 70ns.
- AC measurements assume  $t_T = 5\text{ns}$ .

## Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

| Symbol    | Parameter                                                         | -60 |      | -70 |      | Unit | Notes |
|-----------|-------------------------------------------------------------------|-----|------|-----|------|------|-------|
|           |                                                                   | Min | Max  | Min | Max  |      |       |
| $t_{RC}$  | Random Read or Write Cycle Time                                   | 110 | —    | 130 | —    | ns   |       |
| $t_{RP}$  | $\overline{\text{RAS}}$ Precharge Time                            | 40  | —    | 50  | —    | ns   |       |
| $t_{CP}$  | CAS Precharge Time                                                | 10  | —    | 10  | —    | ns   |       |
| $t_{RAS}$ | $\overline{\text{RAS}}$ Pulse Width                               | 60  | 10K  | 70  | 10K  | ns   |       |
| $t_{CAS}$ | $\overline{\text{CAS}}$ Pulse Width                               | 15  | 100K | 20  | 100K | ns   | 1     |
| $t_{ASR}$ | Row Address Setup Time                                            | 5   | —    | 5   | —    | ns   |       |
| $t_{RAH}$ | Row Address Hold Time                                             | 8   | —    | 8   | —    | ns   |       |
| $t_{ASC}$ | Column Address Setup Time                                         | 2   | —    | 2   | —    | ns   |       |
| $t_{CAH}$ | Column Address Hold Time                                          | 10  | —    | 10  | —    | ns   |       |
| $t_{RCD}$ | $\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time     | 18  | 40   | 18  | 45   | ns   | 2     |
| $t_{RAD}$ | $\overline{\text{RAS}}$ to Column Address Delay Time              | 13  | 25   | 13  | 30   | ns   | 3     |
| $t_{RSH}$ | $\overline{\text{RAS}}$ Hold Time                                 | 20  | —    | 25  | —    | ns   |       |
| $t_{CSH}$ | $\overline{\text{CAS}}$ Hold Time                                 | 58  | —    | 68  | —    | ns   |       |
| $t_{CRP}$ | $\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time | 10  | —    | 10  | —    | ns   |       |
| $t_{ODD}$ | $\overline{\text{OE}}$ to $D_{IN}$ Delay Time                     | 20  | —    | 25  | —    | ns   | 4     |
| $t_{DZO}$ | $\overline{\text{OE}}$ Delay Time from $D_{IN}$                   | -2  | —    | -2  | —    | ns   | 5     |
| $t_{DZC}$ | $\overline{\text{CAS}}$ Delay Time from $D_{IN}$                  | -2  | —    | -2  | —    | ns   | 5     |
| $t_{AR}$  | Column Address Hold Time Referenced to $\overline{\text{RAS}}$    | —   | —    | —   | —    | —    | 6     |
| $t_T$     | Transition Time (Rise and Fall)                                   | 3   | 50   | 3   | 50   | ns   |       |

- The minimum  $t_{CAS}$  requires  $t_{CSH}$  to be met for both writes and reads. Also, because of the buffer, the minimum  $t_{CAS}$  for a read cycle must be extended to guarantee the data out window ( $t_{OH}$ ) in the application. For example, a  $t_{CAS}$  of 15ns plus a minimum  $t_{OH}$  of 2ns would result in turning data out of the DIMM at 17ns (3ns before max  $t_{CAC}$  of 20ns).
- Operation within the  $t_{RCD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met. The  $t_{RCD}(\text{max})$  is specified as a reference point only: If  $t_{RCD}$  is greater than the specified  $t_{RCD}(\text{max})$  limit, then access time is controlled by  $t_{CAC}$ .
- Operation within the  $t_{RAD}(\text{max})$  limit ensures that  $t_{RAC}(\text{max})$  can be met. The  $t_{RAD}(\text{max})$  is specified as a reference point only: If  $t_{RAD}$  is greater than the specified  $t_{RAD}(\text{max})$  limit, then access time is controlled by  $t_{AA}$ .
- Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.
- Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
- This timing parameter is not applicable to this product, but applies to a related product in this family.

## 1M x 72 DRAM MODULE

## Write Cycle

| Symbol    | Parameter                                              | -60 |     | -70 |     | Unit | Notes |
|-----------|--------------------------------------------------------|-----|-----|-----|-----|------|-------|
|           |                                                        | Min | Max | Min | Max |      |       |
| $t_{WCS}$ | Write Command Set Up Time                              | 2   | —   | 2   | —   | ns   | 1     |
| $t_{WCH}$ | Write Command Hold Time                                | 17  | —   | 17  | —   | ns   |       |
| $t_{WP}$  | Write Command Pulse Width                              | 15  | —   | 15  | —   | ns   |       |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time            | 20  | —   | 25  | —   | ns   |       |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time            | 17  | —   | 22  | —   | ns   |       |
| $t_{WCR}$ | Write Command Hold Time Referenced to $\overline{RAS}$ | —   | —   | —   | —   | ns   | 2     |
| $t_{DHR}$ | Data Hold Time Referenced to $\overline{RAS}$          | —   | —   | —   | —   | ns   | 2     |
| $t_{DS}$  | $D_{IN}$ Setup Time                                    | -2  | —   | -2  | —   | ns   | 3     |
| $t_{DH}$  | $D_{IN}$ Hold Time                                     | 17  | —   | 20  | —   | ns   | 3     |

1.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$ , and  $t_{CPW}$  are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$  and  $t_{CPW} \geq t_{CPW}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell; If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.
2. This timing parameter is not applicable to this product, but applies to a related product in this family.
3. Data-in set-up and hold is measured from the latter of the two timings,  $\overline{CAS}$  or  $\overline{WE}$ .



## Read Cycle

| Symbol    | Parameter                                         | -60 |     | -70 |     | Unit | Notes |
|-----------|---------------------------------------------------|-----|-----|-----|-----|------|-------|
|           |                                                   | Min | Max | Min | Max |      |       |
| $t_{RAC}$ | Access Time from $\overline{RAS}$                 | —   | 60  | —   | 70  | ns   | 1, 2  |
| $t_{CAC}$ | Access Time from $\overline{CAS}$                 | —   | 20  | —   | 25  | ns   | 1, 2  |
| $t_{AA}$  | Access Time from Address                          | —   | 35  | —   | 40  | ns   | 1, 2  |
| $t_{OEA}$ | Access Time from $\overline{OE}$                  | —   | 20  | —   | 25  | ns   | 1, 2  |
| $t_{RCS}$ | Read Command Setup Time                           | 2   | —   | 2   | —   | ns   |       |
| $t_{RCH}$ | Read Command Hold Time to $\overline{CAS}$        | 2   | —   | 2   | —   | ns   | 3     |
| $t_{RRH}$ | Read Command Hold Time to $\overline{RAS}$        | 0   | —   | 0   | —   | ns   | 3     |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time      | 35  | —   | 40  | —   | ns   |       |
| $t_{CAL}$ | Column Address to $\overline{CAS}$ Lead Time      | —   | —   | —   | —   | ns   | 4     |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z               | 2   | —   | 2   | —   | ns   |       |
| $t_{ROH}$ | $\overline{RAS}$ Hold to Output Enable            | 5   | —   | 5   | —   | ns   |       |
| $t_{OH}$  | Output Data Hold Time                             | 2   | —   | 2   | —   | ns   |       |
| $t_{OHO}$ | Output Data Hold Time from $\overline{OE}$        | 2   | —   | 2   | —   | ns   |       |
| $t_{OEZ}$ | Output Buffer Turn-off Delay from $\overline{OE}$ | 2   | 20  | 2   | 20  | ns   | 5     |
| $t_{CDD}$ | $\overline{CAS}$ to $D_{IN}$ Delay Time           | 20  | —   | 20  | —   | ns   | 6     |
| $t_{OFF}$ | Output Buffer Turn-off delay                      | 2   | 20  | 2   | 20  | ns   |       |

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{CPA}$ ,  $t_{AA}$ ,  $t_{OEA}$ .
3. Either  $t_{RCH}$  or  $t_{RRH}$  must be satisfied.
4. This timing parameter is not applicable to this product, but applies to a related product in this family.
5.  $t_{OFF}$  (max) and  $t_{OEZ}$  (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. Either  $t_{CDD}$  or  $t_{ODD}$  must be satisfied.

## 1M x 72 DRAM MODULE

## Fast Page Mode Cycle

| Symbol     | Parameter                                                  | -60 |      | -70 |      | Unit | Notes |
|------------|------------------------------------------------------------|-----|------|-----|------|------|-------|
|            |                                                            | Min | Max  | Min | Max  |      |       |
| $t_{PC}$   | Fast Page Mode Cycle Time                                  | 40  | —    | 45  | —    | ns   |       |
| $t_{RASP}$ | Fast Page Mode $\overline{RAS}$ Pulse Width                | 60  | 100K | 70  | 100K | ns   |       |
| $t_{CPRH}$ | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 40  | —    | 45  | —    | ns   |       |
| $t_{CPA}$  | Access Time from $\overline{CAS}$ Precharge                | —   | 40   | —   | 45   | ns   | 1, 2  |

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of  $t_{RAC}$ ,  $t_{CAC}$ ,  $t_{CPA}$ ,  $t_{AA}$ ,  $t_{OEA}$ .

## Read-Modify-Write Cycle

| Symbol    | Parameter                                      | -60 |     | -70 |     | Unit | Notes |
|-----------|------------------------------------------------|-----|-----|-----|-----|------|-------|
|           |                                                | Min | Max | Min | Max |      |       |
| $t_{RWC}$ | Read-Modify-Write Cycle Time                   | 158 | —   | 188 | —   | ns   |       |
| $t_{RWD}$ | $\overline{RAS}$ to $\overline{WE}$ Delay Time | 83  | —   | 98  | —   | ns   | 1     |
| $t_{CWD}$ | $\overline{CAS}$ to $\overline{WE}$ Delay Time | 45  | —   | 55  | —   | ns   | 1     |
| $t_{AWD}$ | Column Address to $\overline{WE}$ Delay Time   | 58  | —   | 68  | —   | ns   | 1     |
| $t_{OEH}$ | $\overline{OE}$ Command Hold Time              | 15  | —   | 15  | —   | ns   |       |

1.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{CWD}$ ,  $t_{AWD}$ , and  $t_{CPW}$  are not restrictive parameters. They are included in the data sheet as electrical characteristics only. If  $t_{WCS} \geq t_{WCS}(\text{min.})$ , the entire cycle is an early write cycle and the data pin will remain open circuit (high impedance) through the entire cycle; If  $t_{RWD} \geq t_{RWD}(\text{min.})$ ,  $t_{CWD} \geq t_{CWD}(\text{min.})$ ,  $t_{AWD} \geq t_{AWD}(\text{min.})$  and  $t_{CPW} \geq t_{CPW}(\text{min.})$  (Fast Page Mode), the cycle is a Read-Modify-Write cycle and the data will contain read from the selected cell; If neither of the above sets of conditions are met, the condition of the data (at access time) is indeterminate.

## Fast Page Mode Read-Modify-Write Cycle

| Symbol     | Parameter                                                  | -60 |     | -70 |     | Unit | Notes |
|------------|------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|            |                                                            | Min | Max | Min | Max |      |       |
| $t_{PRWC}$ | Fast Page Mode Read-Modify-Write Cycle Time                | 83  | —   | 98  | —   | ns   |       |
| $t_{CPW}$  | $\overline{WE}$ Delay time from $\overline{CAS}$ Precharge | —   | —   | —   | —   | ns   | 1     |

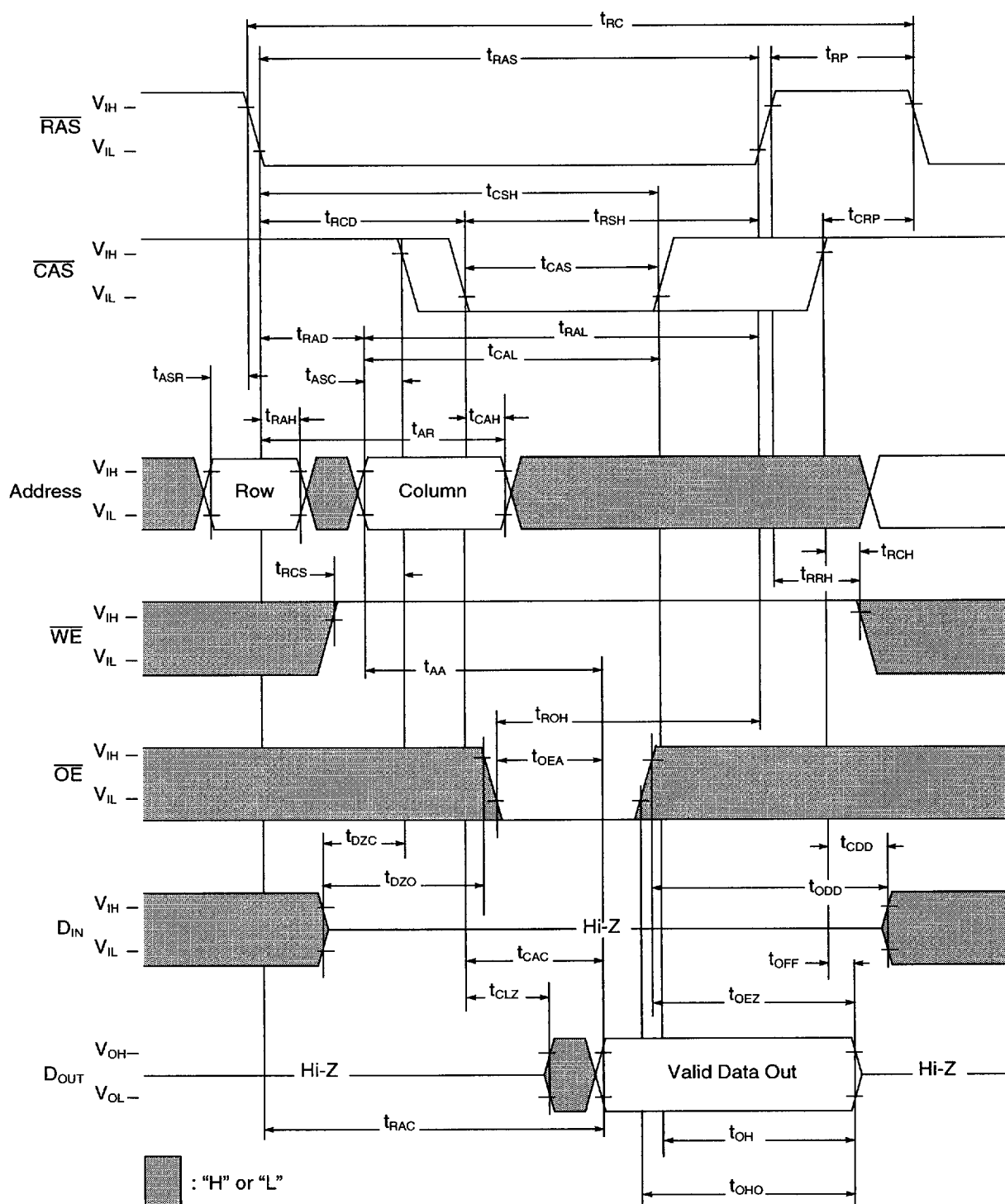
1. This timing parameter is not applicable to this product, but applies to a related product in this family.

## Refresh Cycle

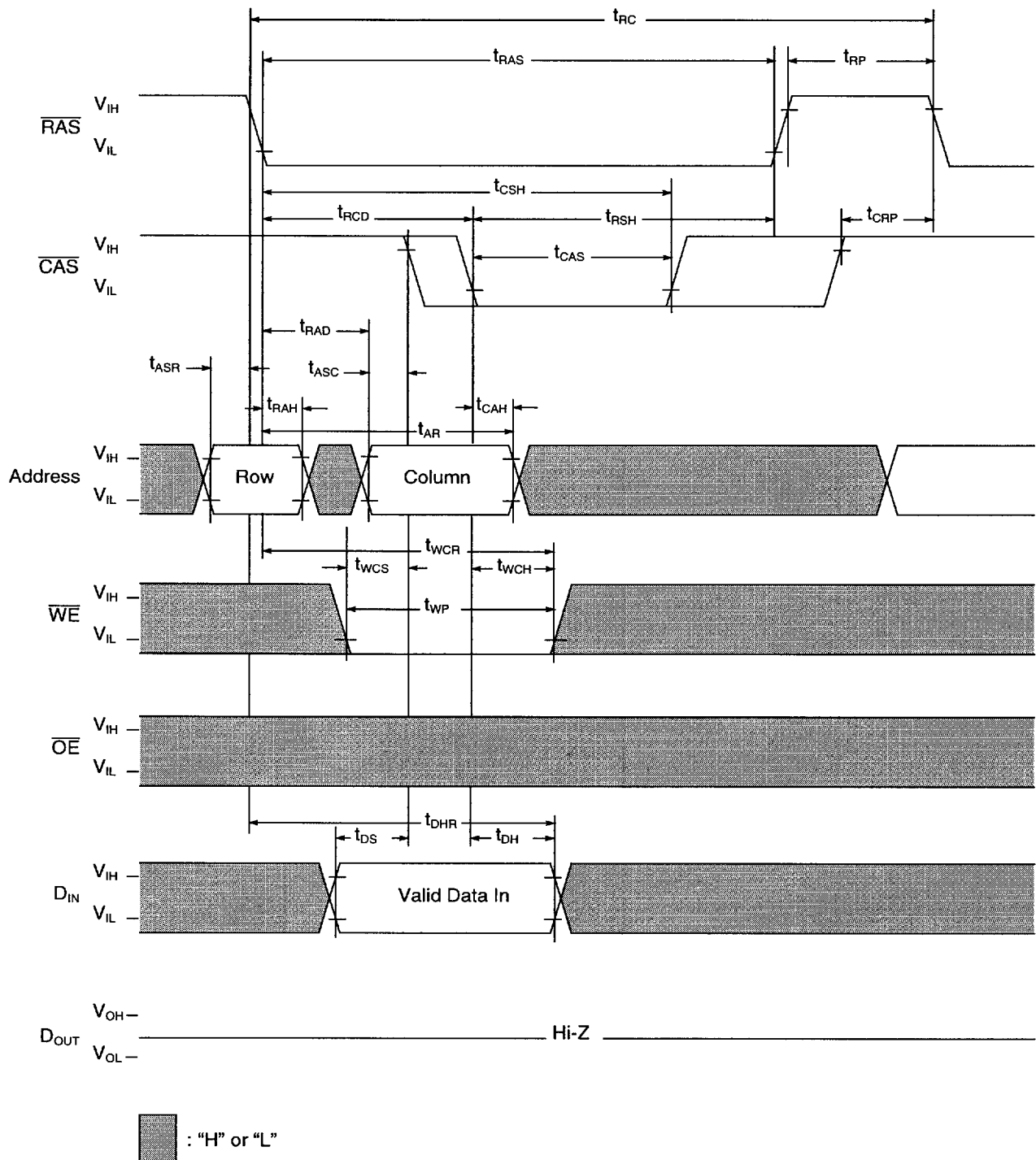
| Symbol                                     | Parameter                                                                   | -60 |     | -70 |     | Unit | Notes |
|--------------------------------------------|-----------------------------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                                            |                                                                             | Min | Max | Min | Max |      |       |
| $t_{CHR}$                                  | CAS Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)  | 8   | —   | 8   | —   | ns   |       |
| $t_{CSR}$                                  | CAS Setup Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 14  | —   | 14  | —   | ns   |       |
| $t_{WRP}$                                  | WE Setup Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)  | 15  | —   | 15  | —   | ns   |       |
| $t_{WRH}$                                  | WE Hold Time<br>( $\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)   | 8   | —   | 8   | —   | ns   |       |
| $t_{RPC}$                                  | $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time                    | 3   | —   | 3   | —   | ns   |       |
| $t_{REF}$                                  | Refresh Period                                                              | —   | 16  | —   | 16  | ms   | 1     |
| 1. 1024 refreshes are required every 16ms. |                                                                             |     |     |     |     |      |       |

## Presence Detect Read Cycle

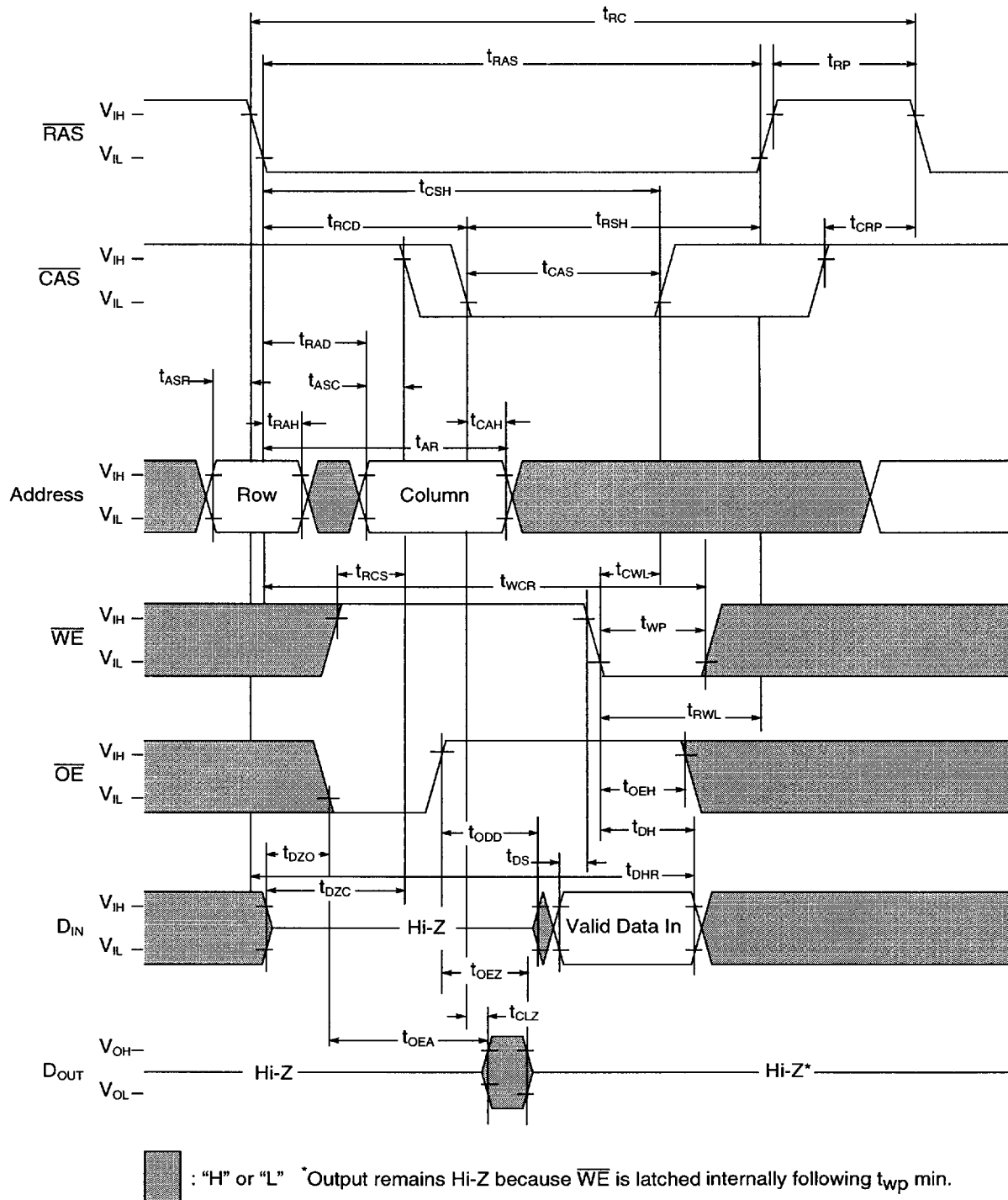
| Symbol                                                                                                                                                                                                        | Parameter                                              | -60 |     | -70 |     | Unit | Notes |
|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------|-----|-----|-----|-----|------|-------|
|                                                                                                                                                                                                               |                                                        | Min | Max | Min | Max |      |       |
| $t_{PD}$                                                                                                                                                                                                      | $\overline{PDE}$ to Valid Presence Detect Data         | —   | 10  | —   | 10  | ns   | 1     |
| $t_{PDOFF}$                                                                                                                                                                                                   | $\overline{PDE}$ Inactive to Presence Detects Inactive | 0   | 10  | 0   | 10  | ns   | 2     |
| 1. Measured with the specified current load and 100pF.<br>2. $t_{PDOFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels. |                                                        |     |     |     |     |      |       |



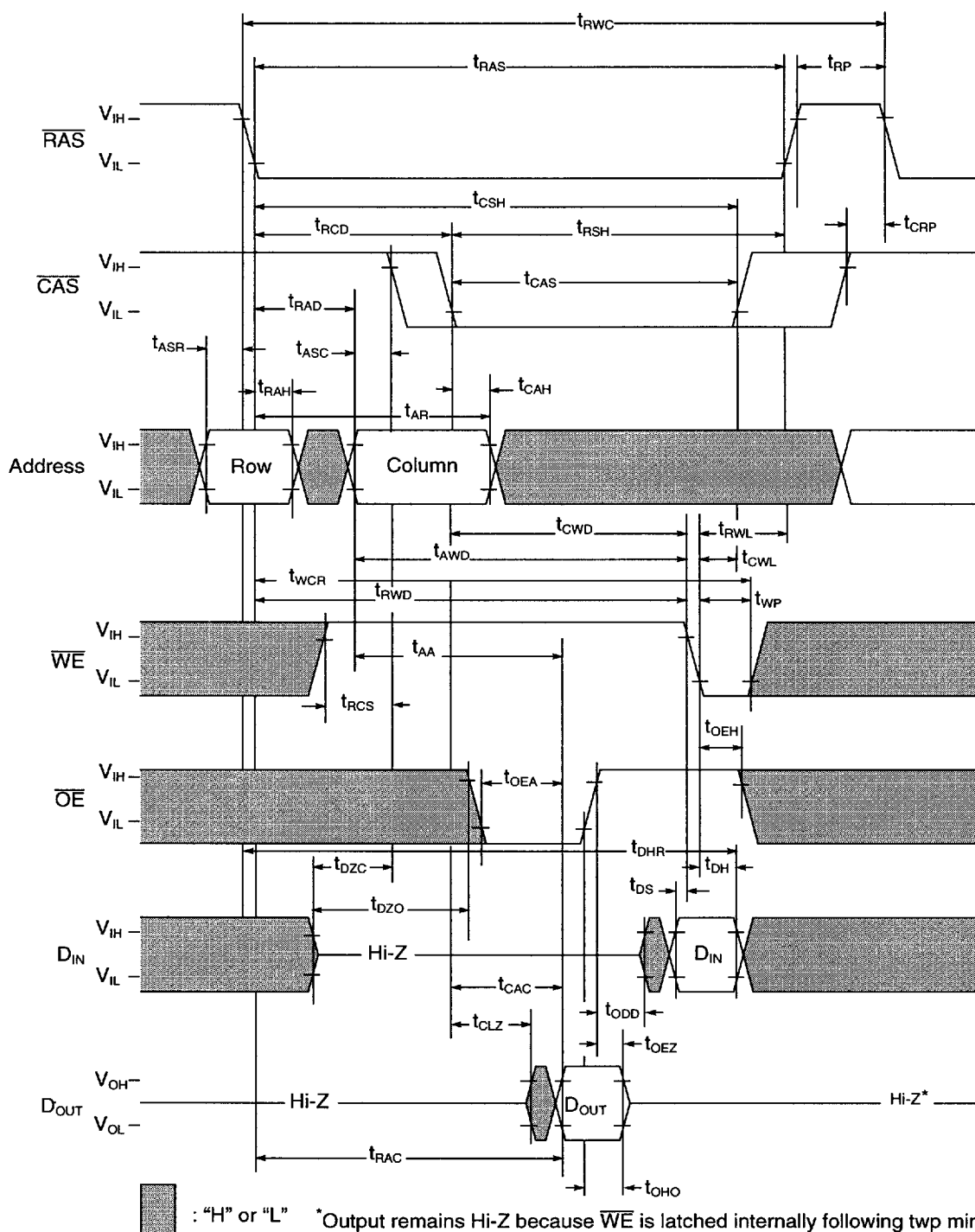
## Write Cycle (Early Write)



## Write Cycle (Late Write)



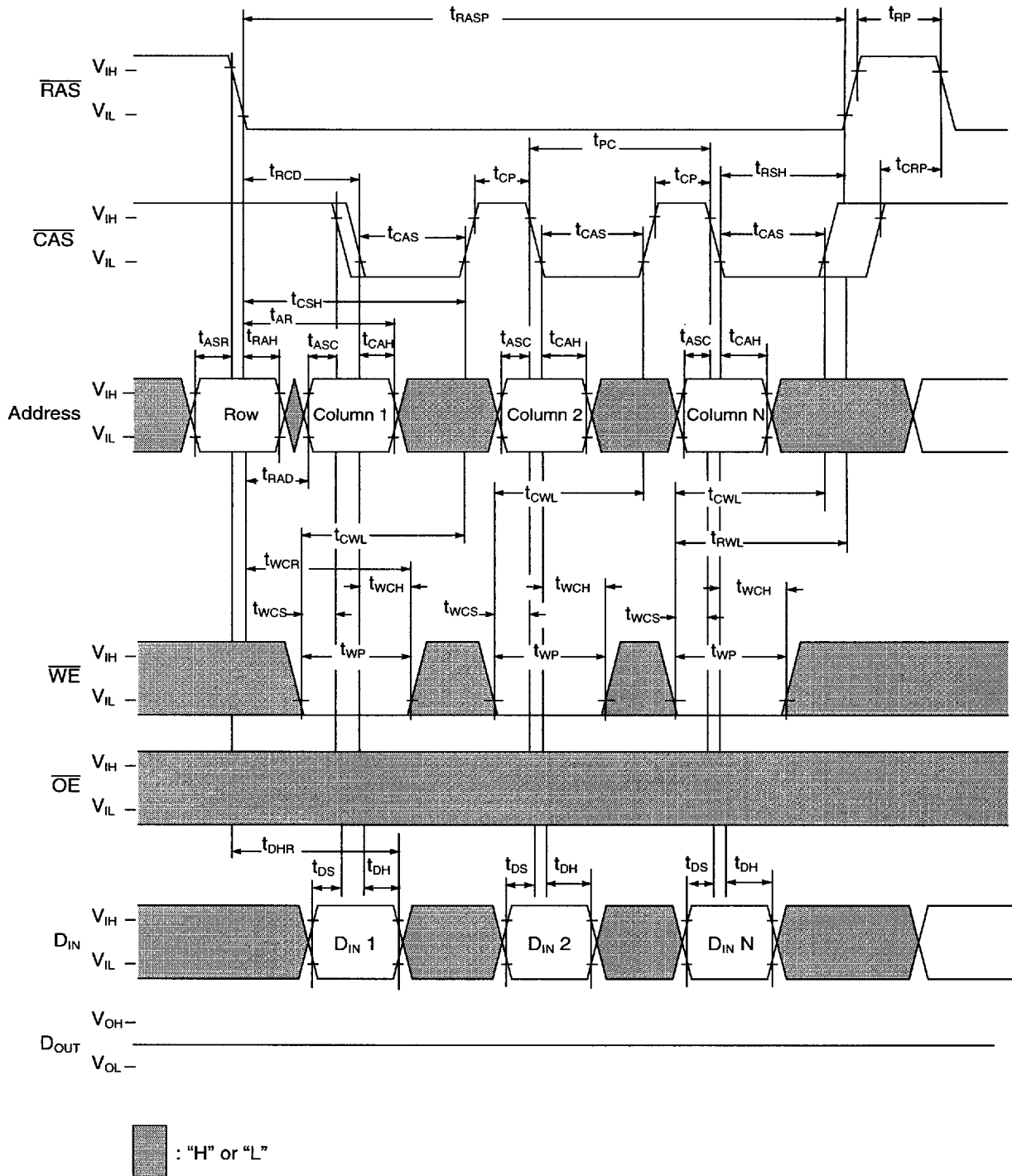
## Read-Modify-Write-Cycle

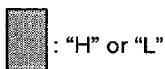




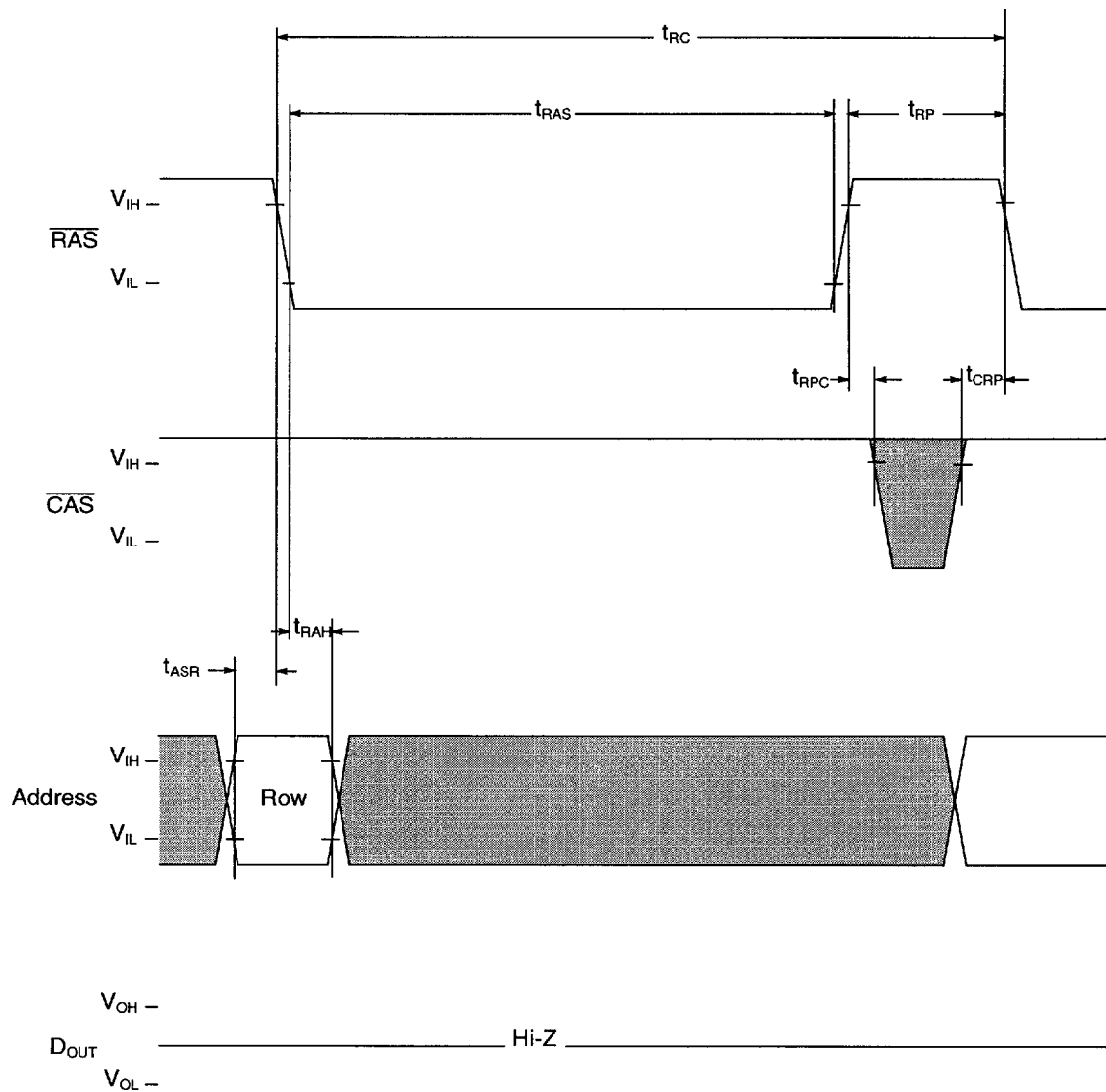


## Fast Page Mode Write Cycle





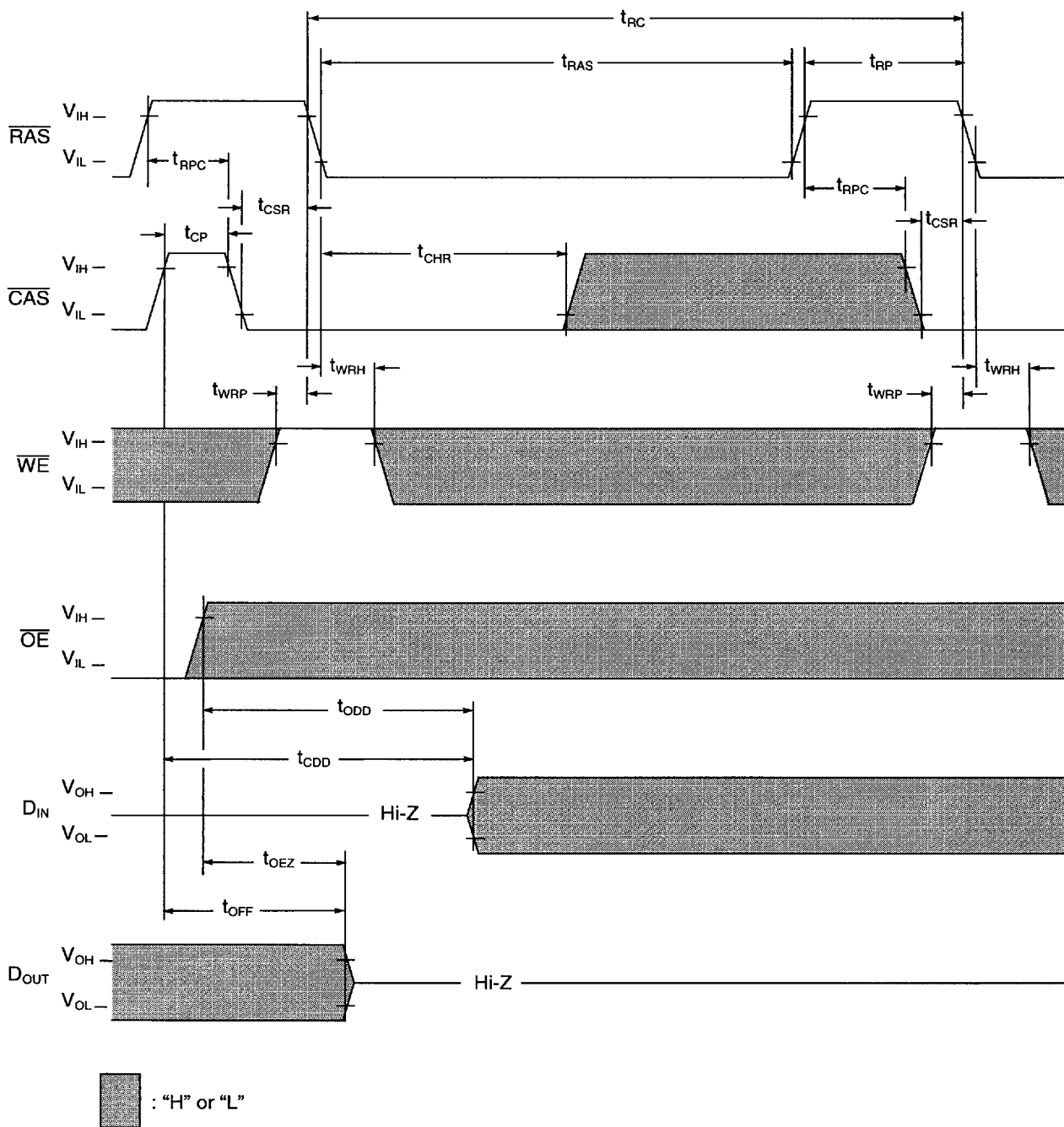
## RAS Only Refresh Cycle



■ : "H" or "L"

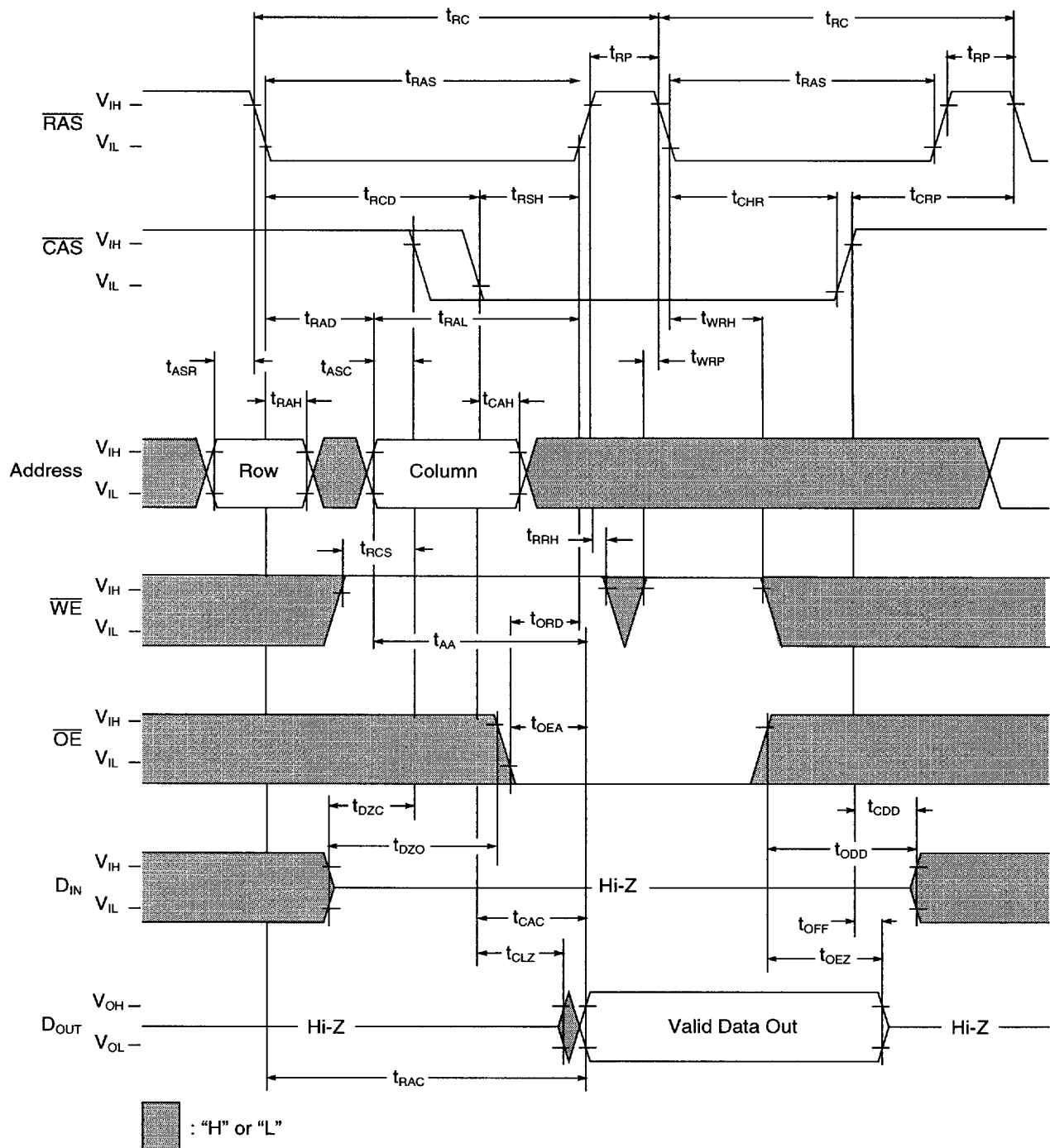
Note:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$ ,  $\text{D}_{\text{IN}}$  are "H" or "L"

## 1M x 72 DRAM MODULE

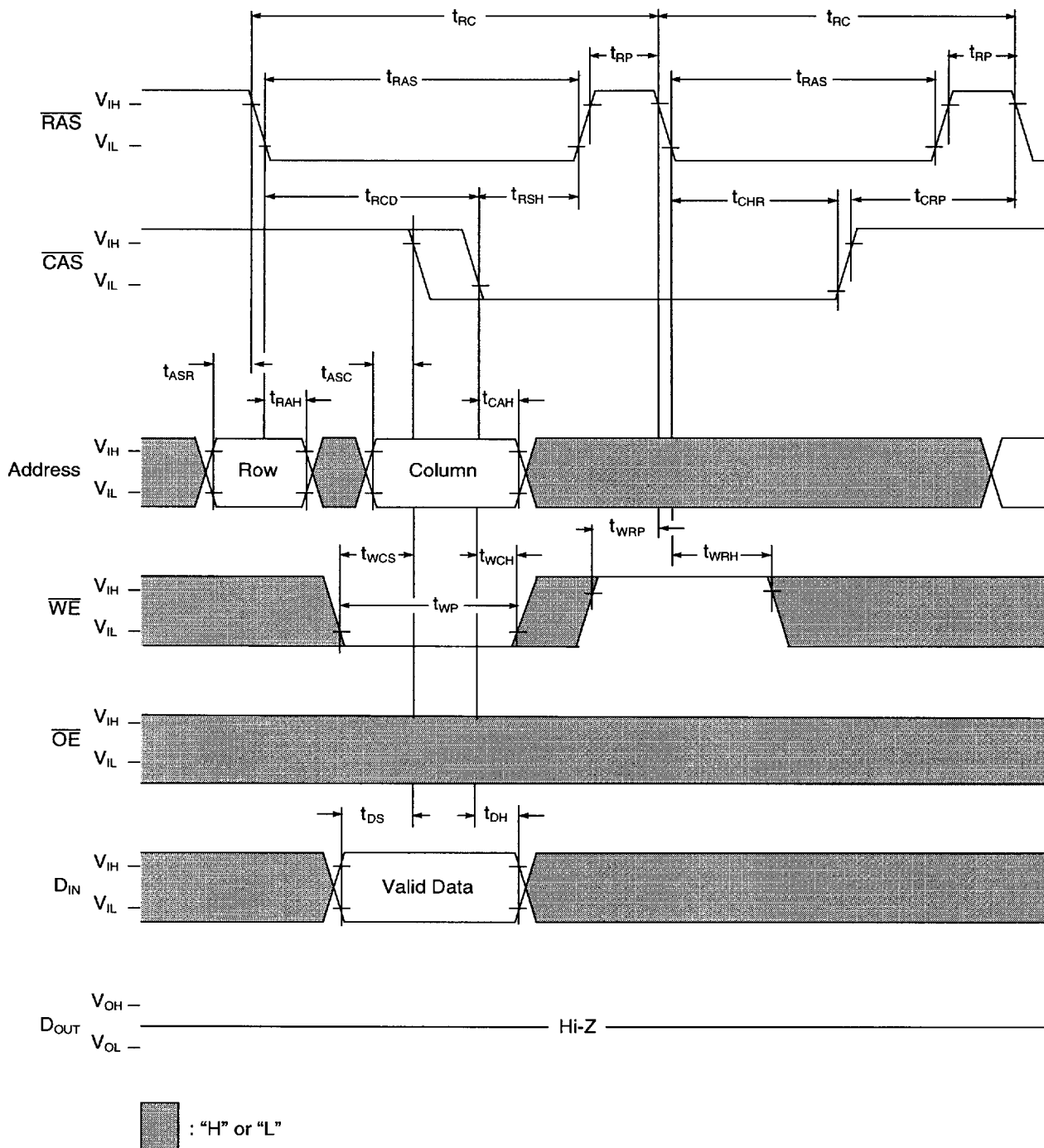
**CAS Before RAS Refresh Cycle**

NOTE: Address is "H" or "L"

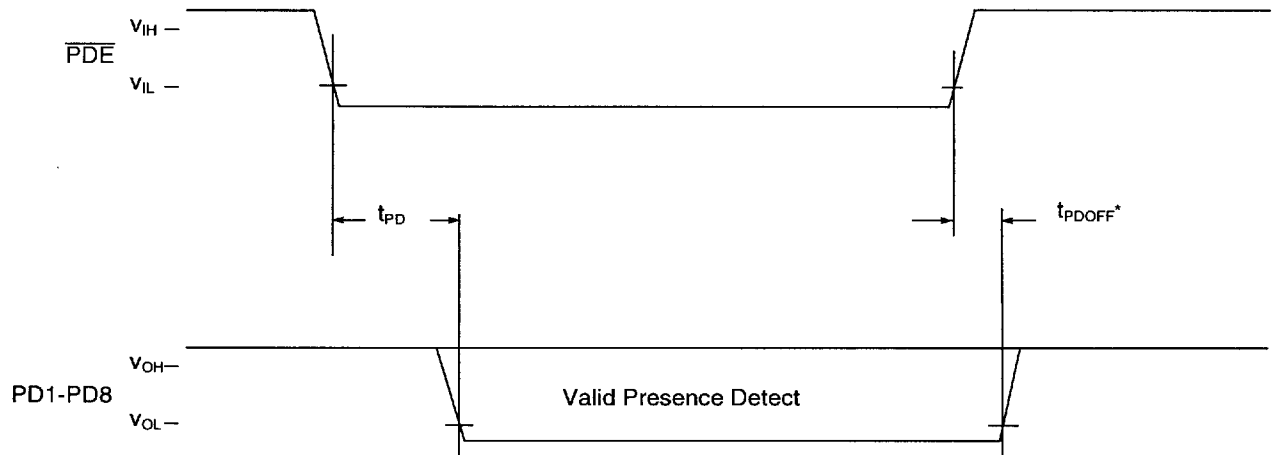
## Hidden Refresh Cycle (Read)



## Hidden Refresh Cycle (Write)



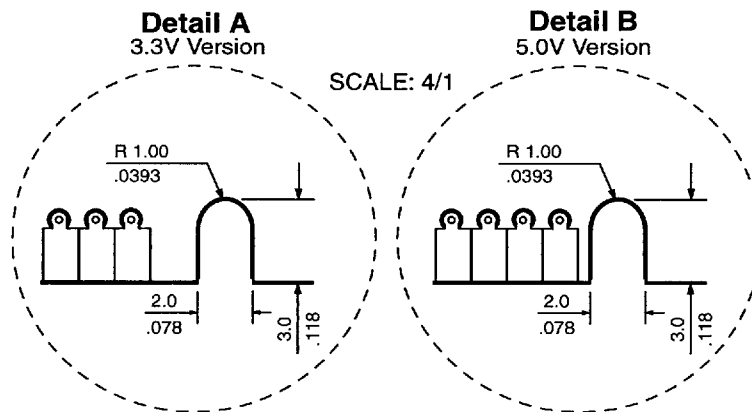
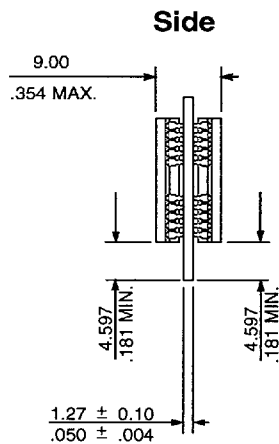
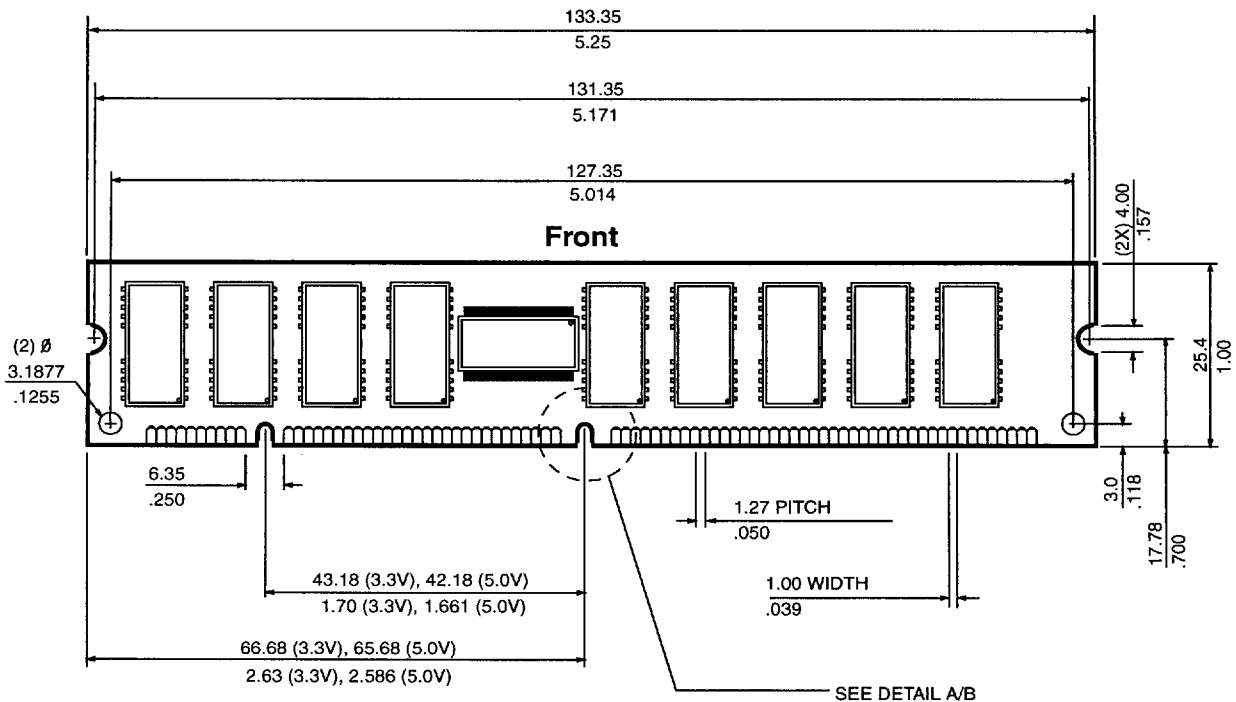
## Presence Detect Read Cycle



\*PD pins must be pulled high at next level of assembly

## 1M x 72 DRAM MODULE

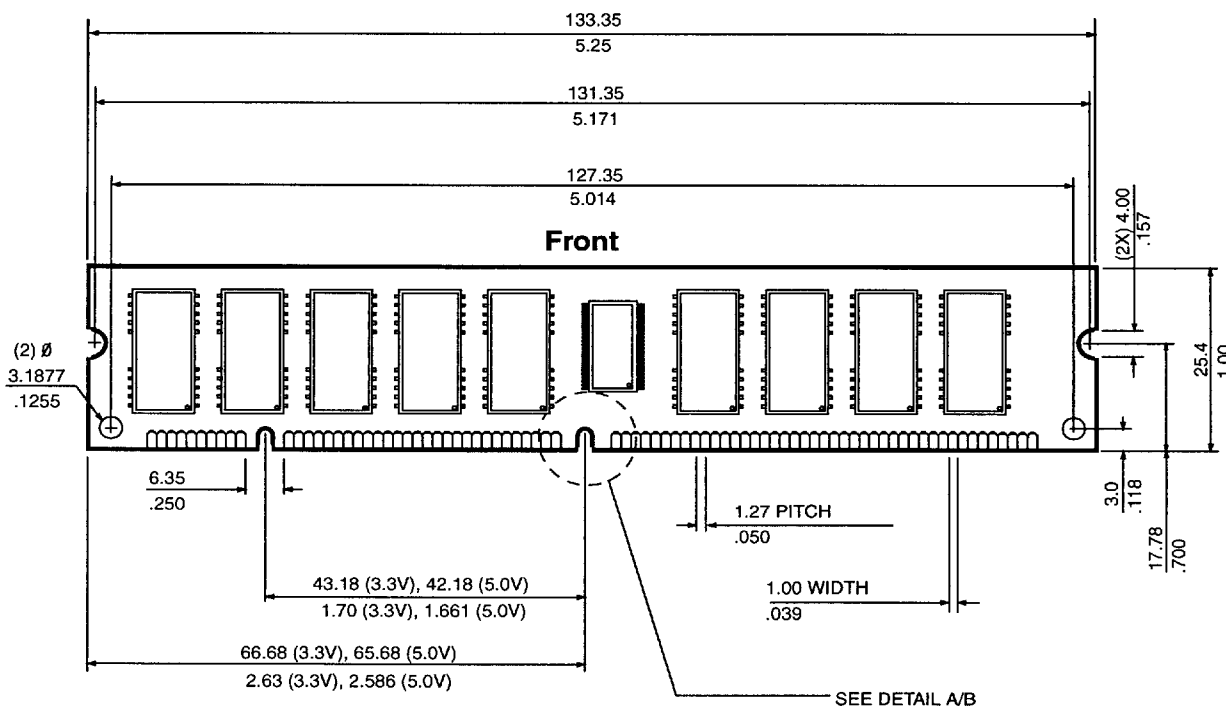
## Layout Drawing 3.3V/5.0V (SOJ)



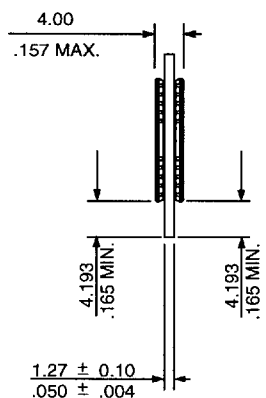
**Note:** All dimensions are typical unless otherwise stated. Millimeters  
Inches



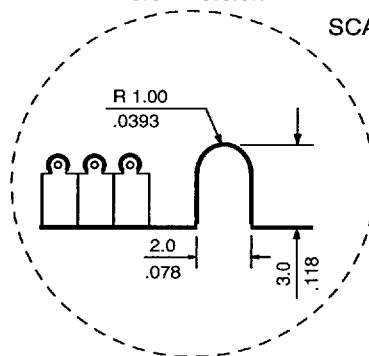
## Layout Drawing 3.3V/5.0V (TSOP)



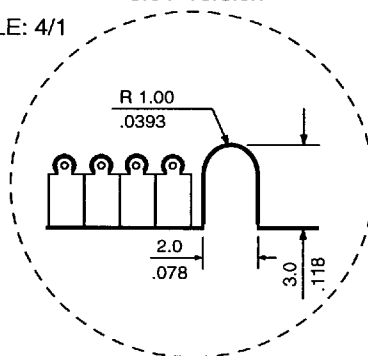
## Side



## Detail A 3.3V Version



## Detail B 5.0V Version



SCALE: 4/1

**Note:** All dimensions are typical unless otherwise stated.

Millimeters  
Inches



1M x 72 DRAM MODULE

Revision Log

| Rev  | Contents of Modification                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7/95 | Initial Release.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| 3/96 | Updated ordering information<br>Updated V <sub>OH</sub> , V <sub>OL</sub><br>Added timing: t <sub>CAS</sub><br>Improved timings: t <sub>CAH</sub> , t <sub>CRP</sub> , t <sub>DH</sub> , t <sub>RRH</sub> , t <sub>ROH</sub> , t <sub>OEZ</sub> , t <sub>CDD</sub> , t <sub>OFF</sub> , t <sub>OEH</sub> , t <sub>CHR</sub> , t <sub>CSR</sub><br>The CBR timing diagram was changed to allow $\overline{\text{CAS}}$ to remain low for back-to-back CBR cycles.<br>Hidden Refresh Cycle (Read) timing diagram was changed to show data being turned off with $\overline{\text{CAS}}$ not $\overline{\text{RAS}}$ |