

Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

		-60	-70
t_{RAC}	RAS Access Time	60ns	70ns
t_{CAC}	CAS Access Time	15ns	20ns
t_{AA}	Access Time From Address	30ns	35ns
t_{RC}	Cycle Time	110ns	130ns
t_{PC}	Fast Page Mode Cycle Time	40ns	45ns

- High Performance CMOS process
- Single $3.3 \pm 0.3V$ or $5.0 \pm 0.25V$ Power Supply
- Low active current consumption

- All inputs & outputs are TTL(5V) or LVTTL(3.3V) compatible
- Fast Page Mode access cycle
- Refresh Modes: RAS-Only, CBR, Hidden Refresh and Self Refresh
- 1024 refresh cycles distributed across 128ms
- 10/10 Addressing (Row/Column)
- Optimized for use in byte-write non-parity applications.
- Au contacts

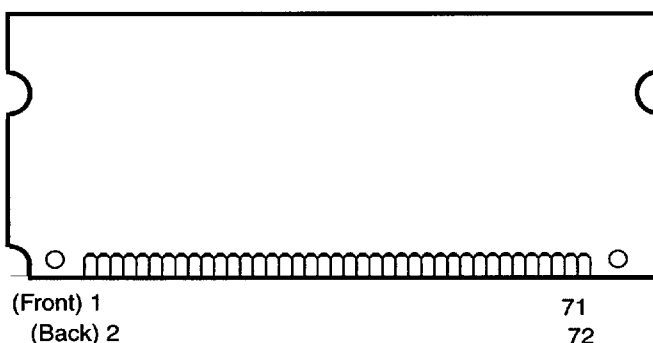
Description

The IBM11S1320LN/L are 4MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMMs). The module is organized as a 1Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with 2 1Mx16 TSOP devices, each in a 400mil package

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint.

This assembly is intended for use in space constrained and or low power applications.

Card Outline



Pin Description

$\overline{RAS}0, \overline{RAS}2$	Row Address Strobe
$\overline{CAS}0 - \overline{CAS}3$	Column Address Strobe
$\overline{WE}$	Read/write Input
A0 - A9	Address Inputs
DQ0-7, 9-16, 18-25, 27-34	Data Input/output
V_{CC}	Power (+3.3V or +5.0V)
V_{SS}	Ground
NC	No Connect
PD1 - PD7	Presence Detects

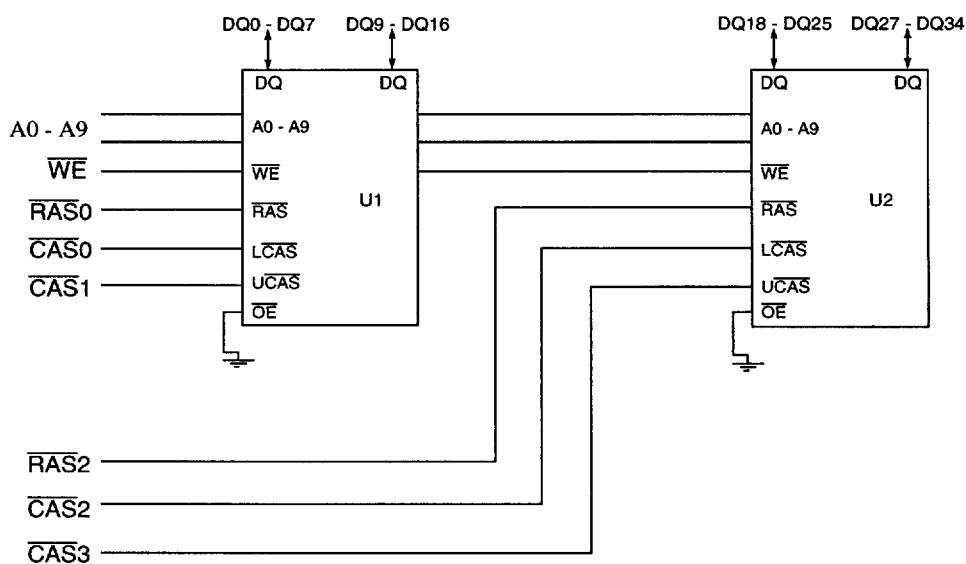
Pinout

Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name	Pin#	Name
1	V_{SS}	13	A1	25	DQ13	37	DQ18	49	DQ20	61	V_{CC}
2	DQ0	14	A2	26	DQ14	38	DQ19	50	DQ21	62	DQ32
3	DQ1	15	A3	27	DQ15	39	V_{SS}	51	DQ22	63	DQ33
4	DQ2	16	A4	28	A7	40	$\overline{CAS}0$	52	DQ23	64	DQ34
5	DQ3	17	A5	29	NC	41	$\overline{CAS}2$	53	DQ24	65	NC
6	DQ4	18	A6	30	V_{CC}	42	$\overline{CAS}3$	54	DQ25	66	PD2
7	DQ5	19	NC	31	A8	43	$\overline{CAS}1$	55	NC	67	PD3
8	DQ6	20	NC	32	A9	44	$\overline{RAS}0$	56	DQ27	68	PD4
9	DQ7	21	DQ9	33	NC	45	NC	57	DQ28	69	PD5
10	V_{CC}	22	DQ10	34	$\overline{RAS}2$	46	NC	58	DQ29	70	PD6
11	PD1	23	DQ11	35	DQ16	47	$\overline{WE}$	59	DQ31	71	PD7
12	A0	24	DQ12	36	NC	48	NC	60	DQ30	72	V_{SS}

Ordering Information

Part Number	Organization	Speed	Dimensions	Power	DRAM Die Revision	Notes
IBM11S1320LNA-60	1M x 32	60ns	2.35" x 1" x .0965"	3.3V	C	
IBM11S1320LNA-70	1M x 32	70ns	2.35" x 1" x .0965"	3.3V	C	
IBM11S1320LLA-60	1M x 32	60ns	2.35" x 1" x .0965"	5.0V	C	
IBM11S1320LLA-70	1M x 32	70ns	2.35" x 1" x .0965"	5.0V	C	
IBM11S1320LNB-60	1M x 32	60ns	2.35" x 1" x .0965"	3.3V	D	
IBM11S1320LNB-70	1M x 32	70ns	2.35" x 1" x .0965"	3.3V	D	
IBM11S1320LLB-60	1M x 32	60ns	2.35" x 1" x .0965"	5.0V	D	
IBM11S1320LLB-70	1M x 32	70ns	2.35" x 1" x .0965"	5.0V	D	

Block Diagram



Truth Table

Function		$\overline{\text{RAS}}$	$\overline{\text{CAS}}$	$\overline{\text{WE}}$	Row Address	Column Address	All DQ bits
Standby		H	X	X	X	X	High Impedance
Read		L	L	H	Row	Col	Valid Data Out
Early-Write		L	L	L	Row	Col	Valid Data In
Fast Page Mode - Read: 1st Cycle		L	H→L	H	Row	Col	Valid Data Out
Subsequent Cycles		L	H→L	H	N/A	Col	Valid Data Out
Fast Page Mode - Write: 1st Cycle		L	H→L	L	Row	Col	Valid Data In
Subsequent Cycles		L	H→L	L	N/A	Col	Valid Data In
$\overline{\text{RAS}}$ -Only Refresh		L	H	X	Row	N/A	High Impedance
$\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$ Refresh		H→L	L	H	X	X	High Impedance
Hidden Refresh	Read	L→H→L	L	H	Row	Col	Data Out
	Write	L→H→L	L	H	Row	Col	Data In
Self Refresh		H→L	L	H	X	X	High Impedance

Presence Detect

Pin	-60	-70
PD1	NC	NC
PD2	V _{SS}	V _{SS}
PD3	V _{SS}	V _{SS}
PD4	NC	NC
PD5	NC	V _{SS}
PD6	NC	NC
PD7	NC	NC
1. NC= OPEN, V _{SS} = GND		



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units	Notes
		3.3 Volt	5.0 Volt		
V_{CC}	Power Supply Voltage	-0.5 to + 4.6	-1.0 to + 7.0	V	1
V_{IN}	Input Voltage	-0.7 to min ($V_{CC} + 0.5$, 4.6)	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
V_{OUT}	Output Voltage	-0.5 to min ($V_{CC} + 0.5$, 4.6)	-0.5 to min ($V_{CC} + 0.5$, 7.0)	V	1
T_{OPR}	Operating Temperature	0 to +70	0 to +70	°C	1
T_{STG}	Storage Temperature	-55 to +150	-55 to +150	°C	1
P_D	Power Dissipation	0.6	2.2	W	1, 2
I_{OUT}	Short Circuit Output Current	50	50	mA	1

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power occurs when all banks are active.

Recommended DC Operating Conditions ($T_A = 0$ to 70°C)

Symbol	Parameter	3.3 Volt			5.0 Volt			Units	Notes
		Min	Typ	Max	Min	Typ	Max		
V_{CC}	Supply Voltage	3.0	3.3	3.6	4.75	5.0	5.25	V	1
V_{IH}	Input High Voltage	2.0	—	$V_{CC} + 0.5$	2.4	—	$V_{CC} + 0.5$	V	1, 2
V_{IL}	Input Low Voltage	-0.5	—	0.8	-0.5	—	0.8	V	1, 2

1. All voltages referenced to V_{SS} .
2. V_{IH} may overshoot to $V_{CC} + 1.2\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ with 3.3 Volt, or $V_{CC} + 2.0\text{V}$ for pulse widths of $\leq 4.0\text{ns}$ (or $V_{CC} + 1.0\text{V}$ for $\leq 8.0\text{ns}$) with 5.0 Volt. Additionally, V_{IL} may undershoot to -1.2V for pulse widths $\leq 4.0\text{ns}$ with 3.3 Volt, or to -2.0V for pulse widths $\leq 4.0\text{ns}$ (or -1.0V for $\leq 8.0\text{ns}$) with 5.0 Volt. Pulse widths measured at 50% points with amplitude measured peak to DC reference.

Capacitance ($T_A = 0$ to $+70^{\circ}\text{C}$, $V_{CC} = 3.3$ 0.3V or 5.0 0.25V)

Symbol	Parameter	Max	Units	Notes
C_{I1}	Input Capacitance (A0-A9)	28	pF	
C_{I2}	Input Capacitance ($\overline{\text{RAS}}$)	16	pF	
C_{I3}	Input Capacitance ($\overline{\text{CAS}}$)	15	pF	
C_{I4}	Input Capacitance ($\overline{\text{WE}}$)	28	pF	
C_{IO}	Input - Output Capacitance (DQ0-DQ34)	16	pF	

DC Electrical Characteristics (T_A = 0 to +70°C, V_{CC} = 3.3 0.3V or 5.0 0.25V)

Symbol	Parameter		3.3 Volt		5.0 Volt		Units	Notes
			Min	Max	Min	Max		
I _{CC1}	Operating Current Average Power Supply Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Address Cycling: $t_{\text{RC}} = t_{\text{RC min}}$)	-60	—	410	—	410	mA	1, 2, 3
		-70	—	360	—	360		
I _{CC2}	Standby Current (TTL) Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} \geq V_{\text{IH}}$)		—	4	—	4	mA	
I _{CC3}	$\overline{\text{RAS}}$ Only Refresh Current Average Power Supply Current, $\overline{\text{RAS}}$ Only Mode ($\overline{\text{RAS}}$ Cycling, $\overline{\text{CAS}} \geq V_{\text{IH}}$: $t_{\text{RC}} = t_{\text{RC min}}$)	-60	—	410	—	410	mA	1, 3
		-70	—	360	—	360		
I _{CC4}	Fast Page Mode Current Average Power Supply Current, Fast Page Mode ($\overline{\text{RAS}} = V_{\text{IL}}$, $\overline{\text{CAS}}$, Address Cycling: $t_{\text{PC}} = t_{\text{PC min}}$)	-60	—	180	—	180	mA	1, 2, 3
		-70	—	160	—	160		
I _{CC5}	Standby Current (CMOS) Power Supply Standby Current ($\overline{\text{RAS}} = \overline{\text{CAS}} = V_{\text{CC}} - 0.2\text{V}$)		—	0.4	—	0.4	mA	
I _{CC6}	$\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Current Average Power Supply Current, $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Mode ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$, Cycling: $t_{\text{RC}} = t_{\text{RC min}}$)	-60	—	410	—	410	mA	1, 3
		-70	—	360	—	360		
I _{CC7}	Self Refresh Current Average Power Supply Current during Self Refresh CBR cycle with $\overline{\text{RAS}} \geq t_{\text{RASS}}$ (min); $\overline{\text{CAS}}$ held low; $\overline{\text{WE}} = V_{\text{CC}} - 0.2\text{V}$; Addresses and $\text{D}_{\text{IN}} = V_{\text{CC}} - 0.2\text{V}$ or 0.2V .	-60	—	400	—	600	μA	
		-70	—	400	—	600		
I _{I(L)}	Input Leakage Current Input Leakage Current, any input ($0.0 \leq V_{\text{IN}} \leq (V_{\text{CC}} - 6.0\text{V})$) All Other Pins Not Under Test = 0V	$\overline{\text{RAS}}$	-10	+10	-10	+10	μA	
		$\overline{\text{CAS}}$	-10	+10	-10	+10		
		All others	-20	+20	-20	+20		
I _{O(L)}	Output Leakage Current (D_{OUT} is disabled, $0.0 \leq V_{\text{OUT}} \leq V_{\text{CC}}$)		-10	+10	-10	+10	μA	
V _{OH}	Output High Level Output "H" Level Voltage ($I_{\text{OUT}} = -5\text{mA}$ @ 2.4V)		2.4	—	2.4	—	V	
V _{OL}	Output Low Level Output "L" Level Voltage ($I_{\text{OUT}} = +4.2\text{mA}$ @ 0.4V)		—	0.4	—	0.4	V	
1. I _{CC1} , I _{CC3} , I _{CC4} and I _{CC6} depend on cycle rate. 2. I _{CC1} , I _{CC4} depend on output loading. Specified values are obtained with the output open. 3. Address can be changed once or less while $\overline{\text{RAS}} = V_{\text{IL}}$. In the case of I _{CC4} , it can be changed once or less when $\overline{\text{CAS}} = V_{\text{IH}}$.								

AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{CC} = 3.3 \pm 0.3\text{V}$ or $5.0 \pm 0.25\text{V}$)

1. An initial pause of $200\mu\text{s}$ is required after power-up followed by 8 $\overline{\text{RAS}}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles instead of 8 $\overline{\text{RAS}}$ only refresh cycles is required.
2. AC measurements assume $t_T=5\text{ns}$.
3. $V_{IH}(\text{min.})$ and $V_{IL}(\text{max.})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
4. When both $\overline{\text{CAS0}}$ & $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ & $\overline{\text{CAS3}}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{\text{CAS0}}$ & $\overline{\text{CAS1}}$ or $\overline{\text{CAS2}}$ & $\overline{\text{CAS3}}$ (CAS'S TO THE SAME DRAM) cannot be staggered within the same read/write cycle.

Read, Write, and Refresh Cycles (Common Parameters)

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RC}	Random Read or Write Cycle Time	110	128K	130	128K	ns	
t_{RP}	$\overline{\text{RAS}}$ Precharge Time	40	—	50	—	ns	
t_{CP}	$\overline{\text{CAS}}$ Precharge Time	10	—	10	—	ns	
t_{RAS}	$\overline{\text{RAS}}$ Pulse Width	60	10K	70	10K	ns	
t_{CAS}	$\overline{\text{CAS}}$ Pulse Width	15	10K	20	10K	ns	
t_{ASR}	Row Address Setup Time	0	—	0	—	ns	
t_{RAH}	Row Address Hold Time	10	—	10	—	ns	
t_{ASC}	Column Address Setup Time	0	—	0	—	ns	
t_{CAH}	Column Address Hold Time	15	—	15	—	ns	
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	20	45	20	50	ns	1
t_{RAD}	$\overline{\text{RAS}}$ to Column Address Delay Time	15	30	15	35	ns	2
t_{RSH}	$\overline{\text{RAS}}$ Hold Time	15	—	20	—	ns	
t_{CSH}	$\overline{\text{CAS}}$ Hold Time	60	—	70	—	ns	
t_{CRP}	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	5	—	5	—	ns	
t_{DZC}	$\overline{\text{CAS}}$ Delay Time from D_{IN}	0	—	0	—	ns	
t_T	Transition Time (Rise and Fall)	3	30	3	30	ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{\text{RAS}}$	—	—	—	—	ns	3

1. Operation within the $t_{RCD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only: if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled by t_{CAC} .

2. Operation within the $t_{RAD}(\text{max})$ limit ensures that $t_{RAC}(\text{max})$ can be met. $t_{RAD}(\text{max})$ is specified as a reference point only: If t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled by t_{AA} .

3. This timing parameter is not applicable to this product, but applies to a related product in this family.

Write Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{WCS}	Write Command Set Up Time	0	—	0	—	ns	
t_{WCH}	Write Command Hold Time	15	—	15	—	ns	
t_{WP}	Write Command Pulse Width	15	—	15	—	ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	15	—	20	—	ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	15	—	20	—	ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DHR}	Data Hold Time Referenced to $\overline{RAS}$	—	—	—	—	ns	1
t_{DS}	D_{IN} Setup Time	0	—	0	—	ns	2
t_{DH}	D_{IN} Hold Time	15	—	15	—	ns	2

1. This timing parameter is not applicable to this product, but applies to a related product in this family.
2. These parameters are referenced to $\overline{CAS}$ 0,2 or $\overline{CAS}$ 1,3 leading edge in early write cycles.

Read Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{RAC}	Access Time from $\overline{RAS}$	—	60	—	70	ns	1, 2, 3
t_{CAC}	Access Time from $\overline{CAS}$	—	15	—	20	ns	1, 3
t_{AA}	Access Time from Address	—	30	—	35	ns	2, 3
t_{RCS}	Read Command Setup Time	0	—	0	—	ns	
t_{RCH}	Read Command Hold Time to $\overline{CAS}$	0	—	0	—	ns	4
t_{RRH}	Read Command Hold Time to $\overline{RAS}$	5	—	5	—	ns	4
t_{RAL}	Column Address to $\overline{RAS}$ Lead Time	30	—	35	—	ns	
t_{CAL}	Column Address to $\overline{CAS}$ Lead Time	30	—	35	—	ns	
t_{CLZ}	$\overline{CAS}$ to Output in Low-Z	0	—	0	—	ns	3
t_{OH}	Output Data Hold Time	3	—	3	—	ns	
t_{CDD}	$\overline{CAS}$ to D_{IN} Delay Time	15	—	20	—	ns	
t_{OFF}	Output Buffer Turn-off Delay	—	15	—	20	ns	5

1. Operation within the $t_{RCD}(\max.)$ limit ensures that $t_{RAC}(\max.)$ can be met. $t_{RCD}(\max.)$ is specified as a reference point only. If t_{RCD} is greater than the specified $t_{RCD}(\max.)$ limit, then access time is controlled by t_{CAC} .
2. Operation within the $t_{RAD}(\max.)$ limit ensures that $t_{RAC}(\max.)$ can be met. $t_{RAD}(\max.)$ is specified as a reference point only. If t_{RAD} is greater than the specified $t_{RAD}(\max.)$ limit, then access time is controlled by t_{AA} .
3. Measured with the specified current load and 100pF.
4. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
5. $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

Fast Page Mode Cycle

Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{PC}	Fast Page Mode Cycle Time	40	—	45	—	ns	
t_{RASP}	Fast Page Mode $\overline{RAS}$ Pulse Width	60	100K	70	100K	ns	
t_{CPRH}	$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	35	—	40	—	ns	
t_{CPA}	Access Time from $\overline{CAS}$ Precharge	—	35	—	40	ns	1

1. Measured with the specified current load and 100pF.

Refresh Cycle

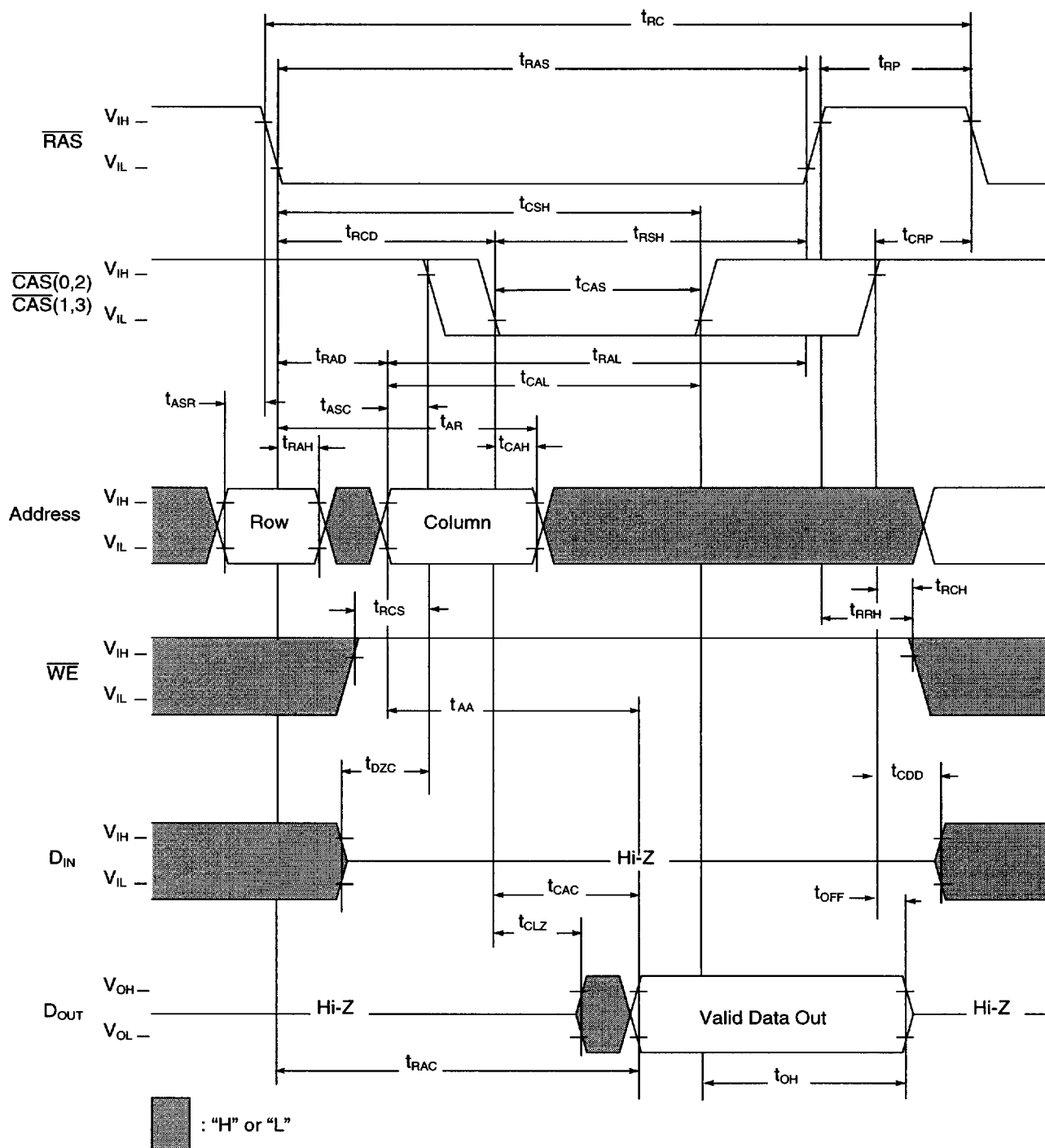
Symbol	Parameter	-60		-70		Units	Notes
		Min	Max	Min	Max		
t_{CHR}	$\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	20	—	20	—	ns	
t_{CSR}	$\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRP}	$\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{WRH}	$\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle)	10	—	10	—	ns	
t_{RPC}	$\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time	5	—	5	—	ns	
t_{REF}	Refresh Period	—	128	—	128	ms	1

1. 1024 refreshes are required every 128ms.

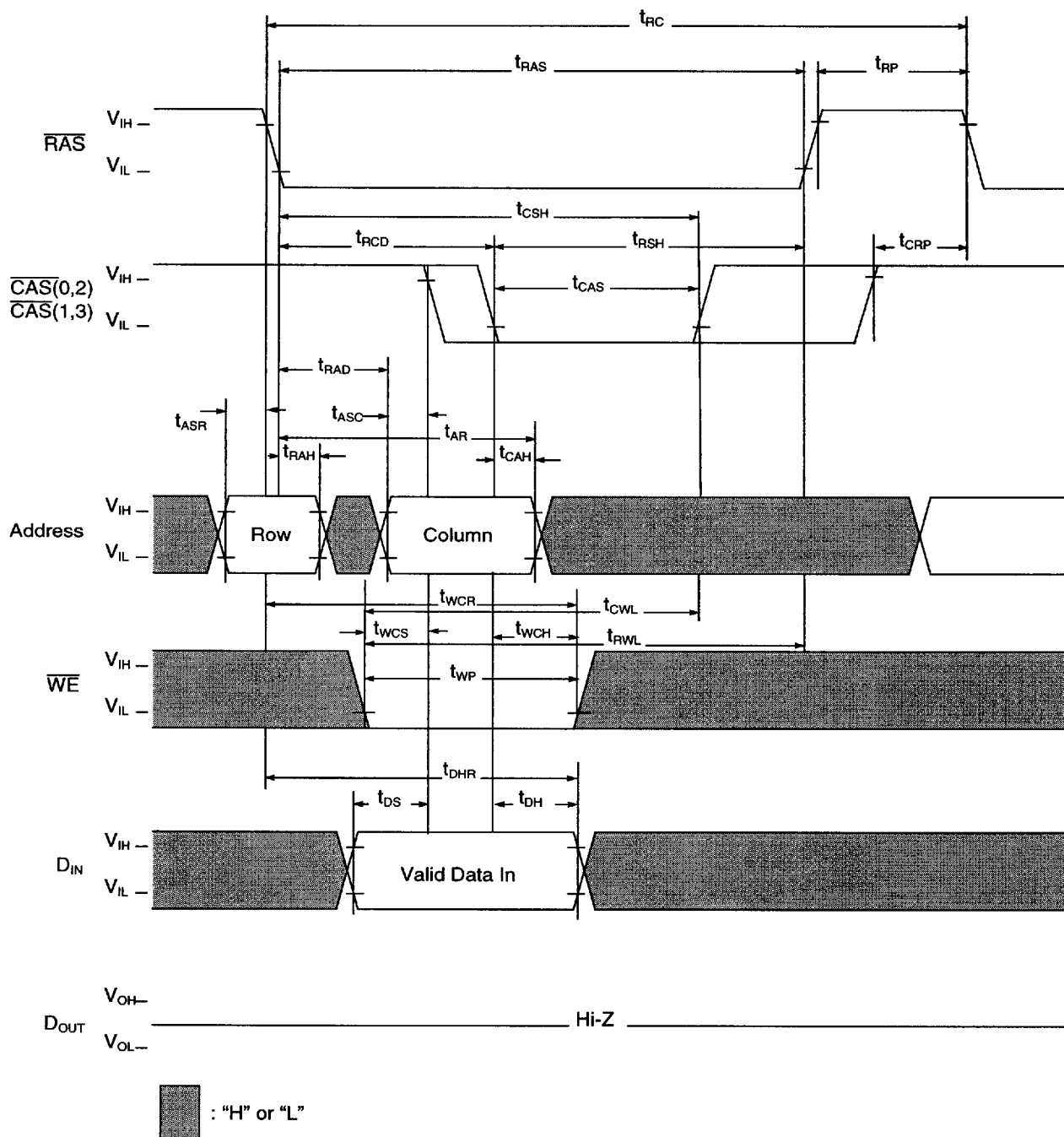
Self Refresh Cycle

Symbol	Parameter	-50		-60		-70		-80		Units	Notes
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.		
t_{RASS}	$\overline{RAS}$ Pulse Width During Self Refresh Cycle	100	—	100	—	100	—	100	—	μs	1
t_{RPS}	$\overline{RAS}$ Precharge Time During Self Refresh Cycle	95	—	110	—	130	—	150	—	ns	1
t_{CHS}	$\overline{CAS}$ Hold Time During Self Refresh Cycle	-50	—	-50	—	-50	—	-50	—	ns	1

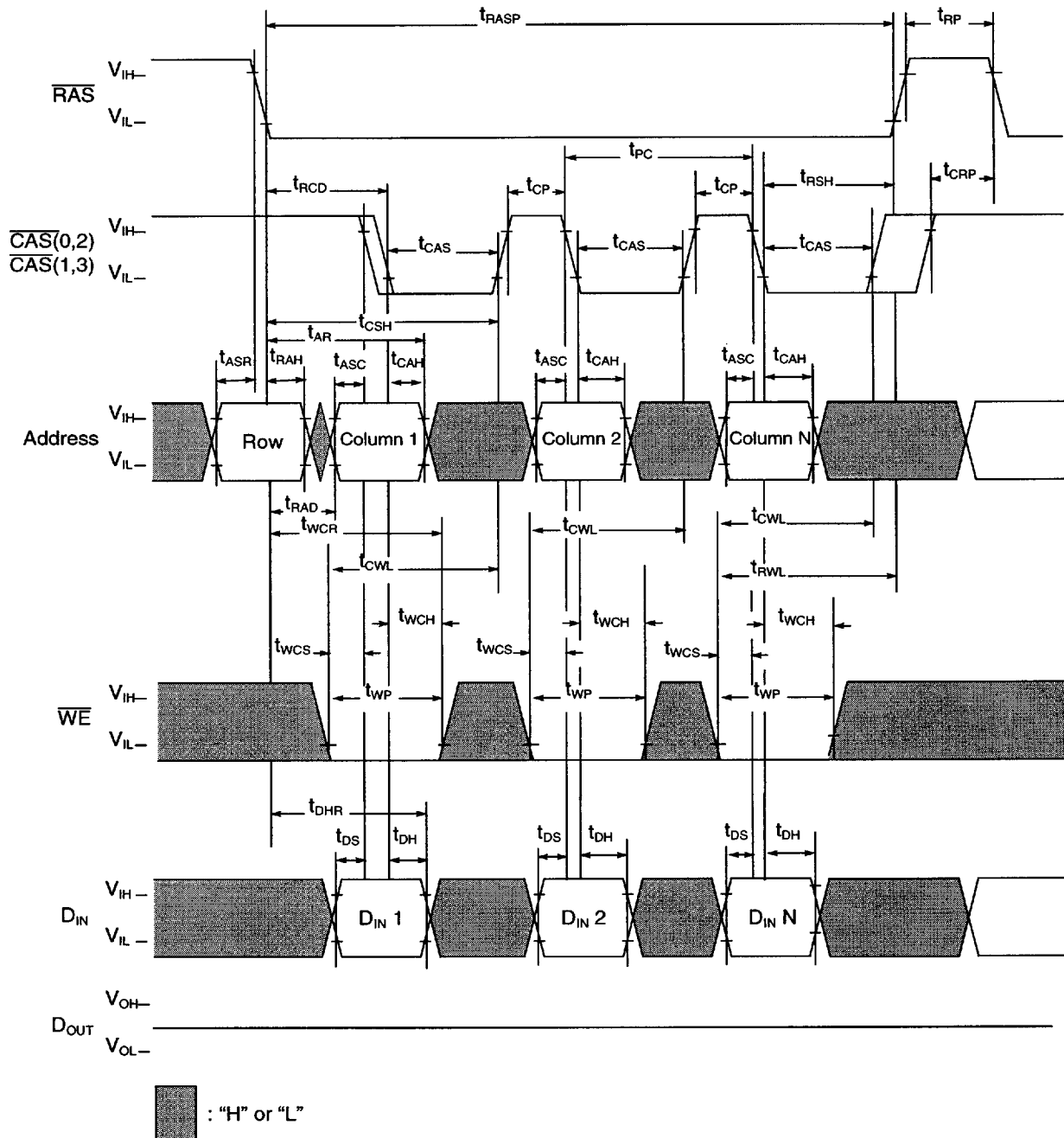
1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.



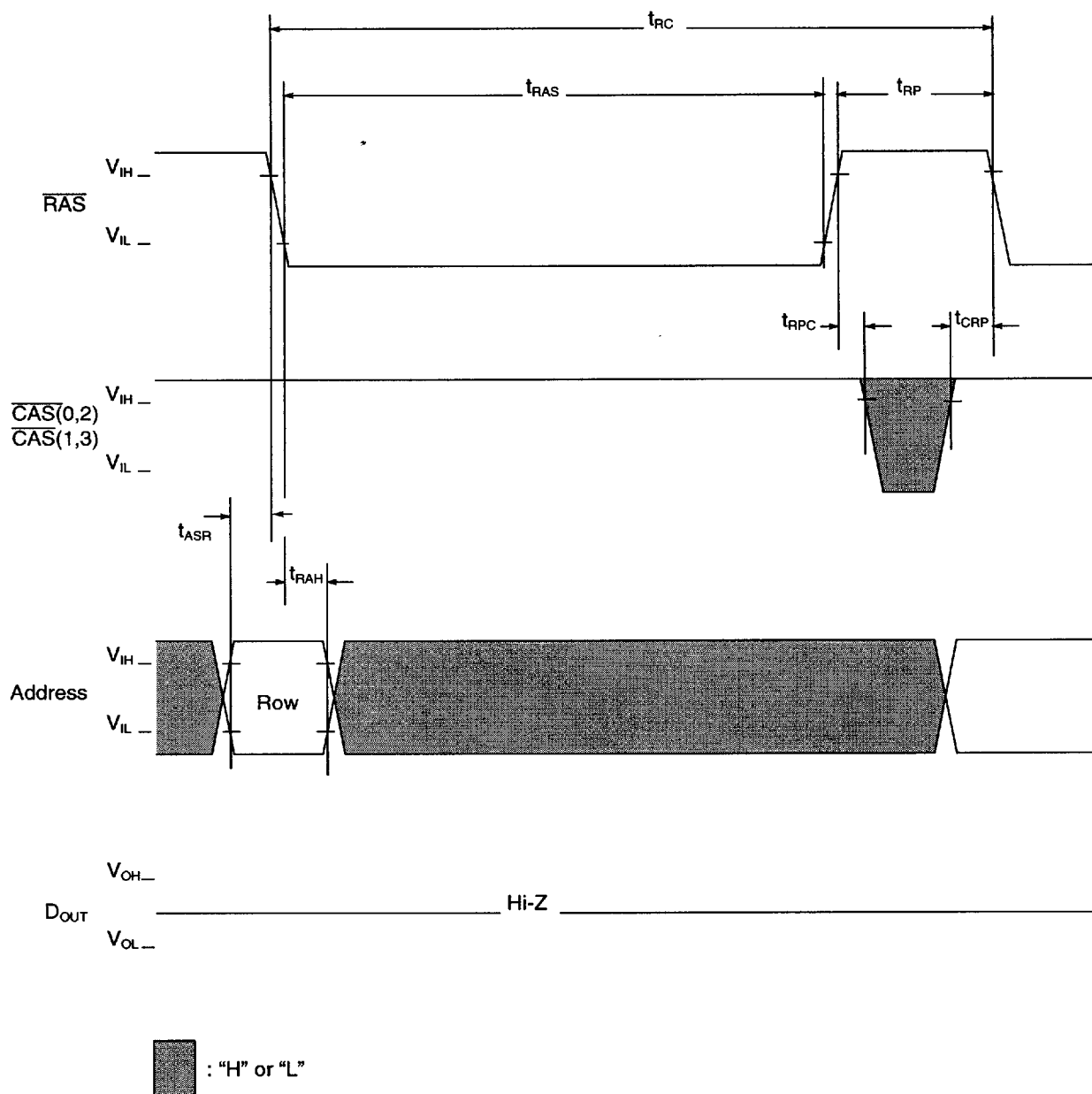
Write Cycle (Early Write)



Fast Page Mode Write Cycle

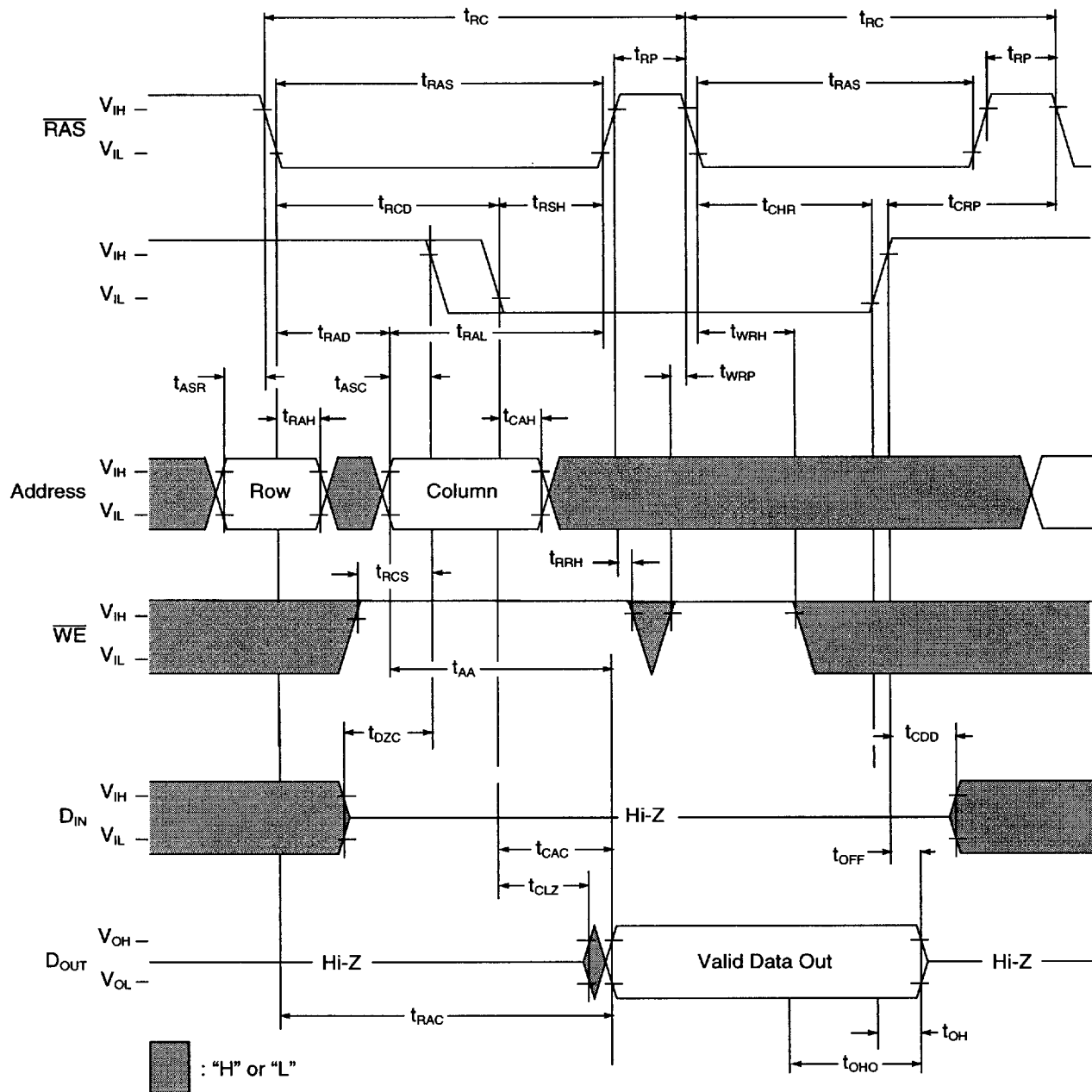


$\overline{\text{RAS}}$ Only Refresh Cycle

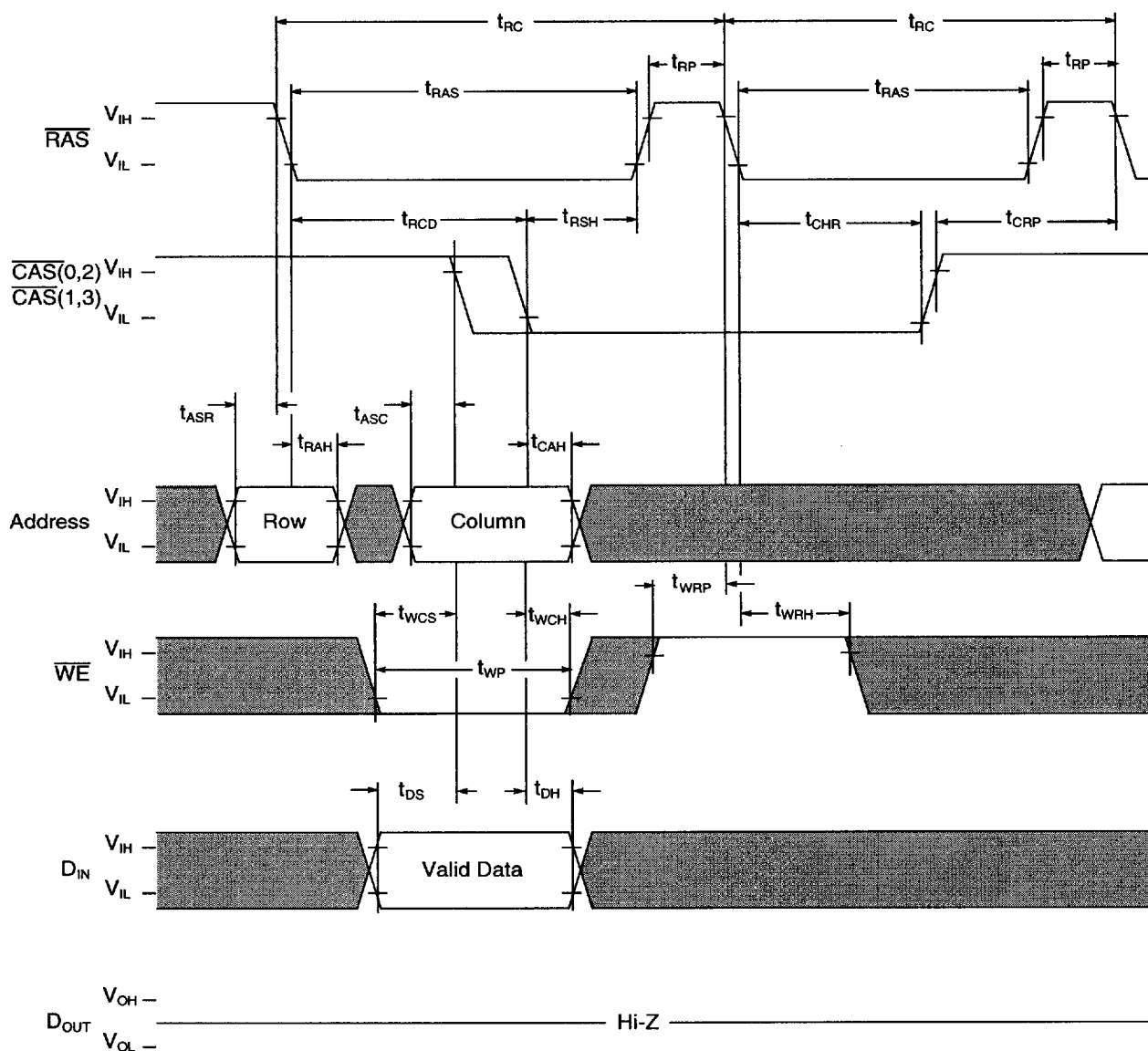


Note: $\overline{\text{WE}}$, D_{IN} are "H" or "L"

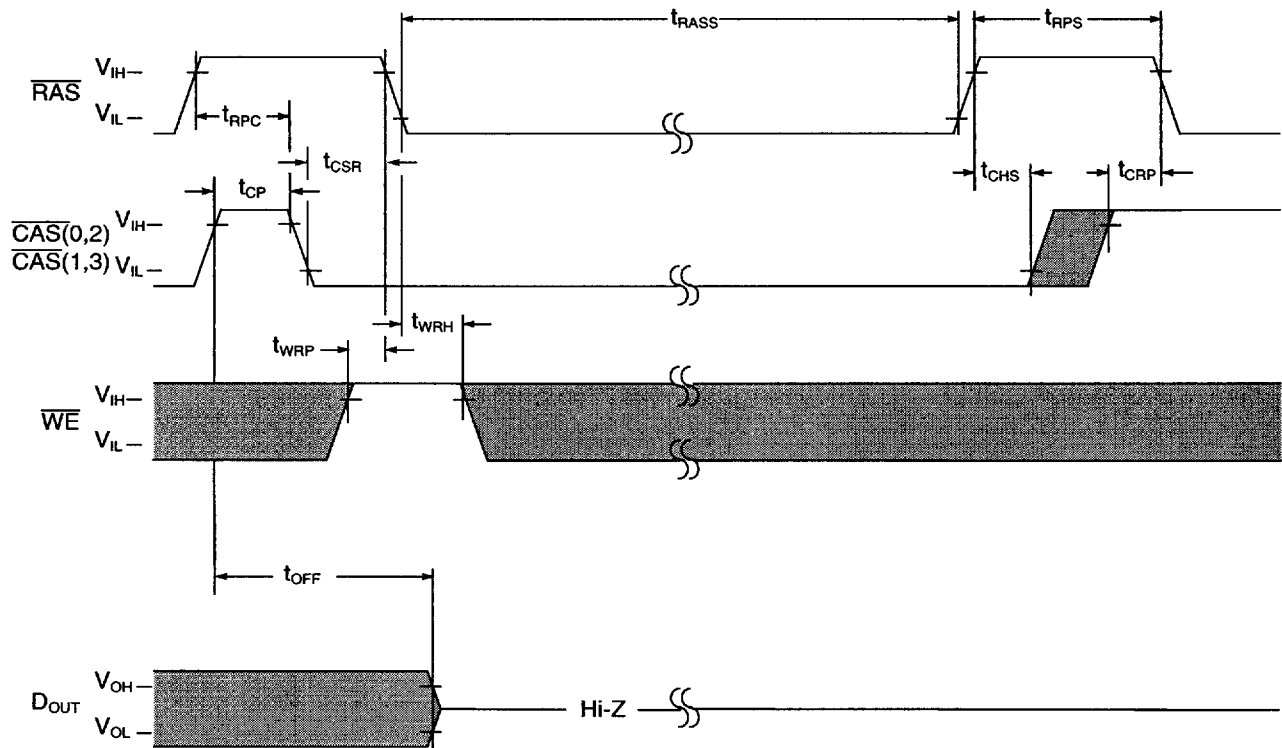
Hidden Refresh Cycle (Read)



Hidden Refresh Cycle (Write)



Self Refresh Cycle (Sleep Mode)

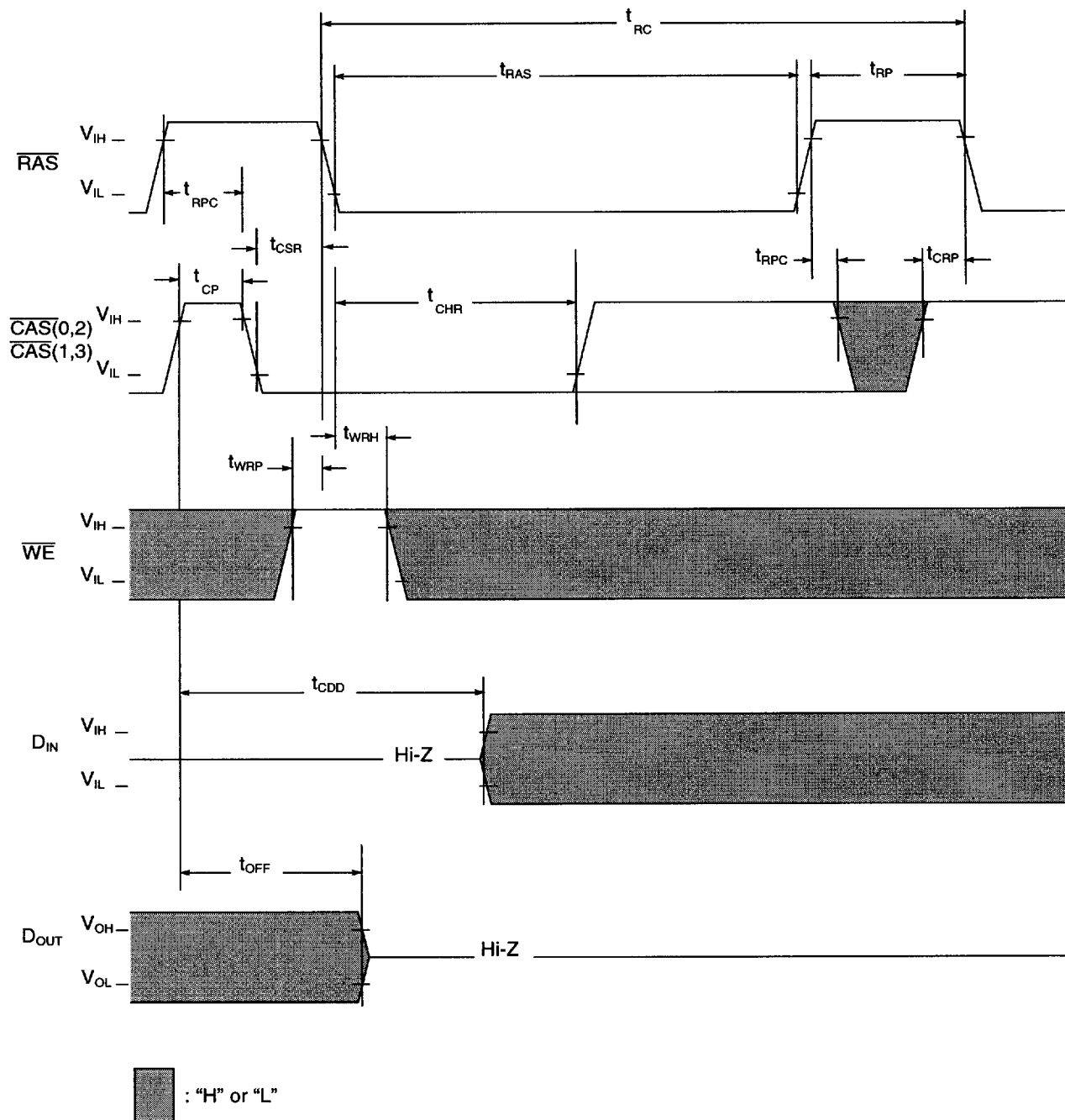


■ : "H" or "L"

NOTE: Address and OE are "H" or "L"

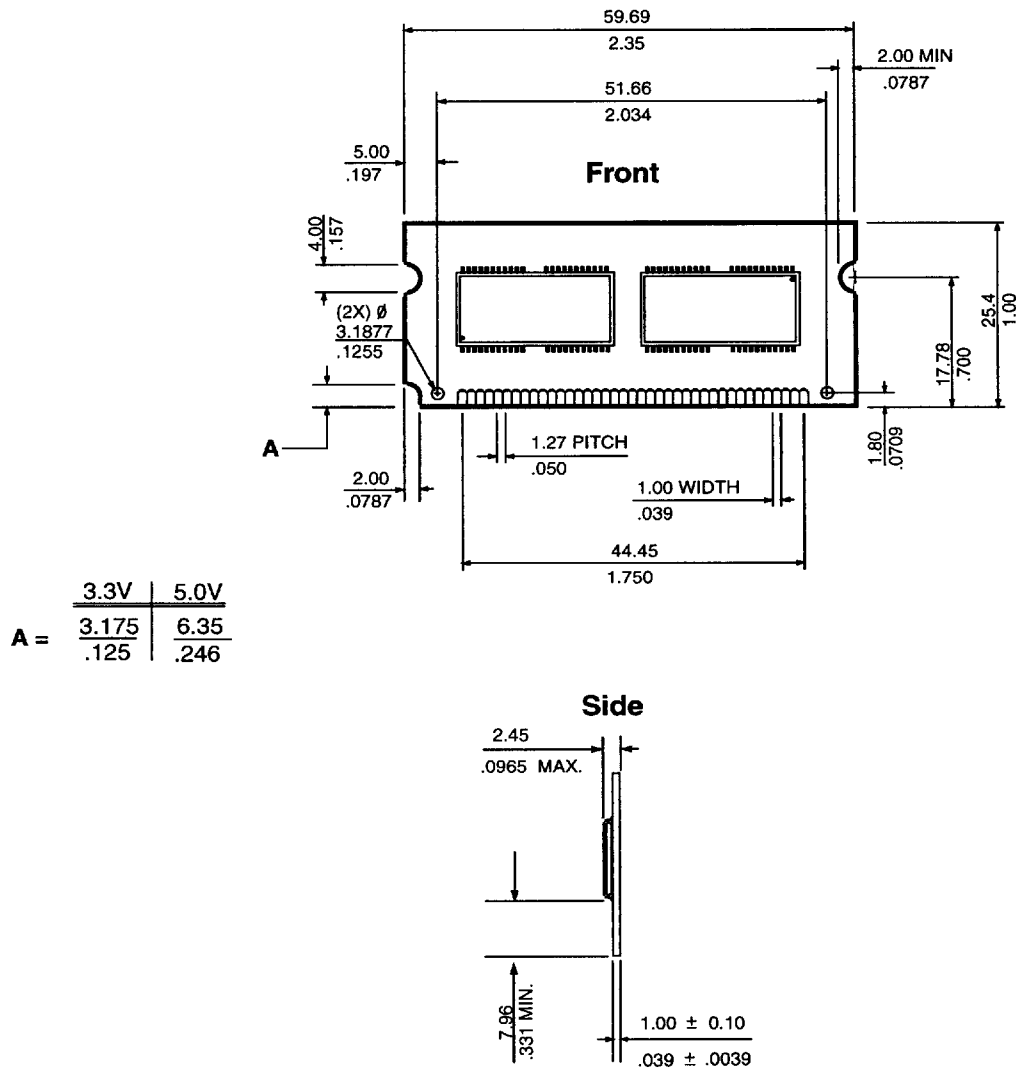
Once t_{RAS} (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

CAS Before RAS Refresh Cycle



Note: Addresses are "H" or "L"

Layout Drawing



Note: All dimensions are typical unless otherwise stated.

Millimeters
Inches

27H5212
SA14-4464-01
Revised 7/95

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Revision Log

Rev	Contents of Modification
12/94	Initial release of 1Mx32 specification using 1Mx16 10/10 Addressing
7/95	Update specification with DRAM Die Rev "D" information; Changed t_{RPC} , t_{RAS} , t_{CAS} , t_{RAD} , t_{OFF} ; Added Hidden Refresh and Self Refresh; Changed currents I_{CC1} , I_{CC3} , I_{CC4} , I_{CC6} ; Added Undershoot/Overshoot note to Recommended DC Operating Condition Table. Changed $\overline{UCAS}$ and $\overline{LCAS}$ to $\overline{CAS}$ 0,2 and $\overline{CAS}$ 1,3 respectively