# 2M x 32 SODIMM Module

## Features

- 72-Pin Small Outline Dual-In-Line Memory Module
- Performance:

| | | -60 | -70 |
|---|---|---|---|
| $t_{RAC}$ | $\overline{RAS}$ Access Time | 60ns | 70ns |
| $t_{CAC}$ | $\overline{CAS}$ Access Time | 15ns | 20ns |
| $t_{AA}$ | Access Time From Address | 30ns | 35ns |
| $t_{RC}$ | Cycle Time | 104ns | 124ns |
| $t_{HPC}$ | EDO Mode Cycle Time | 25ns | 30ns |

- High Performance CMOS process
- Manufactured with 16Mb DRAMS (1M x 16)
- Single 3.3V ± 0.3V or 5.0V ± 0.5V Power Supply
- Optimized for use in byte-write non-parity applications.
- Low active current consumption
- All inputs & outputs are LVTTL(3.3V) or TTL(5V) compatible
- Extended Data Out (EDO) access cycle
- Refresh Modes: $\overline{RAS}$-Only, CBR, Hidden Refresh and Self Refresh
- 1024 refresh cycles distributed across 128ms
- 10/10 Addressing (Row/Column)
- Au contacts

## Description

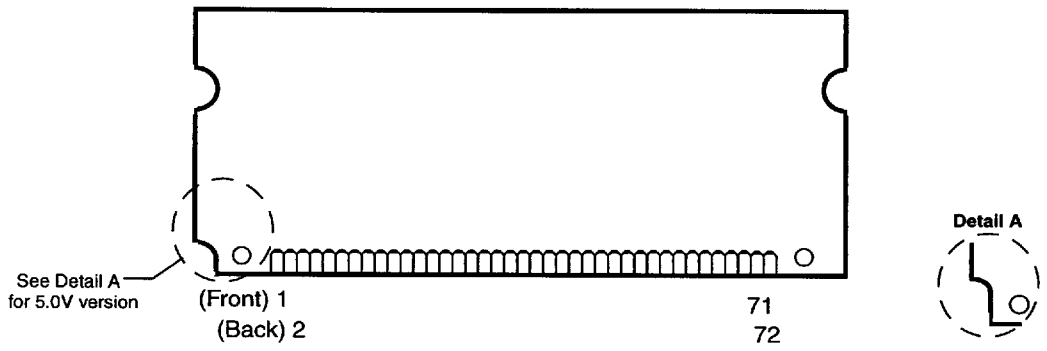
The IBM11S2325LP/M are 8MB industry standard 72-pin 4-byte small outline dual in-line memory modules (SODIMMs). The module is organized as a 2Mx32 high speed memory array that is intended for use in 16, 32 and 64 bit applications. It is manufactured with four 1Mx16 TSOP devices, each in a 400mil package.

The use of EDO DRAMs allows for a reduction in Page Mode cycletime from 40ns (Fast Page) to 25ns (EDO, 60ns sort). The use of TSOP packages allows tight DIMM spacing (.3" on center). Input loading is consistent with 8Mb-based assemblies due to the addition of discrete capacitors maximizing compatibility at the system-level.

This assembly is intended for use in space constrained and/or low power applications.

The IBM 72-Pin SODIMMs provide a high performance, flexible 4-byte interface in a 2.35" long footprint.

## Card Outline 3.3V




50H4743
SA14-4556-00
Released 8/95

## Pin Description

| | |
|---|---|
| $\overline{RAS0}$ - $\overline{RAS3}$ | Row Address Strobe |
| $\overline{CAS0}$ - $\overline{CAS3}$ | Column Address Strobe |
| $\overline{WE}$ | Read/write Input |
| A0 - A9 | Address Inputs |
| DQ0-7, 9-16, 18-25, 27-34 | Data Input/output |
| $V_{CC}$ | Power (+3.3V or +5.0V) |
| $V_{SS}$ | Ground |
| NC | No Connect |
| PD1 - PD7 | Presence Detects |

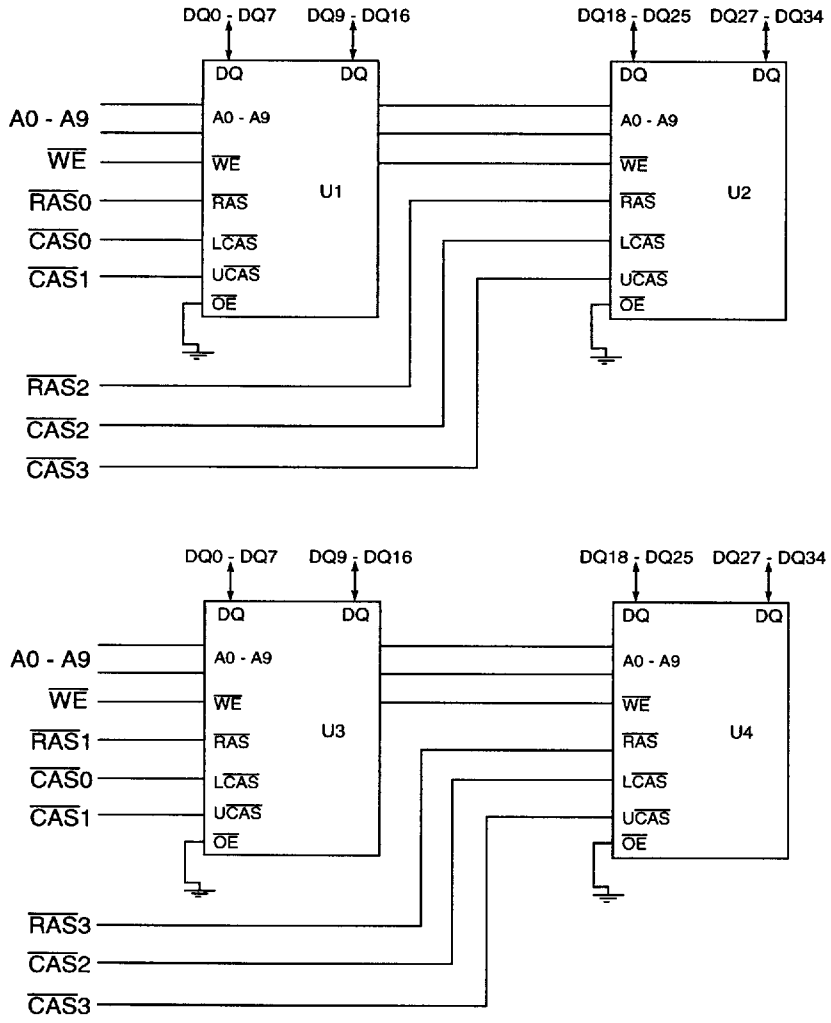
## Pinout

| Pin# | Name | Pin# | Name | Pin# | Name | Pin# | Name | Pin# | Name | Pin# | Name |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 13 | A1 | 25 | DQ13 | 37 | DQ18 | 49 | DQ20 | 61 | $V_{CC}$ |
| 2 | DQ0 | 14 | A2 | 26 | DQ14 | 38 | DQ19 | 50 | DQ21 | 62 | DQ32 |
| 3 | DQ1 | 15 | A3 | 27 | DQ15 | 39 | $V_{SS}$ | 51 | DQ22 | 63 | DQ33 |
| 4 | DQ2 | 16 | A4 | 28 | A7 | 40 | $\overline{CAS0}$ | 52 | DQ23 | 64 | DQ34 |
| 5 | DQ3 | 17 | A5 | 29 | NC | 41 | $\overline{CAS2}$ | 53 | DQ24 | 65 | NC |
| 6 | DQ4 | 18 | A6 | 30 | $V_{CC}$ | 42 | $\overline{CAS3}$ | 54 | DQ25 | 66 | PD2 |
| 7 | DQ5 | 19 | NC | 31 | A8 | 43 | $\overline{CAS1}$ | 55 | NC | 67 | PD3 |
| 8 | DQ6 | 20 | NC | 32 | A9 | 44 | $\overline{RAS0}$ | 56 | DQ27 | 68 | PD4 |
| 9 | DQ7 | 21 | DQ9 | 33 | $\overline{RAS3}$ | 45 | $\overline{RAS1}$ | 57 | DQ28 | 69 | PD5 |
| 10 | $V_{CC}$ | 22 | DQ10 | 34 | $\overline{RAS2}$ | 46 | NC | 58 | DQ29 | 70 | PD6 |
| 11 | PD1 | 23 | DQ11 | 35 | DQ16 | 47 | $\overline{WE}$ | 59 | DQ31 | 71 | PD7 |
| 12 | A0 | 24 | DQ12 | 36 | NC | 48 | NC | 60 | DQ30 | 72 | $V_{SS}$ |

## Ordering Information

| Part Number | Organization | Speed | Dimensions | Power | DRAM Die Revision | Notes |
|---|---|---|---|---|---|---|
| IBM11S2325LPB-60 | 2M x 32 | 60ns | 2.35" x 1" x .1496" | 3.3V | D | |
| IBM11S2325LPB-70 | 2M x 32 | 70ns | 2.35" x 1" x .1496" | 3.3V | D | |
| IBM11S2325LMB-60 | 2M x 32 | 60ns | 2.35" x 1" x .1496" | 5.0V | D | |
| IBM11S2325LMB-70 | 2M x 32 | 70ns | 2.35" x 1" x .1496" | 5.0V | D | |

## Block Diagram



## Truth Table

| Function | | $\overline{RAS}$ | $\overline{CAS}$ | $\overline{WE}$ | Row Address | Column Address | All DQ bits |
|---|---|---|---|---|---|---|---|
| Standby | | H | X | X | X | X | High Impedance |
| Read | | L | L | H | Row | Col | Valid Data Out |
| Early-Write | | L | L | L | Row | Col | Valid Data In |
| EDO Mode - Read: 1st Cycle | | L | H→L | H | Row | Col | Valid Data Out |
| Subsequent Cycles | | L | H→L | H | N/A | Col | Valid Data Out |
| EDO Mode - Write: 1st Cycle | | L | H→L | L | Row | Col | Valid Data In |
| Subsequent Cycles | | L | H→L | L | N/A | Col | Valid Data In |
| $\overline{RAS}$-Only Refresh | | L | H | X | Row | N/A | High Impedance |
| $\overline{CAS}$-Before-$\overline{RAS}$ Refresh | | H→L | L | H | X | X | High Impedance |
| Hidden Refresh | Read | L→H→L | L | H | Row | Col | Data Out |
| | Write | L→H→L | L | L | Row | Col | Data In |
| Self Refresh | | H→L | L | H | X | X | High Impedance |

## Presence Detect

| Pin | -60 | -70 |
|---|---|---|
| PD1 | NC | NC |
| PD2 | $V_{SS}$ | $V_{SS}$ |
| PD3 | $V_{SS}$ | $V_{SS}$ |
| PD4 | NC | NC |
| PD5 | NC | $V_{SS}$ |
| PD6 | NC | NC |
| PD7 | $V_{SS}$ | $V_{SS}$ |

1. NC= OPEN, $V_{SS}$ = GND

## Absolute Maximum Ratings

| Symbol | Parameter | Rating | | Units | Notes |
|---|---|---|---|---|---|
| | | 3.3 Volt | 5.0 Volt | | |
| $V_{CC}$ | Power Supply Voltage | -0.5 to + 4.6 | -1.0 to + 7.0 | V | 1 |
| $V_{IN}$ | Input Voltage | -0.5 to min ($V_{CC}$ + 0.5, 4.6) | -0.5 to min ($V_{CC}$ + 0.5, 7.0) | V | 1 |
| $V_{OUT}$ | Output Voltage | -0.5 to min ($V_{CC}$ + 0.5, 4.6) | -0.5 to min ($V_{CC}$ + 0.5, 7.0) | V | 1 |
| $T_{OPR}$ | Operating Temperature | 0 to +70 | 0 to +70 | °C | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +150 | -55 to +150 | °C | 1 |
| $P_D$ | Power Dissipation | 3.0 | 4.3 | W | 1 |
| $I_{OUT}$ | Short Circuit Output Current | 50 | 50 | mA | 1 |

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Recommended DC Operating Conditions ($T_A$ = 0 to 70°C)

| Symbol | Parameter | 3.3 Volt | | | 5.0 Volt | | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | Min | Typ | Max | Min | Typ | Max | | |
| $V_{CC}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | 4.5 | 5.0 | 5.5 | V | 1 |
| $V_{IH}$ | Input High Voltage | 2.0 | — | $V_{CC}$ + 0.5 | 2.4 | — | $V_{CC}$ + 0.5 | V | 1, 2 |
| $V_{IL}$ | Input Low Voltage | -0.5 | — | 0.8 | -0.5 | — | 0.8 | V | 1, 2 |

1. All voltages referenced to $V_{SS}$.
2. $V_{IH}$ may overshoot to $V_{CC}$ + 1.2V for pulse widths of ≤ 4.0ns with 3.3 Volt, or $V_{CC}$ + 2.0V for pulse widths of ≤ 4.0ns (or $V_{CC}$ + 1.0V for ≤ 8.0ns) with 5.0 Volt. Additionally, $V_{IL}$ may undershoot to -2.0V for pulse widths ≤ 4.0ns (or -1.0V for ≤ 8.0ns). Pulse widths measured at 50% points with amplitude measured peak to DC reference.

## Capacitance ($T_A$ = 0 to +70°C, $V_{CC}$ = 3.3V ± 0.3V or 5.0V ± 0.5V)

| Symbol | Parameter | Max | Units | Notes |
|---|---|---|---|---|
| $C_{I1}$ | Input Capacitance (A0-A9) | 38 | pF | |
| $C_{I2}$ | Input Capacitance ($\overline{RAS}$0) | 16 | pF | |
| $C_{I3}$ | Input Capacitance ($\overline{RAS}$2) | 16 | pF | |
| $C_{I4}$ | Input Capacitance ($\overline{CAS}$) | 22 | pF | |
| $C_{I5}$ | Input Capacitance ($\overline{WE}$) | 42 | pF | |
| $C_{I/O}$ | Output Capacitance (DQ0-DQ34) | 23 | pF | |

## DC Electrical Characteristics ($T_A$ = 0 to +70°C, $V_{CC}$ = 3.3 0.3V or 5.0 0.5V)

| Symbol | Parameter | | 3.3 Volt Min | 3.3 Volt Max | 5.0 Volt Min | 5.0 Volt Max | Units | Notes |
|---|---|---|---|---|---|---|---|---|
| $I_{CC1}$ | Operating Current<br>Average Power Supply Operating Current<br>($\overline{RAS}$, $\overline{CAS}$, Address Cycling: $t_{RC}$ = $t_{RC}$ min) | -60 | — | 410 | — | 370 | mA | 1, 2, 3 |
| | | -70 | — | 390 | — | 350 | | |
| $I_{CC2}$ | Standby Current (TTL)<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ ≥$V_{IH}$) | | — | 8 | — | 8 | mA | |
| $I_{CC3}$ | $\overline{RAS}$ Only Refresh Current<br>Average Power Supply Current, $\overline{RAS}$ Only Mode<br>($\overline{RAS}$ Cycling, $\overline{CAS}$ ≥$V_{IH}$: $t_{RC}$ = $t_{RC}$ min) | -60 | — | 410 | — | 370 | mA | 1, 3 |
| | | -70 | — | 390 | — | 350 | | |
| $I_{CC4}$ | EDO Mode Current<br>Average Power Supply Current, EDO Mode<br>($\overline{RAS}$ = $V_{IL}$, $\overline{CAS}$, Address Cycling: $t_{HPC}$ = $t_{HPC}$ min) | -60 | — | 180 | — | 180 | mA | 1, 2, 3 |
| | | -70 | — | 160 | — | 160 | | |
| $I_{CC5}$ | Standby Current (CMOS)<br>Power Supply Standby Current<br>($\overline{RAS}$ = $\overline{CAS}$ = $V_{CC}$ - 0.2V) | | — | 2 | — | 2 | mA | |
| $I_{CC6}$ | $\overline{CAS}$ Before $\overline{RAS}$ Refresh Current<br>Average Power Supply Current, $\overline{CAS}$ Before $\overline{RAS}$ Mode<br>($\overline{RAS}$, $\overline{CAS}$, Cycling: $t_{RC}$ = $t_{RC}$ min) | -60 | — | 410 | — | 370 | mA | 1, 3 |
| | | -70 | — | 390 | — | 350 | | |
| $I_{CC7}$ | Self Refresh Current<br>Average Power Supply Current during Self Refresh<br>CBR cycle with $\overline{RAS}$ ≥ $t_{RASS}$ (min); $\overline{CAS}$ held low;<br>$\overline{WE}$ = $V_{CC}$ - 0.2V; Addresses and $D_{IN}$ = $V_{CC}$ - 0.2V or 0.2V. | -60 | — | 400 | — | 600 | µA | |
| | | -70 | — | 400 | — | 600 | | |
| $I_{I(L)}$ | Input Leakage Current<br>Input Leakage Current, any input<br>(0.0 ≤ $V_{IN}$ ≤ ($V_{CC}$ + 0.3v))<br>All Other Pins Not Under Test = 0V | $\overline{RAS}$ | -10 | +10 | -10 | +10 | µA | |
| | | $\overline{CAS}$ | -20 | +20 | -20 | +20 | | |
| | | All others | -40 | +40 | -40 | +40 | | |
| $I_{O(L)}$ | Output Leakage Current<br>($D_{OUT}$ is disabled, 0.0 ≤ $V_{OUT}$ ≤ $V_{CC}$) | | -10 | +10 | -10 | +10 | µA | |
| $V_{OH}$ | Output High Level<br>Output "H" Level Voltage ($I_{OUT}$ = -2.5mA for 3.3V, or $I_{OUT}$ = -5mA for 5.0V) | | 2.4 | — | 2.4 | — | V | |
| $V_{OL}$ | Output Low Level<br>Output "L" Level Voltage ($I_{OUT}$ = +2.1mA for 3.3V, or $I_{OUT}$ = +4.2mA for 5.0V) | | — | 0.4 | — | 0.4 | V | |

1. $I_{CC1}$, $I_{CC3}$, $I_{CC4}$ and $I_{CC6}$ depend on cycle rate.
2. $I_{CC1}$, $I_{CC4}$ depend on output loading. Specified values are obtained with the output open.
3. Address can be changed once or less while $\overline{RAS}$ = $V_{IL}$. In the case of $I_{CC4}$, it can be changed once or less when $\overline{CAS}$ = $V_{IH}$.

## AC Characteristics ($T_A$ = 0 to +70°C, $V_{CC}$ = 3.3V 0.3V or 5.0V 0.5V)

1. An initial pause of 200µs is required after power-up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using the internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles is required.
2. AC measurements assume $t_T$=2ns.
3. $V_{IH}$(min.) and $V_{IL}$(max.) are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}$ and $V_{IL}$.
4. When both $\overline{CAS0}$ & $\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ go low at the same time, all 16 bits of data are read/written into the device. $\overline{CAS0}$ & $\overline{CAS1}$ or $\overline{CAS2}$ & $\overline{CAS3}$ (CAS's to the same DRAM) cannot be staggered within the same read/write cycle.

## Read, Write, and Refresh Cycles (Common Parameters)

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{RC}$ | Random Read or Write Cycle Time | 104 | 128K | 124 | 128K | ns | |
| $t_{RP}$ | $\overline{RAS}$ Precharge Time | 40 | — | 50 | — | ns | |
| $t_{CP}$ | $\overline{CAS}$ Precharge Time | 10 | — | 10 | — | ns | |
| $t_{RAS}$ | $\overline{RAS}$ Pulse Width | 60 | 10K | 70 | 10K | ns | |
| $t_{CAS}$ | $\overline{CAS}$ Pulse Width | 10 | 10K | 12 | 10K | ns | |
| $t_{ASR}$ | Row Address Setup Time | 0 | — | 0 | — | ns | |
| $t_{RAH}$ | Row Address Hold Time | 10 | — | 10 | — | ns | |
| $t_{ASC}$ | Column Address Setup Time | 0 | — | 0 | — | ns | |
| $t_{CAH}$ | Column Address Hold Time | 10 | — | 12 | — | ns | |
| $t_{RCD}$ | $\overline{RAS}$ to $\overline{CAS}$ Delay Time | 14 | 45 | 14 | 50 | ns | 1 |
| $t_{RAD}$ | $\overline{RAS}$ to Column Address Delay Time | 12 | 30 | 12 | 35 | ns | 2 |
| $t_{RSH}$ | $\overline{RAS}$ Hold Time | 10 | — | 12 | — | ns | |
| $t_{CSH}$ | $\overline{CAS}$ Hold Time | 50 | — | 55 | — | ns | |
| $t_{CRP}$ | $\overline{CAS}$ to $\overline{RAS}$ Precharge Time | 5 | — | 5 | — | ns | |
| $t_{DZC}$ | $\overline{CAS}$ Delay Time from $D_{IN}$ | 0 | — | 0 | — | ns | |
| $t_T$ | Transition Time (Rise and Fall) | 2 | 30 | 2 | 30 | ns | |

1. Operation within the $t_{RCD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RCD}$ (max) is specified as a reference point only: if $t_{RCD}$ is greater than the specified $t_{RCD}$ (max) limit, then access time is controlled by $t_{CAC}$.
2. Operation within the $t_{RAD}$ (max) limit ensures that $t_{RAC}$ (max) can be met. $t_{RAD}$ (max) is specified as a reference point only: If $t_{RAD}$ is greater than the specified $t_{RAD}$ (max) limit, then access time is controlled by $t_{AA}$.

## Write Cycle

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{WCS}$ | Write Command Set Up Time | 0 | — | 0 | — | ns | |
| $t_{WCH}$ | Write Command Hold Time | 10 | — | 12 | — | ns | |
| $t_{WP}$ | Write Command Pulse Width | 10 | — | 12 | — | ns | |
| $t_{RWL}$ | Write Command to $\overline{RAS}$ Lead Time | 10 | — | 12 | — | ns | |
| $t_{CWL}$ | Write Command to $\overline{CAS}$ Lead Time | 10 | — | 12 | — | ns | |
| $t_{DS}$ | $D_{IN}$ Setup Time | 0 | — | 0 | — | ns | 1 |
| $t_{DH}$ | $D_{IN}$ Hold Time | 10 | — | 12 | — | ns | 1 |

1. This timing parameter is not applicable to this product, but applies to a related product in this family.

## Read Cycle

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{RAC}$ | Access Time from $\overline{RAS}$ | — | 60 | — | 70 | ns | 1, 2 |
| $t_{CAC}$ | Access Time from $\overline{CAS}$ | — | 15 | — | 20 | ns | 1, 2 |
| $t_{AA}$ | Access Time from Address | — | 30 | — | 35 | ns | 1, 2 |
| $t_{RCS}$ | Read Command Setup Time | 0 | — | 0 | — | ns | |
| $t_{RCH}$ | Read Command Hold Time to $\overline{CAS}$ | 0 | — | 0 | — | ns | 3 |
| $t_{RRH}$ | Read Command Hold Time to $\overline{RAS}$ | 0 | — | 0 | — | ns | 3 |
| $t_{RAL}$ | Column Address to $\overline{RAS}$ Lead Time | 30 | — | 35 | — | ns | |
| $t_{CLZ}$ | $\overline{CAS}$ to Output in Low-Z | 0 | — | 0 | — | ns | |
| $t_{CDD}$ | $\overline{CAS}$ to $D_{IN}$ Delay Time | 15 | — | 20 | — | ns | |
| $t_{OFF}$ | Output Buffer Turn-off Delay | — | 15 | — | 20 | ns | 4 |

1. Measured with the specified current load and 100pF.
2. Access time is determined by the latter of $t_{RAC}$, $t_{CAC}$, $t_{CPA}$, $t_{AA}$.
3. Either $t_{RCH}$ or $t_{RRH}$ must be satisfied for a read cycle.
4. $t_{OFF}$ (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

## Extended Data Out Cycle

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{HCAS}$ | $\overline{CAS}$ Pulse Width (EDO Mode) | 10 | 10K | 12 | 10K | ns | |
| $t_{HPC}$ | EDO Mode Cycle Time (Read/Write) | 25 | — | 30 | — | ns | |
| $t_{DOH}$ | Data-out Hold Time from $\overline{CAS}$ | 5 | — | 5 | — | ns | |
| $t_{WHZ}$ | Output buffer Turn-Off Delay from $\overline{WE}$ | 0 | 10 | 0 | 15 | ns | |
| $t_{WPZ}$ | $\overline{WE}$ Pulse Width to Output Disable at $\overline{CAS}$ High | 10 | — | 10 | — | ns | |
| $t_{CPRH}$ | $\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge | 35 | — | 40 | — | ns | |
| $t_{CPA}$ | Access Time from $\overline{CAS}$ Precharge | — | 35 | — | 40 | ns | 1 |
| $t_{RASP}$ | EDO Mode $\overline{RAS}$ Pulse Width | 60 | 125K | 70 | 125K | ns | |

1. Measured with the specified current load and 100pF at $V_{OL}$ = 0.8V and $V_{OH}$ = 2.0V.

## Refresh Cycle

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | | |
| $t_{CHR}$ | $\overline{CAS}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 10 | — | 10 | — | ns | |
| $t_{CSR}$ | $\overline{CAS}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 5 | — | 5 | — | ns | |
| $t_{WRP}$ | $\overline{WE}$ Setup Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 10 | — | 10 | — | ns | |
| $t_{WRH}$ | $\overline{WE}$ Hold Time ($\overline{CAS}$ before $\overline{RAS}$ Refresh Cycle) | 10 | — | 10 | — | ns | |
| $t_{RPC}$ | $\overline{RAS}$ Precharge to $\overline{CAS}$ Hold Time | 5 | — | 5 | — | ns | |
| $t_{REF}$ | Refresh Period | — | 128 | — | 128 | ms | 1 |

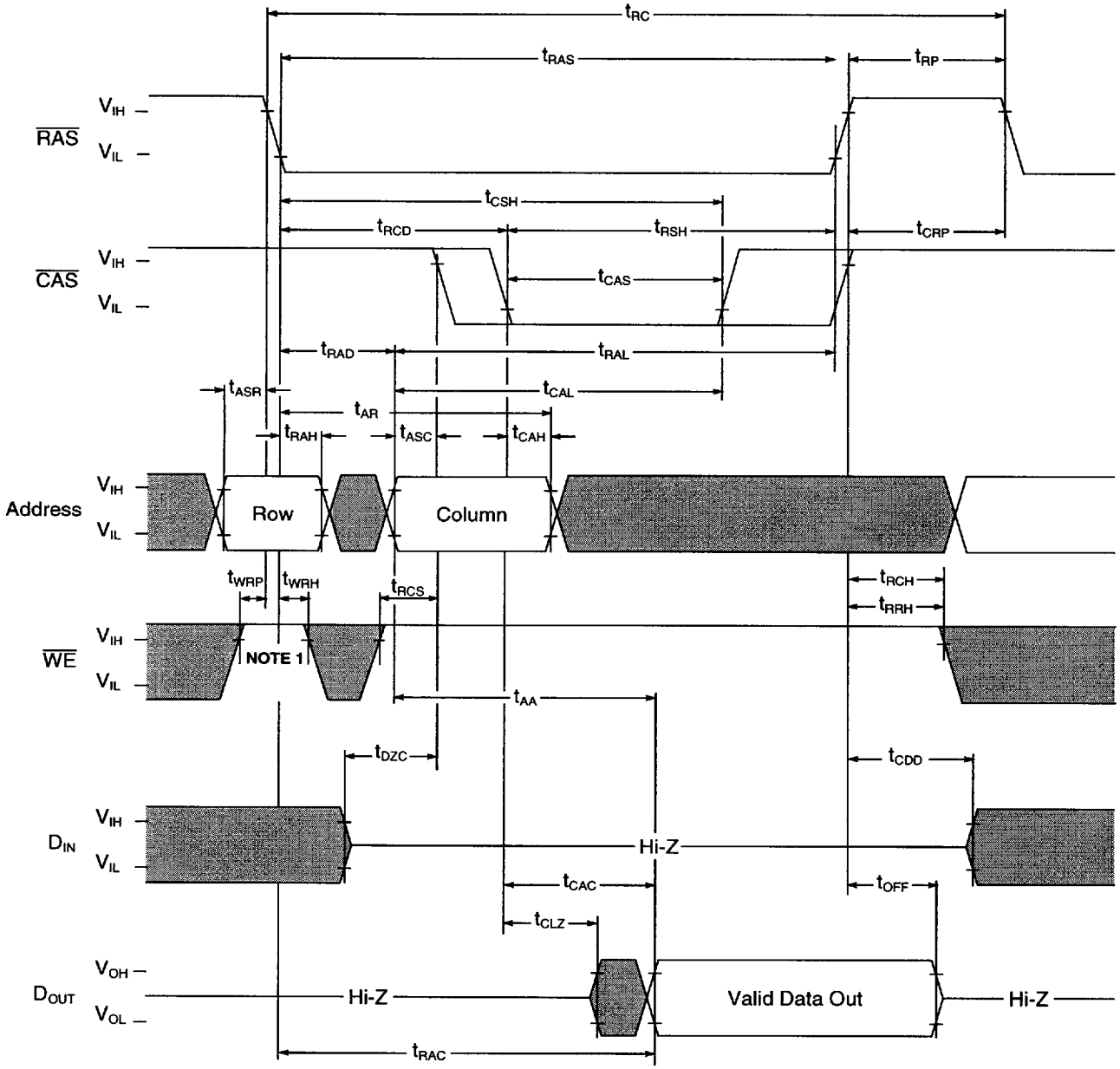
1. 1024 refreshes are required every 128ms.

## Self Refresh Cycle

| Symbol | Parameter | -60 | | -70 | | Units | Notes |
|---|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | | |
| $t_{RASS}$ | $\overline{RAS}$ Pulse Width During Self Refresh Cycle | 100 | — | 100 | — | µs | 1 |
| $t_{RPS}$ | $\overline{RAS}$ Precharge Time During Self Refresh Cycle | 104 | — | 126 | — | ns | 1 |
| $t_{CHS}$ | $\overline{CAS}$ Hold Time During Self Refresh Cycle | -50 | — | -50 | — | ns | 1 |

1. When using Self Refresh mode, the following refresh operations must be performed to ensure proper DRAM operation: If row addresses are being refreshed in a EVENLY DISTRIBUTED manner over the refresh interval using CBR refresh cycles, then only one CBR cycle must be performed immediately after exit from Self Refresh. If row addresses are being refreshed in any other manner (ROR - Distributed/Burst; or CBR-Burst) over the refresh interval, then a full set of row refreshes must be performed immediately before entry to and immediately after exit from Self Refresh.

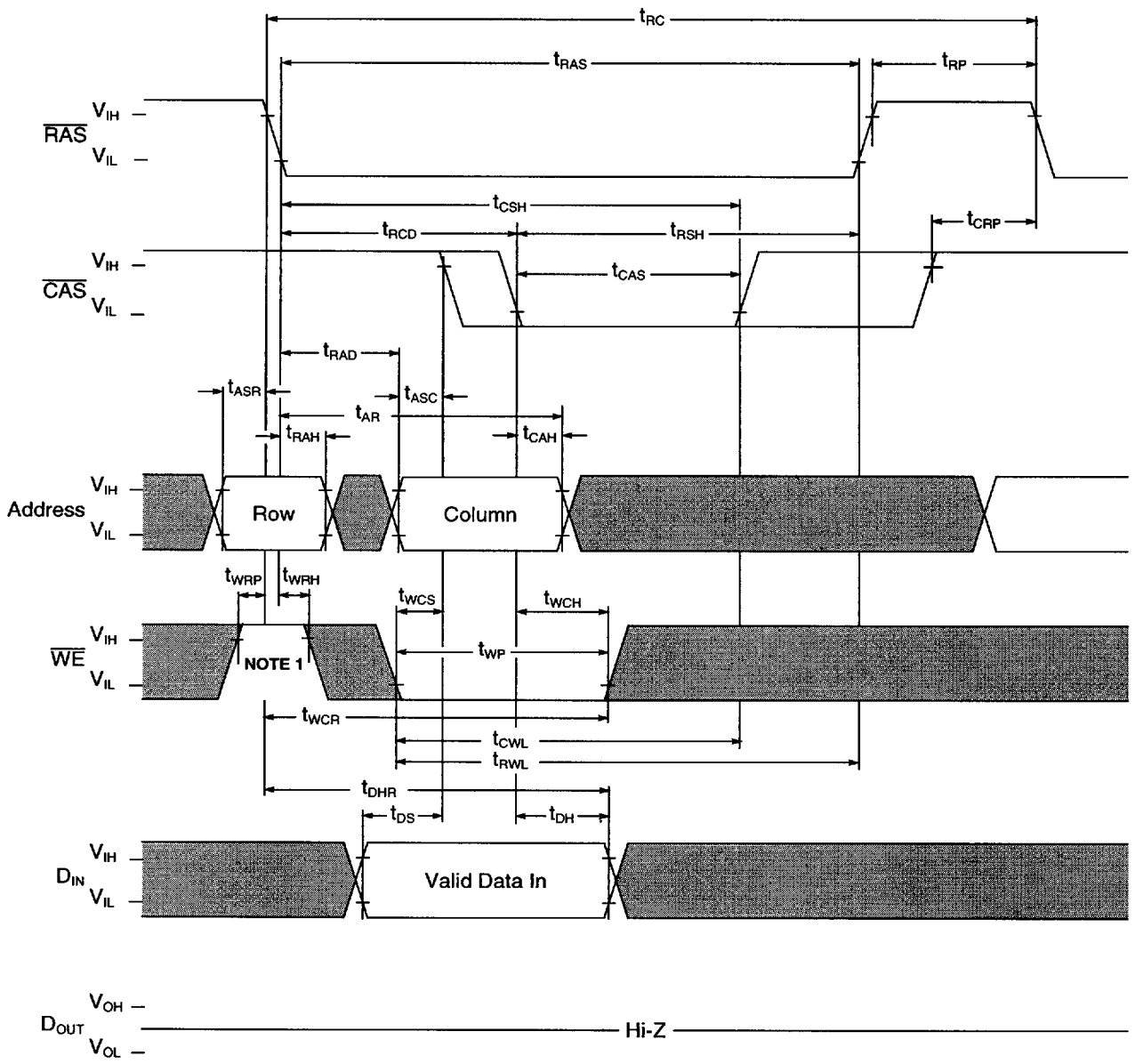
## Read




: "H" or "L"

**NOTE 1:** Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

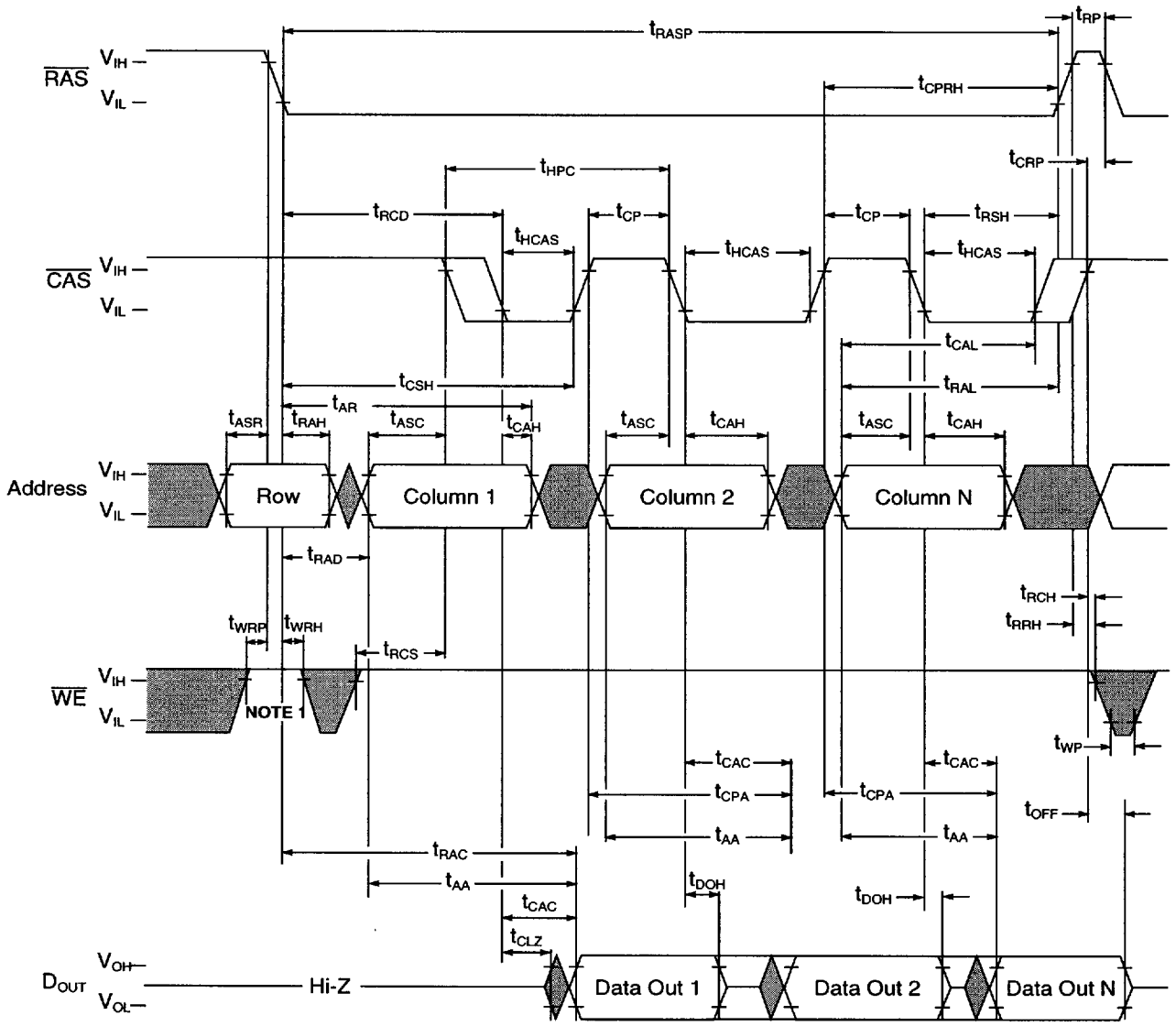
## Write Cycle (Early Write)




: "H" or "L"

**NOTE 1:** Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

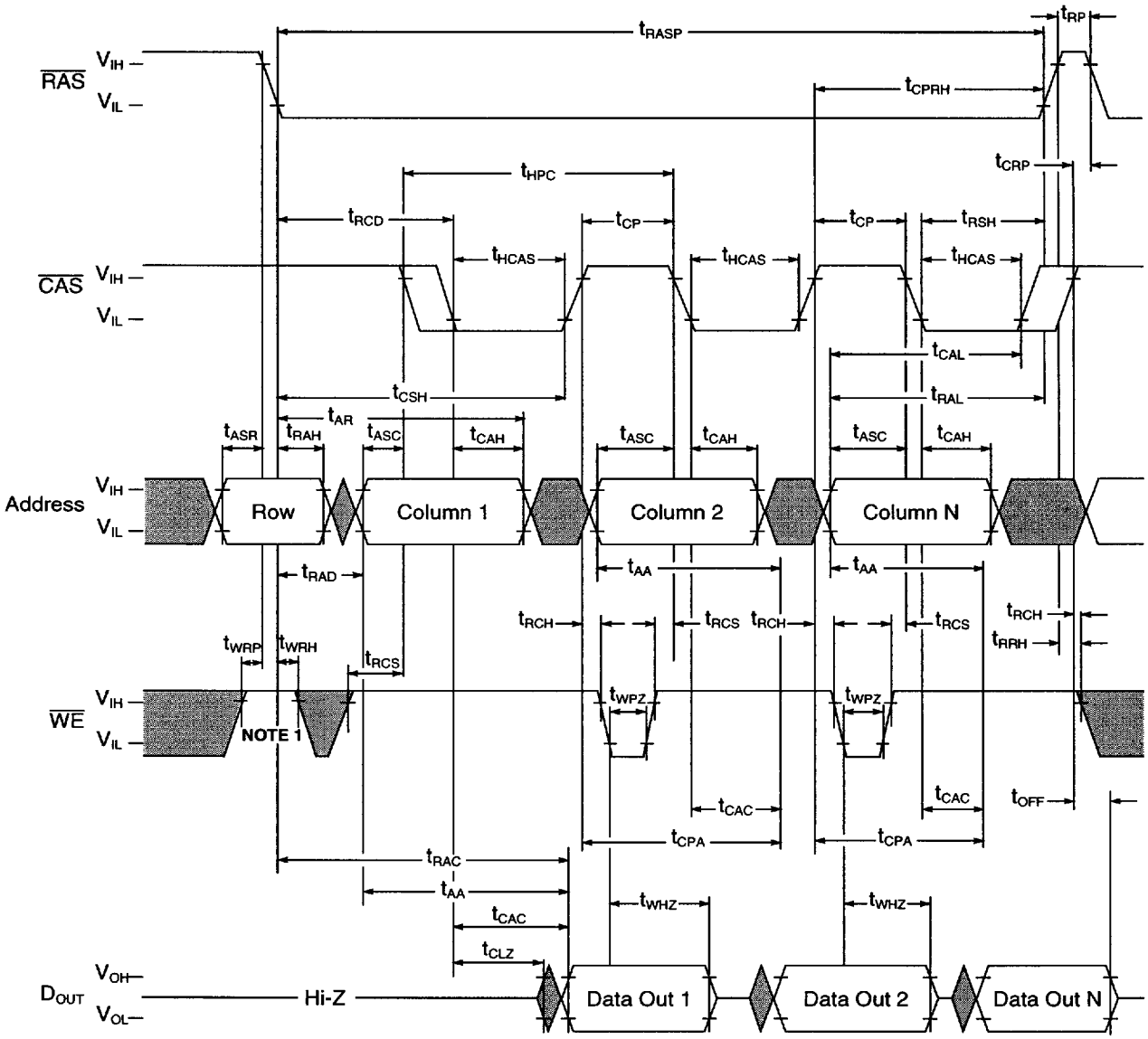
## Extended Data Out Mode Read Cycle




: "H" or "L"

**NOTE 1:** Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

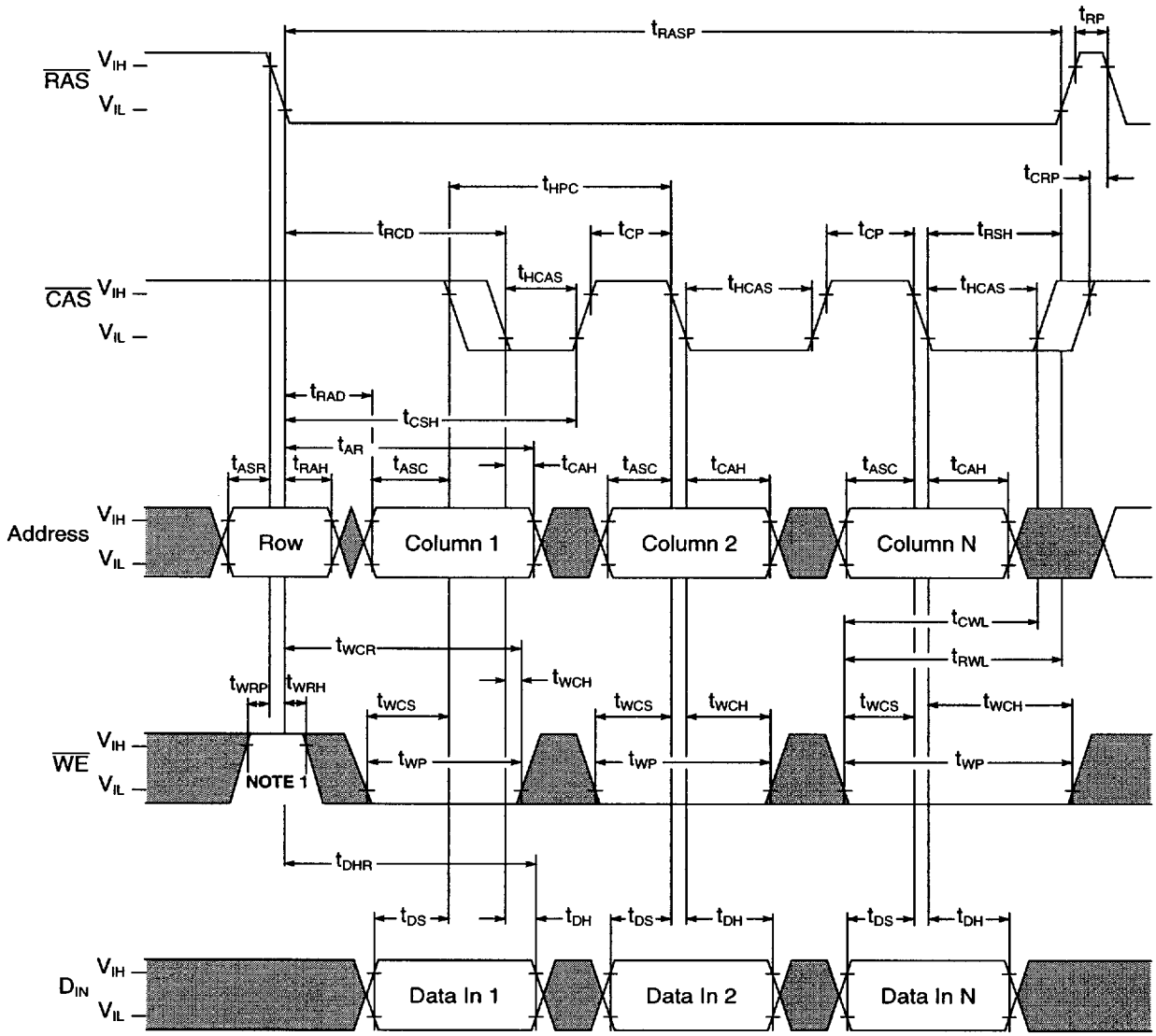
## Extended Data Out Mode Read Cycle ($\overline{WE}$ Control)




: "H" or "L"

**NOTE 1:** Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional Doing so will facilitate compatibility with future EDO DRAMs.

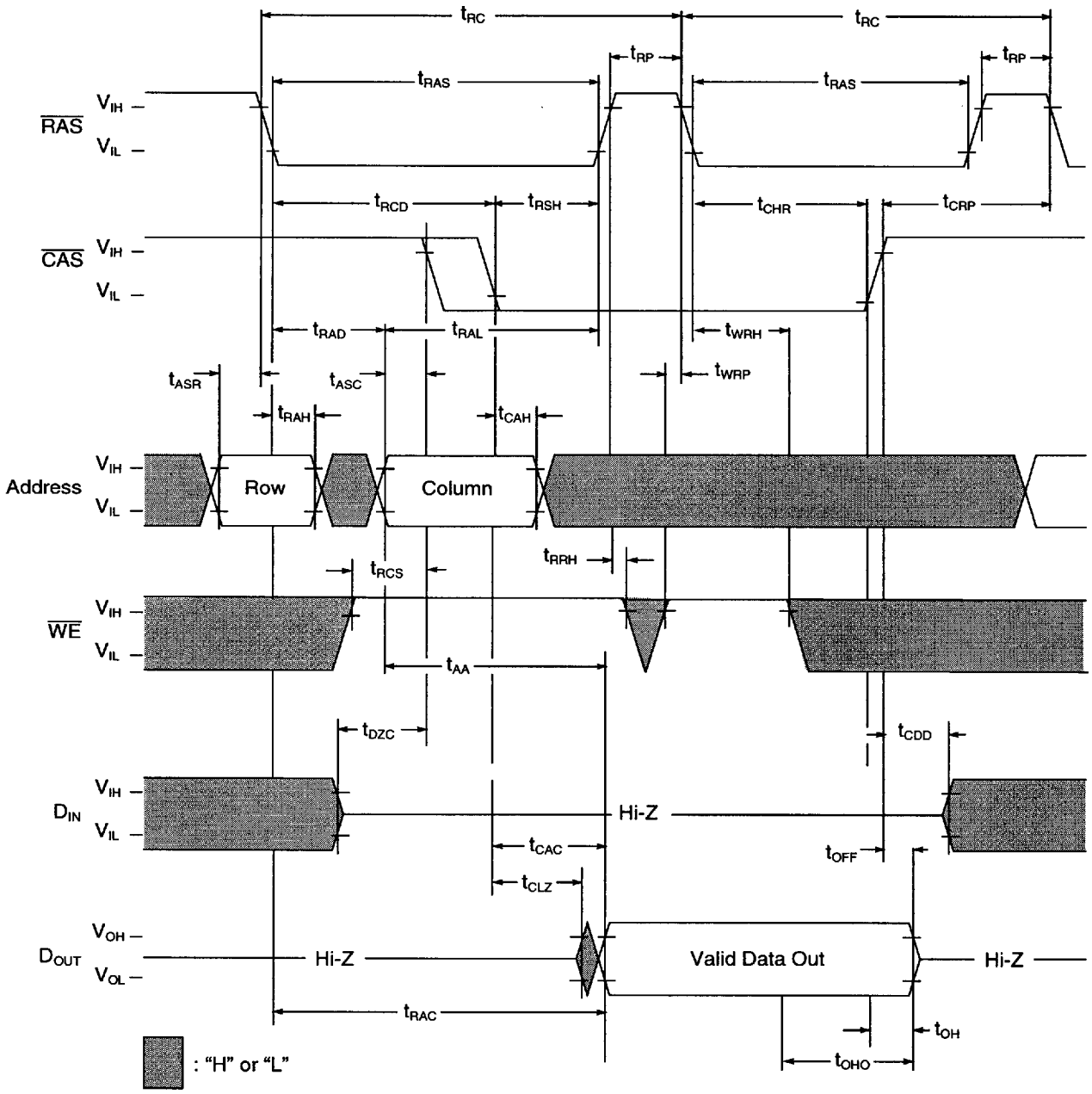
## Extended Data Out Mode Write Cycle



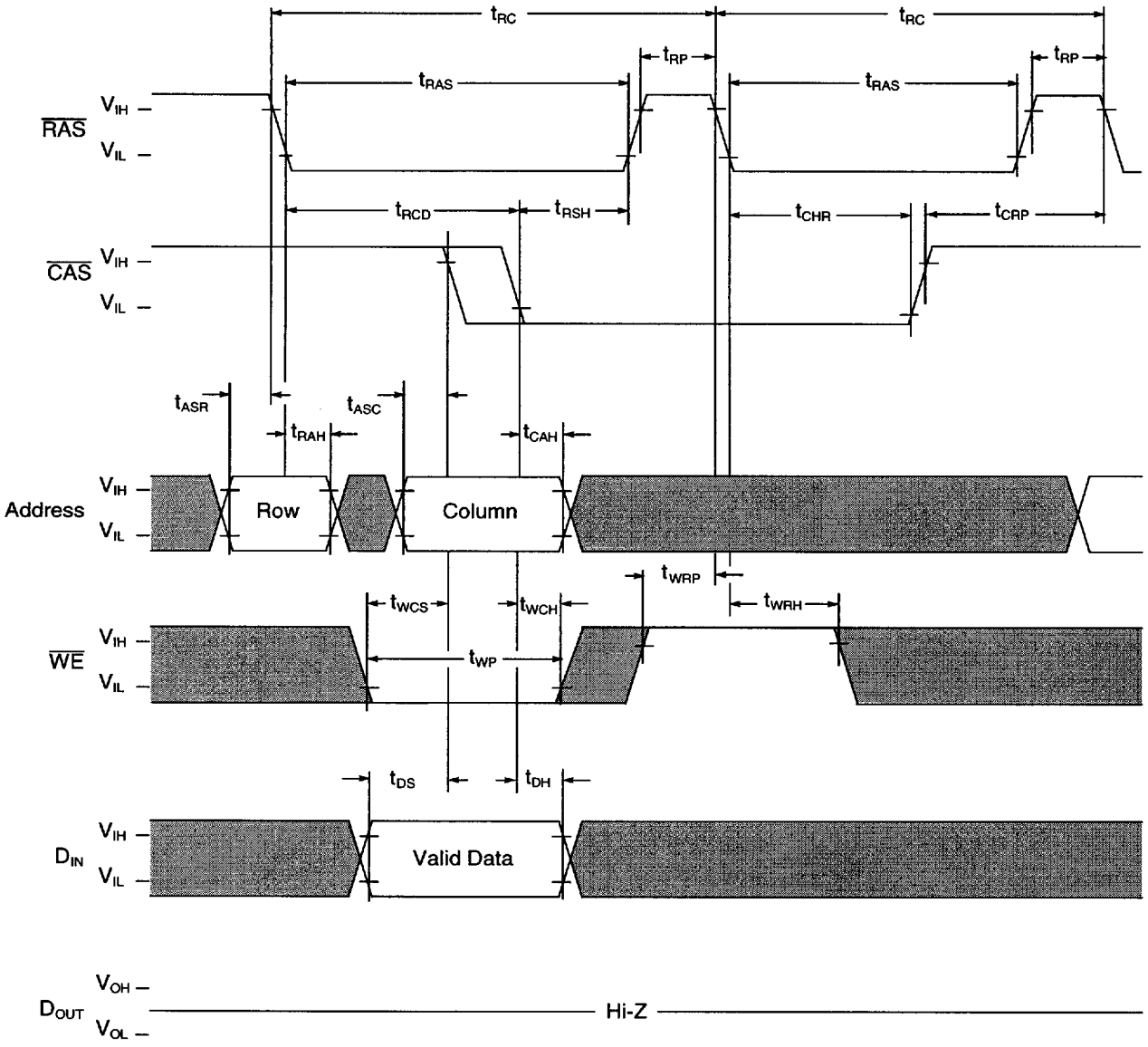

: "H" or "L"

**NOTE 1:** Implementing $\overline{WE}$ at $\overline{RAS}$ time During a Read or Write Cycle is optional. Doing so will facilitate compatibility with future EDO DRAMs.

## Hidden Refresh Cycle (Read)

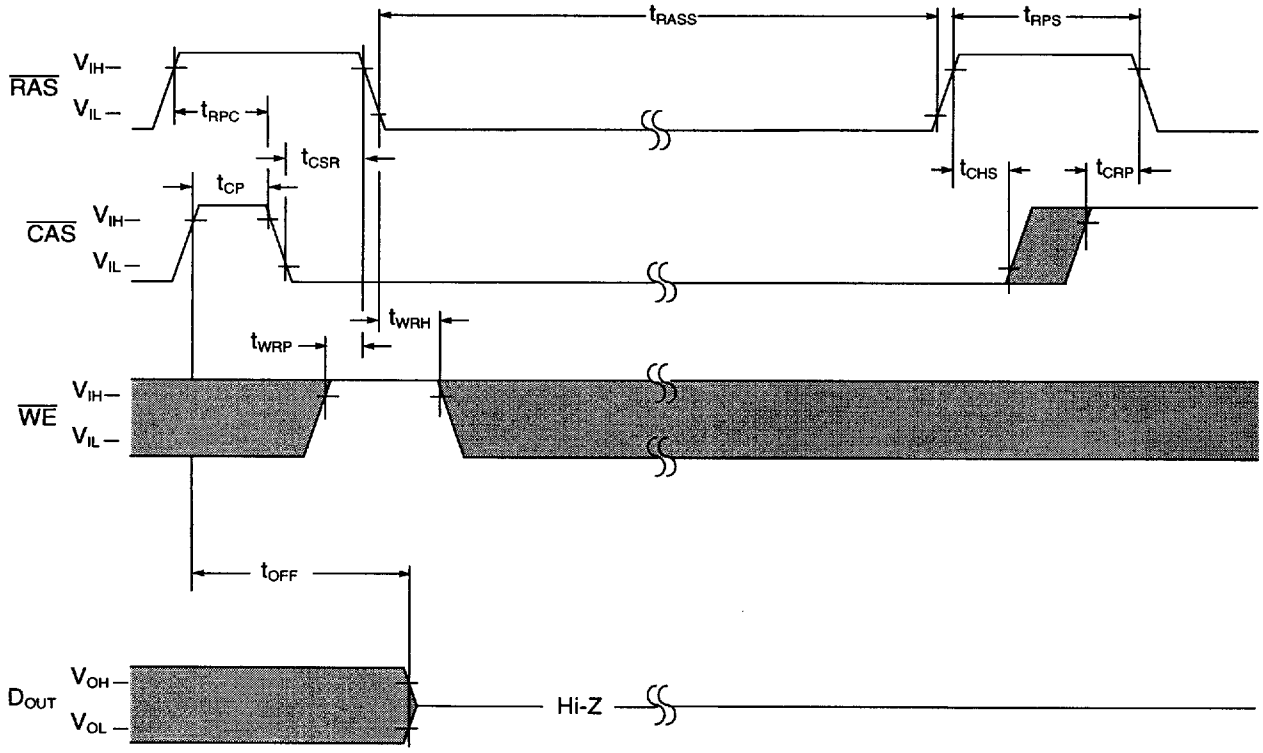


## Hidden Refresh Cycle (Write)




: "H" or "L"

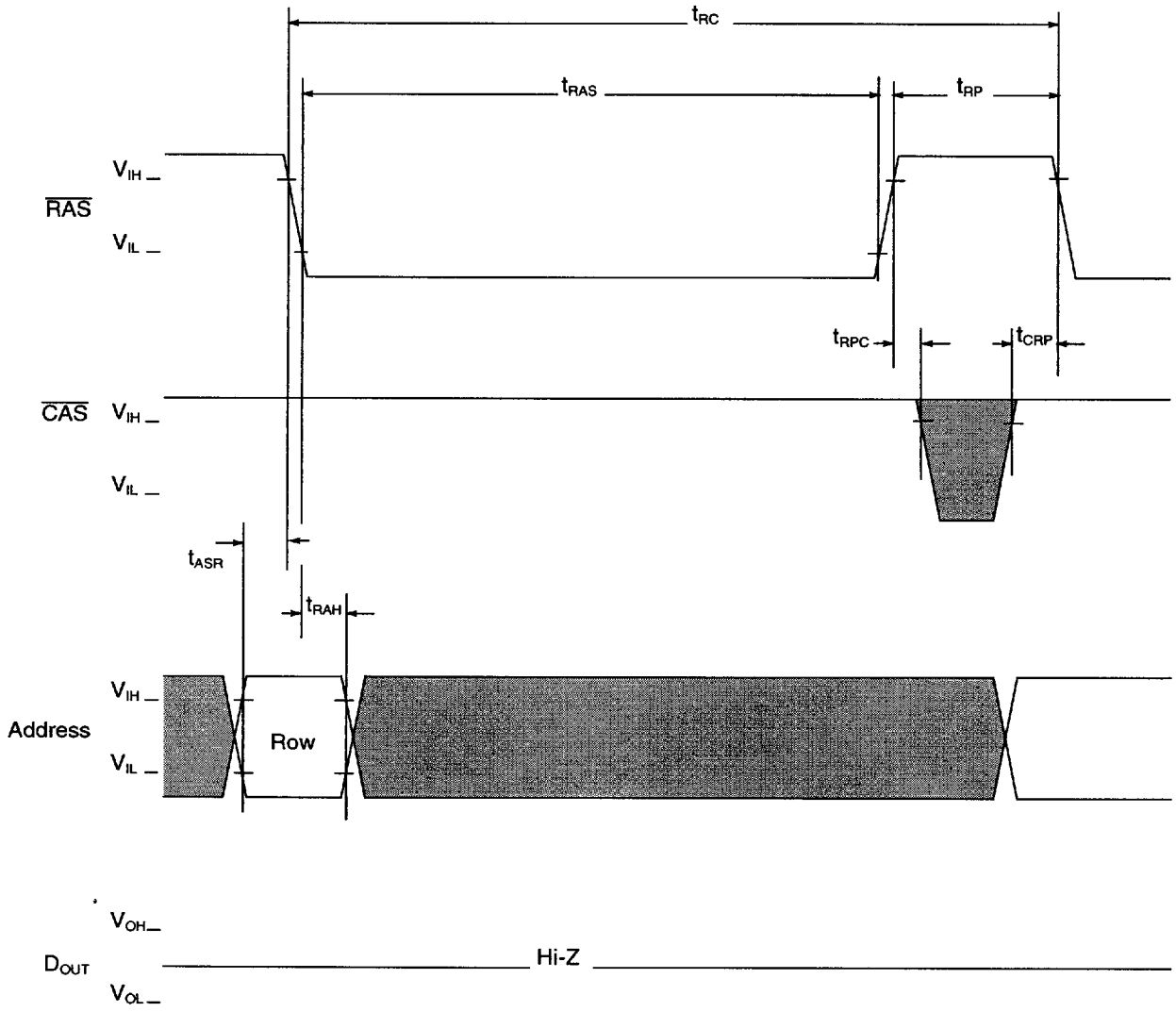
## Self Refresh Cycle (Sleep Mode)




: "H" or "L"

NOTE: Address is "H" or "L"
Once $t_{RASS}$ (min) is provided and RAS remains low, the DRAM will be in Self Refresh, commonly known as "Sleep Mode."

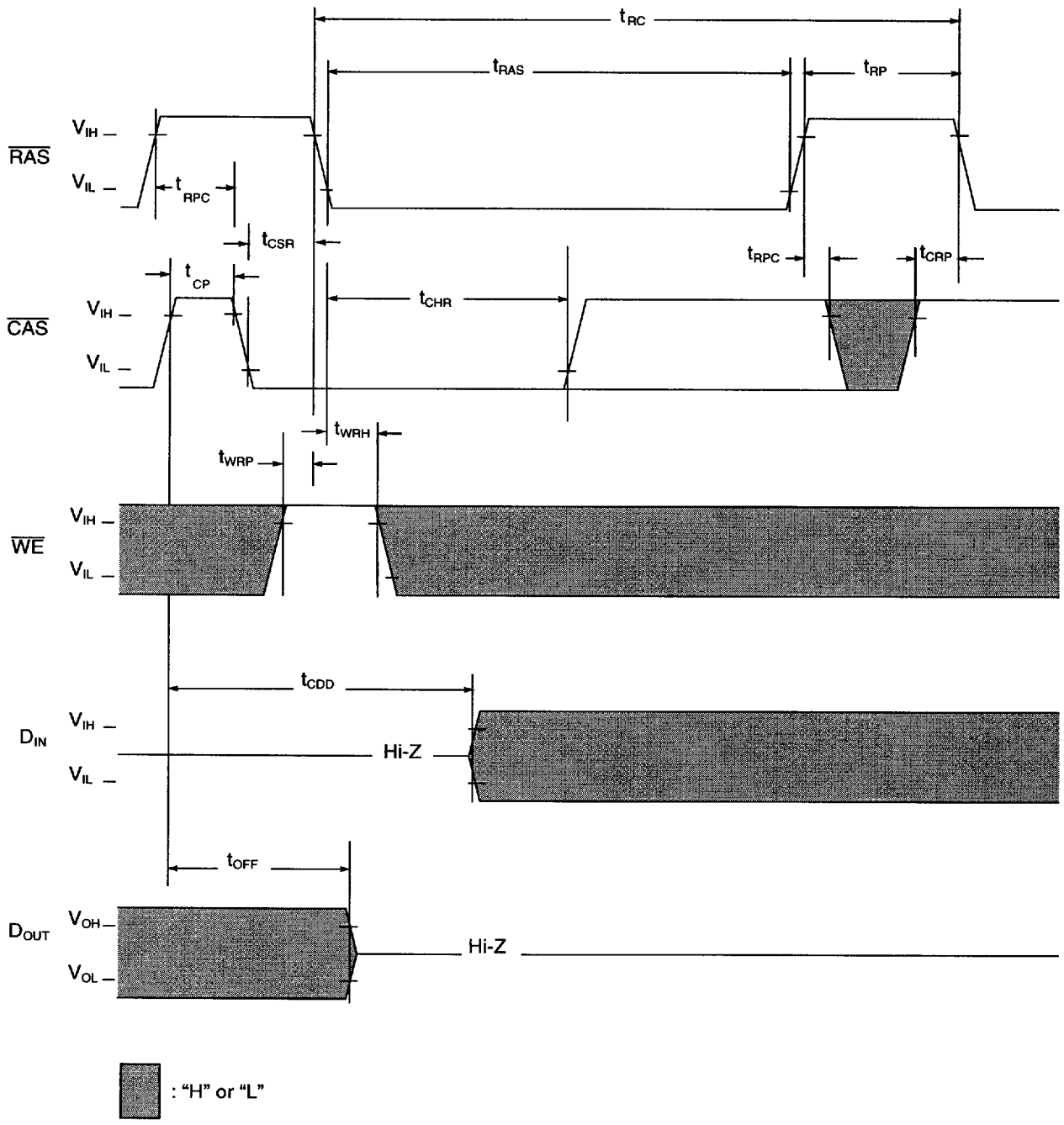
## $\overline{RAS}$ Only Refresh Cycle




: "H" or "L"

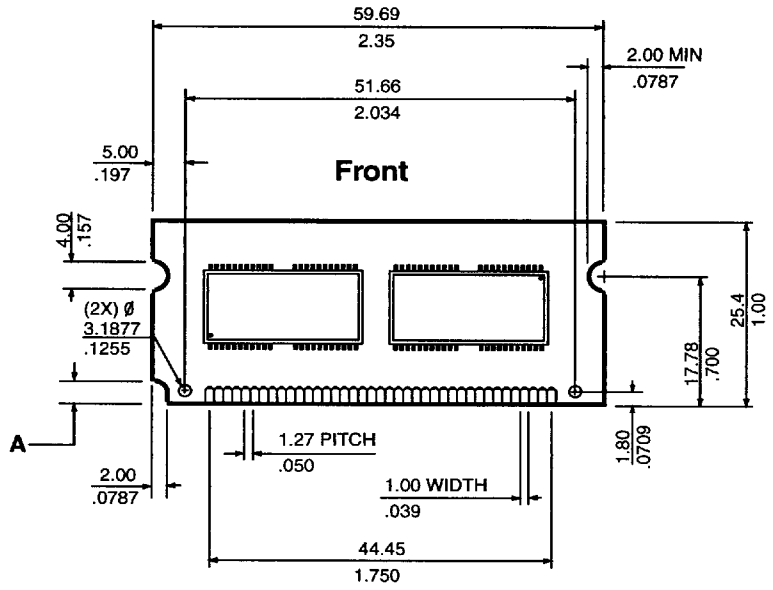
Note: $\overline{WE}$, $D_{IN}$ are "H" or "L"

## $\overline{CAS}$ Before $\overline{RAS}$ Refresh Cycle

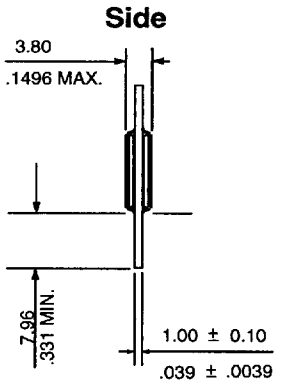



Note: Addresses are "H" or "L"

## Layout Drawing




| A = | 3.3V | 5.0V |
|---|---|---|
| | 3.175 / .125 | 6.35 / .246 |




**Note:** All dimensions are typical unless otherwise stated. Millimeters / Inches

## Revision Log

| Rev | Contents of Modification |
|---|---|
| 8/95 | Initial release of 2Mx32 EDO specification using 1Mx16 with 10/10 Addressed DRAMs. |