64M x 72 Two-Bank Registered SDRAM Module

Features

- 168-Pin Registered 8-Byte Dual In-Line Memory Module
- 64Mx72 Synchronous DRAM DIMM
- Performance:

		-75A		Units
DIMM CAS Latency		4		
f_{CK}	Clock Frequency	133	100	MHz
f_{CK}	Clock Cycle	7.5	10	ns
t_{AC}	Clock Access	5.65	5.65	ns

- Intended for 100MHz and 133MHz applications
- Inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have four internal banks
- Module has two physical banks
- Fully Synchronous to positive Clock Edge
- Programmable Operation:
  - DIMM $\overline{CAS}$ Latency: 3, 4 (Registered mode)
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8
  - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 13/10/2 Addressing (Row/Column/Bank)
- 8192 refresh cycles distributed across 64ms
- Card size: 5.25" x 0.157" x 1.70"
- Gold contacts
- SDRAMs in TSOP
- Serial Presence Detect with Write protect

Description

IBM13M64734HCA is a registered 168-Pin Synchronous DRAM Dual In-Line Memory Module (DIMM) organized as a 64Mx72 high-speed memory array and is configured as two 32M x 72 physical banks. The DIMM uses eighteen 32Mx8 SDRAMs in 400 mil TSOP packages. The DIMM achieves high-speed data-transfer rates of 100MHz and 133MHz by employing a prefetch/pipeline hybrid architecture that synchronizes the output data to a system clock.

The DIMM is intended for use in applications operating at 100MHz and 133MHz memory bus speeds. All control and address signals are re-driven through registers to the SDRAM devices. The DIMM operates in registered mode (REGE pin tied high), during which the control/address input signals are latched in the register on one rising clock edge and sent to the SDRAM devices on the following rising clock edge (data access is delayed by one clock).

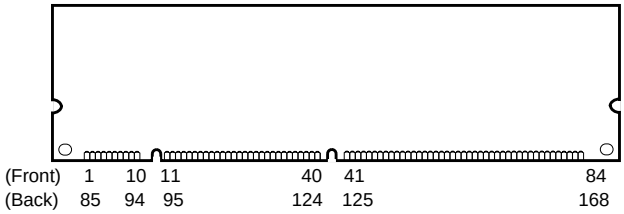
A phase-lock loop (PLL) on-board the DIMM re-drives the clock signals to the SDRAM devices and registers to minimize system clock loading. (CK0 is connected to the PLL, and CK1, CK2, and CK3 are terminated on the DIMM.) A single clock enable (CKE0) controls all devices on the DIMM, enabling the use of SDRAM power-down modes.

Prior to any access operation, the device $\overline{CAS}$ latency and burst type/length/operation type must be programmed into the DIMM by address inputs A0-A9 using the mode register set cycle. The DIMM $\overline{CAS}$ latency is one clock later due to the address and control signals being clocked to the SDRAM devices.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are programmed and locked by the DIMM manufacturer. The last 128 bytes are available to the customer and can be write protected by providing a high level to pin 81 on the DIMM. An on-board pulldown resistor keeps this in the write-enable mode.

All IBM 168-pin DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

Card Outline



Pin Description

CK0-CK3	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0	Clock Enable	CB0 - CB7	Check Bit Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQMB0 - DQMB7	Data Mask
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power (3.3V)
$\overline{WE}$	Write Enable	V_{SS}	Ground
$\overline{S}0$, $\overline{S}1$, $\overline{S}2$, $\overline{S}3$	Chip Selects	NC	No Connect
A0-A9, A11, A12	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0, BA1	SDRAM Bank Address Inputs	SA0-2	Serial Presence Detect Address Inputs
WP	SPD Write Protect	REGE	Register Enable

Pinout

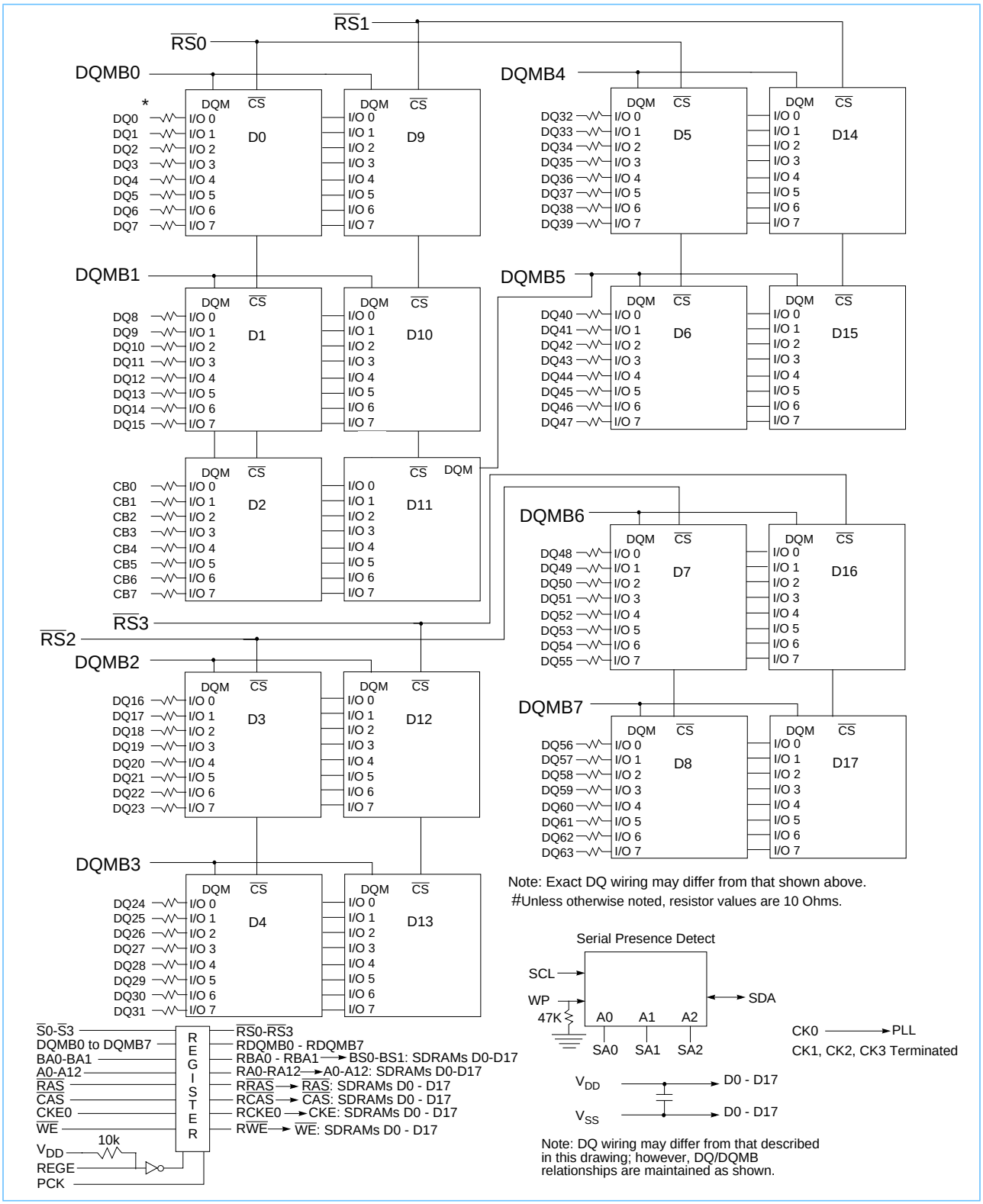
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S}2$	129	$\overline{S}3$	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	$\overline{WE}$	111	$\overline{CAS}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S}0$	114	$\overline{S}1$	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	$\overline{RAS}$	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	BA1	123	A11	60	DQ20	144	DQ52	81	WP	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	A12	63	NC	147	REGE	84	V_{DD}	168	V_{DD}

Note: All pin assignments are consistent with all 8-byte unbuffered versions.

Ordering Information

Part Number	Organization	Clock Cycle (CL, t_{RCD}, t_P)	Device Access Time	Leads	Dimension	Power
IBM13M64734HCA-75AT	64Mx72	7.5ns (3,3,3)	5.65ns	Gold	5.25" x 0.157" x 1.70"	3.3V

64Mx72 SDRAM DIMM Block Diagram (2 Bank, 32Mx8 SDRAMs)



Note: Exact DQ wiring may differ from that shown above.
#Unless otherwise noted, resistor values are 10 Ohms.

Note: DQ wiring may differ from that described in this drawing; however, DQ/DQMB relationships are maintained as shown.

Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0 - CK3	Input	Pulse	Positive Edge	The system clock inputs. All the SDRAM inputs are sampled on the rising edge of their associated clock. CK0 drives the PLL. CK1, CK2, and CK3 are terminated.
CKE0	Input	Level	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, the Suspend mode, or the Self Refresh mode.
$\overline{S}0$-$\overline{S}3$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0, 1	Input	Level	—	Selects which SDRAM bank of four is activated.
A0 - A9 A10/AP A11, A12	Input	Level	—	During a Bank Activate command cycle, A0-A12 defines the row address (RA0-RA12) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 define the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0 or BA1. If AP is low, BA0 and BA1 are used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	Level	—	Data and Check Bit Input/Output pins.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output masks, associated with one data byte, place the DQ buffers in a high-impedance state when sampled high. In Read mode, DQMB has a latency of two clock cycles in Buffered mode or three clock cycles in Registered mode, and controls the output buffers like an output enable. In Write mode, DQMB has a zero clock latency in Buffered mode and a latency of one clock cycle in Registered mode. In this case, DQMB operates as a byte mask by allowing input data to be written if it is low but blocking the write operation if it is high.
V_{DD}, V_{SS}	Supply		—	Power and ground for the module.
REGE	Input	Level	Active High (Register Mode Enable)	The Register Enable pin must be held high to permit the DIMM to operate in “registered” mode (signals re-driven to SDRAMs when clock rises, and held valid until next rising clock).
SA0 - 2	Input	Level	—	These signals are tied at the system planar to either V_{SS} or V_{DD} to configure the serial SPD EEPROM.
SDA	Input Output	Level	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup.
SCL	Input	Pulse	—	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup.
WP	Input	Level	Active High	This signal is pulled low on the DIMM to enable data to be written into the last 128 bytes of the SPD EEPROM.

Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	13	0D	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of DIMM Banks	2	02	
6 - 7	Data Width of Assembly	x72	4800	
8	Assembly Voltage Interface Levels	LVTTL	01	
9	SDRAM Device Cycle Time (CL = 3)	7.5ns	75	1, 2
10	SDRAM Device Access Time from Clock at CL=3	5.4ns	54	
11	Assembly Error Detection/Correction Scheme	ECC	02	
12	Assembly Refresh Rate/Type	SR/1X(7.8125µs)	82	
13	SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	x8	08	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8	0F	
17	SDRAM Device Attributes: Number of Device Banks	4	04	
18	SDRAM Device Attributes: $\overline{CAS}$ Latency	2, 3	06	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	Registered/Buffered with PLL	IF	
22	SDRAM Device Attributes: General	Write-1/Read Burst, Precharge All, Auto-Precharge	0E	
23	Minimum Clock Cycle at CLX-1 (CL = 2)	15.0ns	1F	1, 2
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-1 (CL = 2)	9.0ns	90	
25	Minimum Clock Cycle Time at CLX-2 (CL = 1)	N/A	00	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-2 (CL = 1)	N/A	00	
27	Minimum Row Precharge Time (t_{RP})	20.0ns	14	
28	Minimum Row Active to Row Active delay (t_{RRD})	15.0ns	0F	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	20.0ns	14	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	45.0ns	2D	
31	Module Bank Density	256MB	40	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. Minimum application clock cycle time is 7.5ns (133 MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. “R” = Alphanumeric revision code, A-Z, 0-9.
5. rr = ASCII coded revision code byte “R”.
6. ww = Binary coded decimal week code, 01-52 (Decimal) ‘ 01-34 (Hex).
7. yy = Binary coded decimal year code, 00-99 (Decimal) ‘ 00-63 (Hex).
8. ss = Serial number data byte, 00-FF (Hex).
9. These values apply to PC100 applications only.

Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
32	Address and Command Setup Time Before Clock	1.5ns	15	
33	Address and Command Hold Time After Clock	0.8ns	08	
34	Data Input Setup Time Before Clock	1.5ns	15	
35	Data Input Hold Time After Clock	0.8ns	08	
36 - 61	Reserved	Undefined	00	
62	SPD Revision	JEDEC	02	
63	Checksum for bytes 0 - 62	Checksum Data	cc	3
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Assembly Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Assembly Part Number	ASCII '13M64734HC"R"-75AT'	31334D363437333448 43rr2D373548542020	4, 5
91 - 92	Assembly Revision Code	"R" plus ASCII blank	rr20	5
93 - 94	Assembly Manufacturing Date	Year/Week Code	yyww	6, 7
95 - 98	Assembly Serial Number	Serial Number	ssssssss	8
99 - 125	Reserved	Undefined	Not Specified	
126	Module Supports this Clock Frequency	100MHz	64	9
127	Attributes for clock frequency defined in Byte 126	CLK0, CL=3, ConAP	85	9
128 - 255	Open for Customer Use	Undefined	00	

1. In a registered DIMM, data is delayed an additional clock cycle due to the on-DIMM pipeline register (that is, Device CL [clock cycles] + 1 = DIMM $\overline{CAS}$ latency).
2. Minimum application clock cycle time is 7.5ns (133 MHz).
3. cc = Checksum Data byte, 00-FF (Hex).
4. "R" = Alphanumeric revision code, A-Z, 0-9.
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8. ss = Serial number data byte, 00-FF (Hex).
9. These values apply to PC100 applications only.

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
		Register	0 - V_{DD}		
		PLL	0 - V_{DD}		
V_{OUT}	Output Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T_A	Operating Temperature (ambient)		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation		11.9	W	1, 2
I_{OUT}	Short Circuit Output Current		50	mA	1
F_{MIN}	Minimum Operating Frequency		66	MHz	

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Maximum power is calculated assuming the physical bank is in Auto Refresh Mode.

Recommended DC Operating Conditions (T_A= 0 to 70˚C)

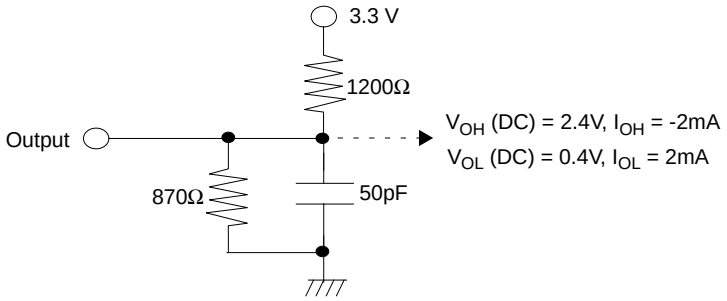
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25˚C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Organization	Units
		x72 Max.	
C_{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, BA1, A11, A12)	21	pF
C_{I2}	Input Capacitance ($\overline{RAS}$)	20	pF
C_{I3}	Input Capacitance ($\overline{CAS}$)	20	pF
C_{I4}	Input Capacitance ($\overline{S}$0, $\overline{S}$3)	13	pF
C_{I5}	Input Capacitance (CKE0)	15	pF
C_{I6}	Input Capacitance (CK0)	28	pF
C_{I7}	Input Capacitance (DQMB0 - DQMB7)	13	pF
C_{I8}	Input Capacitance (SA0 - SA2, SCL, WP)	9	pF
C_{I9}	Input Capacitance (REGE)	10	pF
C_{I10}	Input Capacitance (CK1 - CK3)	14	pF
C_{I11}	Input Capacitance (WE)	23	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	18	pF
C_{IO2}	Input/Output Capacitance (SDA)	11	pF

DC Output Load Circuit



Input/Output Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter		x72		Units	Notes
			Min.	Max.		
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	Address and Control Inputs	10	10	µA	
		DQ0-63, CB0 - 7	-2	+2		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	DQ0-63, CB0 - 7	-2	+2	µA	
		SDA	-1	+1		
V_{OH}	Output Level Output “H” Level Voltage (I_{OUT} = -2.0mA)		2.4	V_{DD}	V	1
V_{OL}	Output Level Output “L” Level Voltage (I_{OUT} = +2.0mA)		0.0	0.4		

1. See DC output load circuit.

Operating, Standby, and Refresh Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

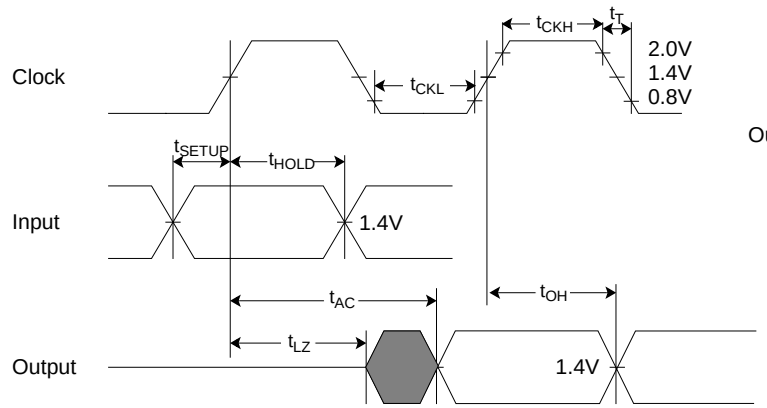
Parameter	Symbol (Physical Bank 0/ Physical Bank 1)	Test Condition	Speed -75A Clock Cycle 7.5ns	Units	Notes
Burst Operating Mode/Active Standby	I_{CC4}/I_{CC3N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	2085	mA	1, 2
Burst Operating Mode/Precharge Standby	I_{CC4}/I_{CC2N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	1815	mA	1, 2
Burst Operating Mode/Auto Refresh	I_{CC4}/I_{CC5}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	3279	mA	1, 2
Non-burst Operating Mode/Active Standby	I_{CC1}/I_{CC3N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	1929	mA	1, 2
Non-burst Operating Mode/Precharge Standby	I_{CC1}/I_{CC2N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	1407	mA	1, 2
Non-burst Operating Mode/Auto Refresh	I_{CC1}/I_{CC5}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	2964	mA	1
Active Standby/Active Standby	I_{CC3N}/I_{CC3N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	1389	mA	
Active Standby/Precharge Standby	I_{CC3N}/I_{CC2N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	1119	mA	
Active Standby/Auto Refresh	I_{CC3N}/I_{CC5}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	2424	mA	1
Precharge Standby/Precharge Standby	I_{CC2N}/I_{CC2N}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	849	mA	
Precharge Standby/Auto Refresh	I_{CC2N}/I_{CC5}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	2154	mA	1
Auto Refresh/Auto Refresh	I_{CC5}/I_{CC5}	CKE ≥ V_{IH} (min), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	3300	mA	1
Active Standby Power Down/ Active Standby Power Down	I_{CC3p}/I_{CC3p}	CKE ≤ V_{IL} (max), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	417	mA	
Active Standby Power Down/Precharge Standby Power Down	I_{CC3p}/I_{CC2p}	CKE ≤ V_{IL} (max), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	381	mA	
Precharge Standby Power Down/ Precharge Standby Power Down	I_{CC2p}/I_{CC2p}	CKE ≤ V_{IL} (max), t_{CK} = min, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	345	mA	
Precharge Standby Non-power Down/Pre-charge Standby Non-power Down (NO CLOCK)	I_{CC2NS}/I_{CC2NS}	CKE ≥ V_{IH} (min), t_{CK} = Infinity, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	156	mA	
Precharge Standby Power Down/Precharge Standby Power Down (NO CLOCK)	I_{CC2PS}/I_{CC2PS}	CKE ≤ V_{IH} (min), t_{CK} = Infinity, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	84	mA	
Self Refresh Current /Self Refresh Current	I_{CC6}/I_{CC6}	CKE ≤ V_{IH} (min), t_{CK} = Infinity, $\overline{S}0$ - $\overline{S}3$ =V_{IH} (min)	102	mA	

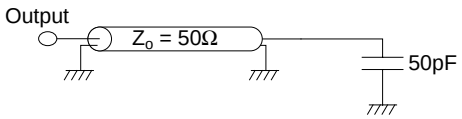
1. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed once during t_{CK}(min).
2. The specified values are obtained with the output open.

AC Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 200µs, with CKE0 held high, is required after power-up. A Precharge All Banks command must be given followed by a minimum of eight Auto (CBR) Refresh cycles before or after the Mode Register Set operation.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.
3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1.2ns (1 Volt/ns rise time).
5. In addition to meeting the transition rate specification, the clock and CKE must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
6. A 1 ms stabilization time is required by the on-board PLL circuit to phase lock its feedback signal to its reference signal.
7. All timings are specified at the input receiver of the signal, not at the DIMM connector.

AC Characteristics Diagrams





AC Output Load Circuit

Clock and Clock Enable Parameters

Symbol	Parameter	-75A max. (Device CL, t_{RCD}, t_{RP}= 3, 3, 3)		Units	Notes
		Min.	Max.		
t_{CK4}	Clock Cycle Time, DIMM $\overline{CAS}$ Latency = 4	7.5	1000	ns	1
t_{AC4}	Clock Access Time, DIMM $\overline{CAS}$ Latency = 4	—	5.65	ns	1, 2
t_{CKH}	Clock High Pulse Width	2.5	—	ns	3
t_{CKL}	Clock Low Pulse Width	2.5	—	ns	3
t_{CES}	Clock Enable Setup Time	1.65	—	ns	1
t_{CEH}	Clock Enable Hold Time	0.35	—	ns	1
t_{SB}	Power Down Mode Entry Time	0	7.5	ns	
t_T	Transition Time (Rise and Fall)	0.5	10	ns	

1. DIMM $\overline{CAS}$ latency = device CL [clock cycles] + 1 for Register mode.
2. Access time is measured at 1.4V. See AC output load circuit.
3. t_{CKH} is the pulse width of CLK measured from the positive edge to the negative edge referenced to V_{IH} (min). t_{CKL} is the pulse width of CLK measured from the negative edge to the positive edge referenced to V_{IL} (max).

Common Parameters

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{CS}	Command Setup Time	1.65	—	ns	1
t_{CH}	Command Hold Time	0.35	—	ns	1
t_{AS}	Address and Bank Select Setup Time	1.65	—	ns	1
t_{AH}	Address and Bank Select Hold Time	0.35	—	ns	1
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	—	ns	1
t_{RC}	Bank Cycle Time	67.5	—	ns	1
t_{RAS}	Active Command Period	45	100000	ns	1
t_{RP}	Precharge Time	20	—	ns	1
t_{RRD}	Bank to Bank Delay Time	15	—	ns	1
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	1	—	CLK	

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number).

Mode Register Set Style

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{RSC}	Mode Register Set Cycle Time	2	—	CLK	1

1. These parameters account for the number of clock cycles and depend on the operating frequency of the clock as follows: the number of clock cycles = specified value of timing/clock period (count fractions as a whole number).

Refresh Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{REF}	Refresh Period	—	64	ns	1, 2
t_{REFI}	Average Refresh Interval Time	—	7.813	µs	
t_{SREX}	Self Refresh Exit Time	10	—	ns	3

1. 8192 cycles
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to ‘wake up’ the device.
3. Self Refresh exit is asynchronous, requiring 10ns to ensure initiation. Self Refresh exit is complete in 10ns + t_{RC}.

Read Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3.1	—	ns	
t_{LZ}	Data Out to Low Impedance Time	0.6	—	ns	
t_{HZ3}	Data Out to High Impedance Time	3.6	6.6	ns	1
t_{DQZ}	DQM Data Out Disable Latency	3	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	-75A		Units
		Min.	Max.	
t_{DS}	Data In Setup Time	1.75	—	ns
t_{DH}	Data In Hold Time	1.05	—	ns
t_{DPL}	Data input to Precharge	15	—	ns
t_{DAL3}	Data in to Active Delay ($\overline{CAS}$ Latency = 3)	5	—	CLK
t_{DQW}	DQM Write Mask Latency	1	—	CLK

Presence Detect Read and Write Cycle

Symbol	Parameter	-75A		Units	Notes
		Min.	Max.		
f_{SCL}	SCL Clock Frequency	—	100	KHz	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs	—	100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7	—	µs	
$t_{HD:STA}$	Start Condition Hold Time	4	—	µs	
t_{LOW}	Clock Low Period	4.7	—	µs	
t_{HIGH}	Clock High Period	4	—	µs	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7	—	µs	
$t_{HD:DAT}$	Data in Hold Time	0	—	µs	
$t_{SU:DAT}$	Data in Setup Time	250	—	ns	
t_r	SDA and SCL Rise Time	—	1	µs	
t_f	SDA and SCL Fall Time	—	300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7	—	µs	
t_{DH}	Data Out Hold Time	300	—	ns	
t_{WR}	Write Cycle Time	—	15	ms	1

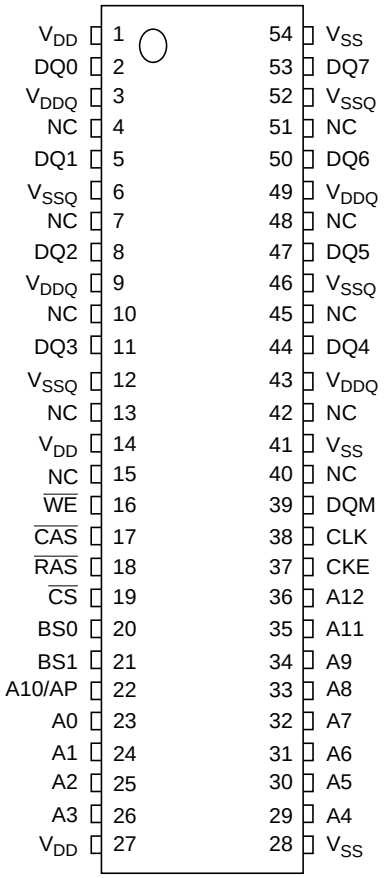
1. The write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal erase/program cycle. During the write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pull-up resistor, and the device does not respond to its slave address.

Wiring and Topology

This section contains the information needed to understand the timing relationships presented in AC Characteristics beginning on page 12. Each timing parameter is measured at the first receiving device (SDRAM DQ pin for data input, register input pin for address and control, and PLL Clk input pin for clock). This section will enable the user to understand the pin numbers on the DIMM, the net structures, and the loading associated with these devices. For detailed timing analysis, contact the IBM Marketing Representative for simulation models. Modeling is strongly recommended to determine delay adders of the entire net structure.

Pin Assignments for the 256Mbit SDRAM Planar Component

TOP VIEW



54-pin Plastic TSOP(II) 400mil

16Mbit x 8 I/O x 4 Bank

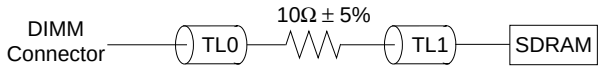
The table below describes the physical DQ wiring information for each SDRAM on the DIMM. Note that the DQ wiring is different from that described in the Block Diagram on page 4; the DQs are scrambled within the same device for wiring optimization.

Data Wiring Cross Reference

DQ SDRAM Designator	DQ SDRAM Pin Number	Device position to DIMM Tab Data I/O[1]																	
		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17
DQ0	2	7	38	15	47	CB2	55	23	63	31	0	33	8	41	CB1	48	16	55	25
DQ1	5	6	37	14	46	CB7	54	22	62	30	1	34	9	42	CB5	49	17	57	26
DQ2	8	5	36	13	45	CB3	53	21	61	29	2	35	10	40	CB4	50	18	58	27
DQ3	11	4	39	12	44	CB6	52	20	60	28	3	32	11	43	CB0	51	19	59	24
DQ4	44	3	32	11	43	CB0	51	19	59	24	4	39	12	44	CB6	52	20	60	28
DQ5	47	2	35	10	40	CB4	50	18	58	27	5	36	13	45	CB3	53	21	61	29
DQ6	50	1	34	9	42	CB5	49	17	57	26	6	37	14	46	CB7	54	22	62	30
DQ7	53	0	33	8	41	CB1	48	16	56	25	7	38	15	47	CB2	55	23	63	31

1. These numbers can be associated with the corresponding DIMM tab pin by referencing the DIMM connector pinout on page 3 of this specification. Example: DQ14 at the DIMM tab (pin 19) is wired to both SDRAM device position D2, pin 5 and SDRAM D11, pin 50.

Data Topology



Note: Transmission lines (“TL”) are represented as cylinders and labeled with length designators. These are the only lines which represent physical trace segments.
For more detailed topology information please refer to the current PC133 SDRAM Registered DIMM specification.

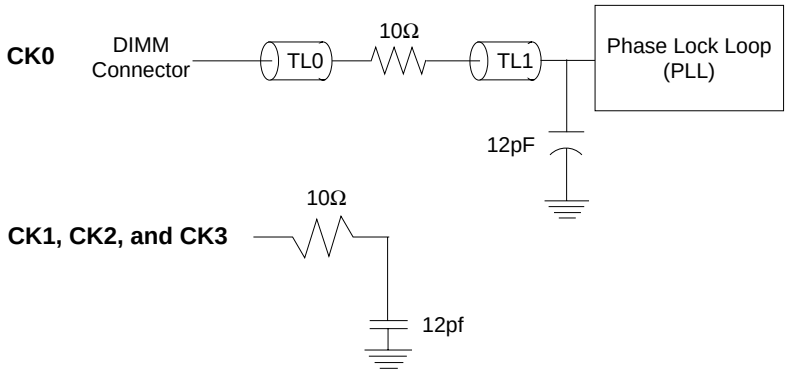
TL0		TL1		Total		Unit
Min	Max	Min	Max	Min	Max	
0.126	0.345	1.013	1.415	1.145	1.658	in.

The table below describes the input wiring for each clock on the DIMM.

Clock Input Wiring

CK0	CK1	CK2	CK3
PLL CLK Input Pin 24	Termination RC	Termination RC	Termination RC

Clock Topology



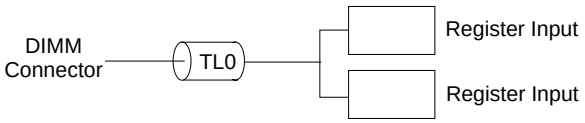
TL0	TL1	Unit
0.127	2.647	in.

The table below describes the address and control information for each signal on the DIMM. Note that several signals are double loaded at the input of the register.

Register Input Wiring Register Type:ALVCF162835

Register Pin number	Register 1 Signal	Register 2 Signal	Register 3 Signal
30	CLK	CLK	CLK
31	$\overline{CAS}$	NC	DQMB0
33	$\overline{RAS}$	NC	DQMB4
34	A1	BS1	DQMB1
36	A0	A11	DQMB5
37	A3	A10	A12
38	A2	BS0	A12
40	A5	A8	S0
41	A4	A9	NC
42	A7	A6	$\overline{WE}$
43	A6	A7	$\overline{WE}$
44	A9	A4	NC
45	A8	A5	S2
47	BS0	A2	DQMB6
48	A10	A3	DQMB2
49	A11	A0	NC
51	BS1	A1	NC
52	$\overline{CKE0}$	$\overline{RAS}$	DQMB7
54	CKE0	$\overline{CAS}$	DQMB3

Address/Control Signal Topology



TL0		Unit
Min	Max	
0.199	1.336	in.

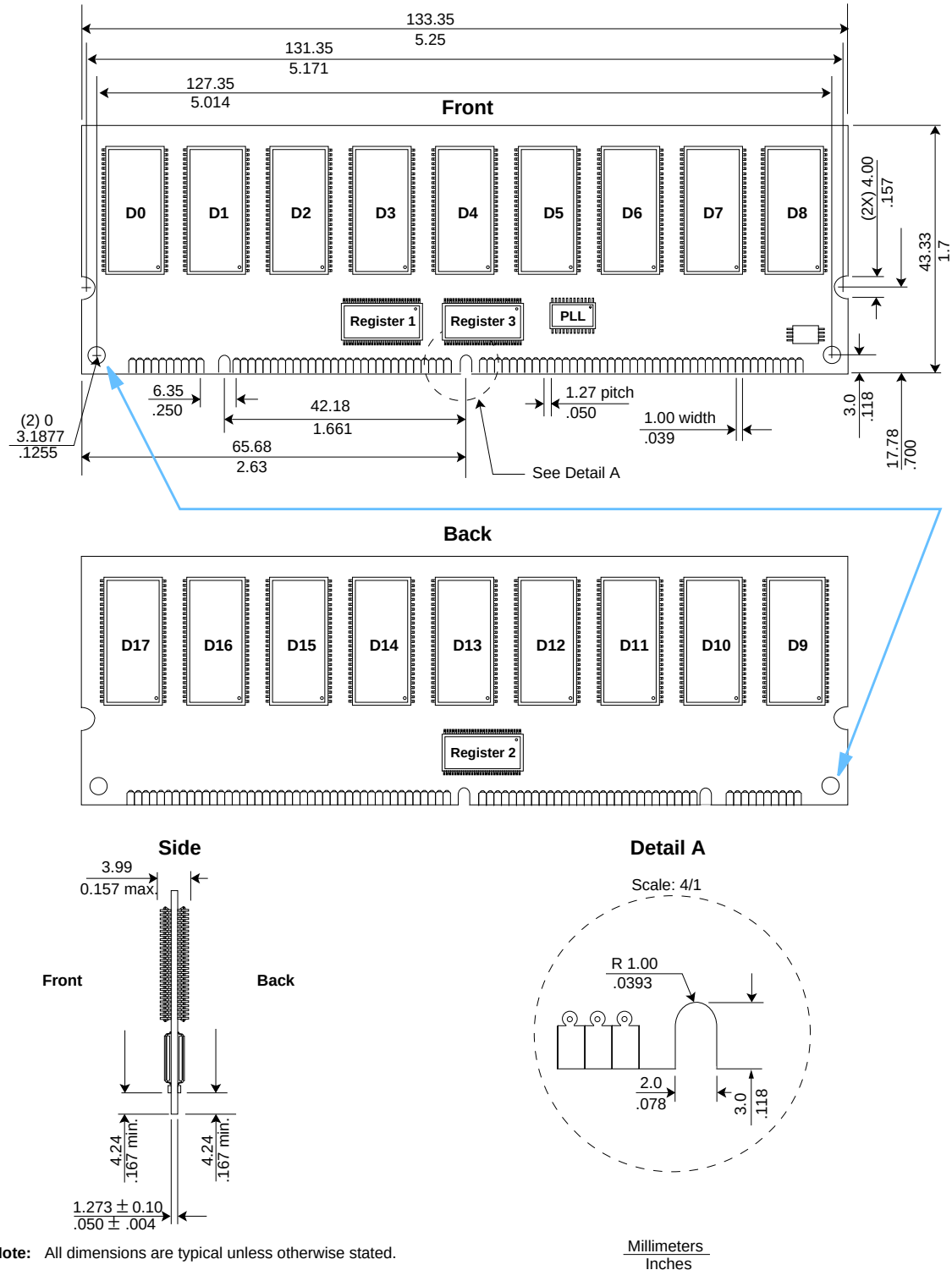
Note: Each Signal has two register input loads with the exception of DQMBs and Chip Select which have one.
For more detailed topology information please refer to the current PC133 SDRAM Registered DIMM specification.

Functional Description and Timing Diagrams

Refer to the IBM PC133 256Mb Synchronous DRAM data sheet (document 29L0000) for the functional description and timing diagrams for buffered-mode operation.

Refer to the IBM Application Notes *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

Layout Drawing



Note: All dimensions are typical unless otherwise stated.

Revision Log

Rev	Contents of Modification
5/00	Initial release

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