Preliminary

2M x 64/72 1 Bank Unbuffered SDRAM Module

Features

- 168 Pin (emerging) JEDEC Standard, Unbuffered 8 Byte Dual In-line Memory Module
- 2Mx64/72 Synchronous DRAM DIMM
- Performance:

		10	12	Units
	$\overline{CAS}$ Latency	3	3	
f_{CK}	Clock Frequency	100	83	MHz
t_{CK}	Clock Cycle	10	12	ns
t_{AC}	Clock Access Time	8	9	ns

- All inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V $\pm$ 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have 2 internal banks
- Module has 1 bank
- Fully Synchronous to positive Clock Edge
- Programmable Operation:
  - -CAS Latency: 1, 2, 3
  - -Burst Type: Sequential or Interleave
  - -Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  - -Operation: Burst Read and Write <u>or</u> Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 11/9/1 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 5.25" x 1.15" x 0.157"
- Au contacts
- SDRAMS in TSOP Type II Package

Description

IBM13N2649JC/ IBM13N2739JC are unbuffered 168-pin Synchronous DRAM Dual In-line Memory Modules (DIMMs) which are organized as 2Mx64 and 2Mx72 high-speed memory arrays. The DIMMs use 8 (2Mx64) or 9 (2Mx72) 2Mx8 SDRAMs in 400mil TSOP II packages. The DIMMs achieve high speed data transfer rates of up to 100MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1-N rule while allowing very low burst power.

The DIMMs are intended to comply with all JEDEC standards set for 168 pin unbuffered SDRAM DIMMs.

All control, address, and data input/output circuits (except CKE0) are synchronized with the positive edge of the externally supplied clock inputs.

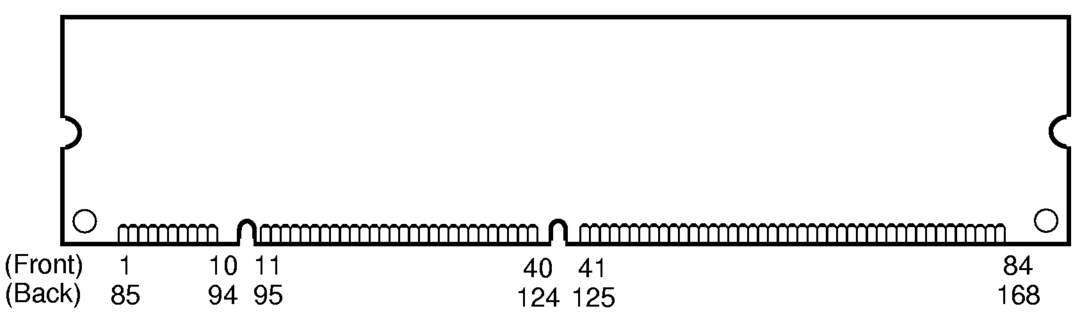
All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}/\overline{S2}$, DQMB, and CKE0 signals. A command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the DIMM by address inputs A0-A9 during the mode register set cycle.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25” long space-saving footprint. Related products include both EDO DRAM and SDRAM unbuffered DIMMs in both non-parity x64 and ECC-Optimized x72 configurations.

Card Outline



Pin Description

CK0, CK1	Clock Inputs	DQ0 - DQ63	Data Input/Output
CK2, CK3	Unused (terminated) Clock Inputs	CB0 - CB7	Check Bit Data Input/Output
CKE0	Clock Enable	DQMB0 - DQMB7	Data Mask
$\overline{RAS}$	Row Address Strobe	V_{CC}	Power (3.3V)
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	NC	No Connect
$\overline{S0}$, $\overline{S2}$	Chip Selects	SCL	Serial Presence Detect Clock Input
A0 - A9	Address Inputs	SDA	Serial Presence Detect Data Input/Output
A10 /AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0	SDRAM Bank Address		

Pinout

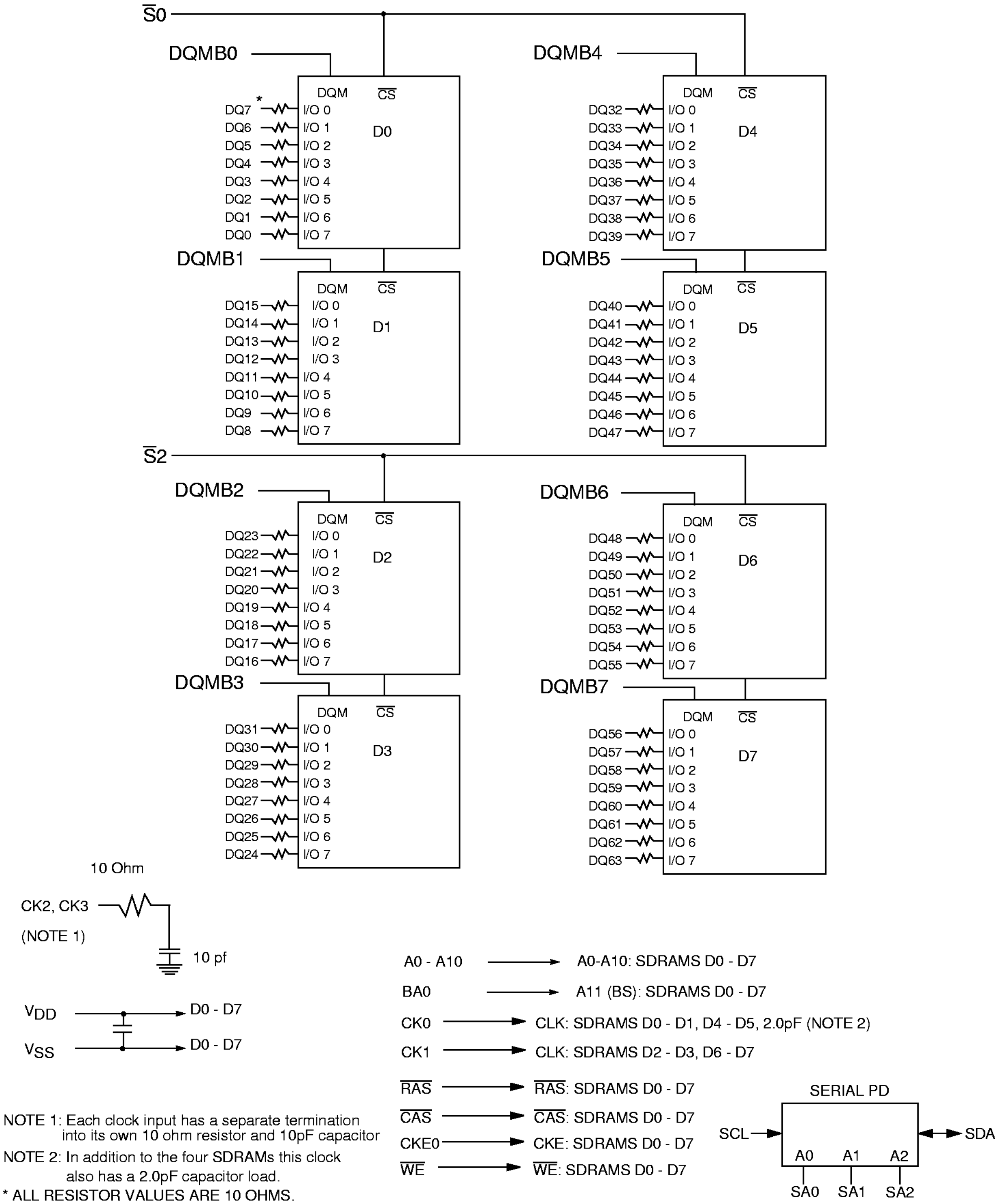
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S2}$	129	NC	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{CC}	110	V_{CC}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{CC}	90	V_{CC}	27	$\overline{WE}$	111	$\overline{CAS}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{CC}	133	V_{CC}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S0}$	114	NC	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	$\overline{RAS}$	52	CB2	136	CB6	73	V_{CC}	157	V_{CC}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	*CK2	163	*CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{CC}	143	V_{CC}	80	NC	164	NC
18	V_{CC}	102	V_{CC}	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	V_{CC}	124	V_{CC}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{CC}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	NC	63	NC	147	NC	84	V_{CC}	168	V_{CC}

Note: All pin assignments are consistent for all 8 Byte unbuffered versions. Check Bits (CB0 - CB7) are applicable only to the X72 DIMM, for the x64 DIMM these pins are no connects (NC). * CK2, CK3 are terminated to a load equivalent of four SDRAMs.

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13N2649JC-10T	2Mx64	10ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N2649JC-12T	2Mx64	12ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N2739JC-10T	2Mx72	10ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N2739JC-12T	2Mx72	12ns	Au	5.25"x1.15"x0.157"	3.3V

2Mx64 SDRAM DIMM Block Diagram (1 Bank, x8 SDRAMs)

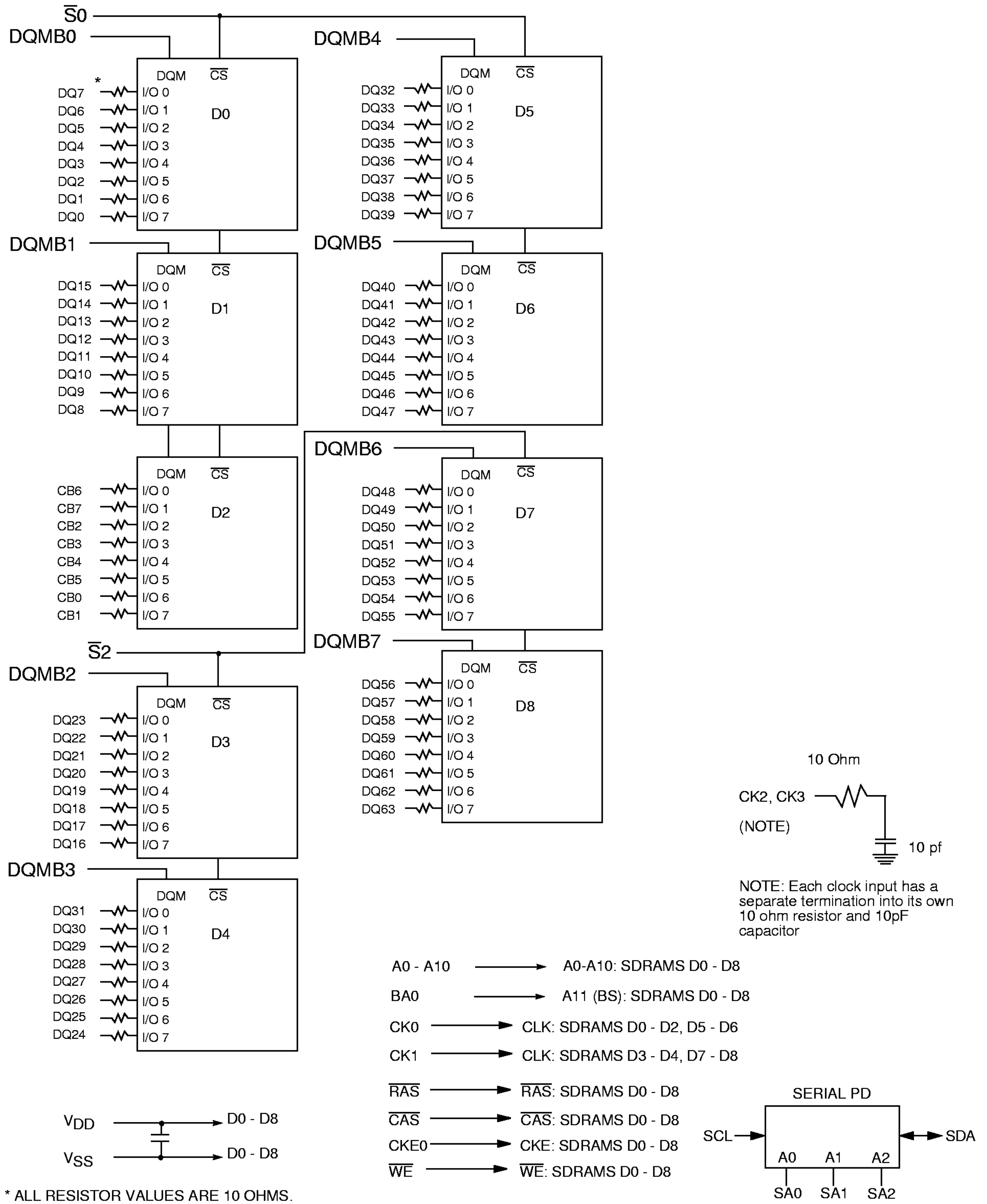


NOTE 1: Each clock input has a separate termination into its own 10 ohm resistor and 10pF capacitor

NOTE 2: In addition to the four SDRAMs this clock also has a 2.0pF capacitor load.

* ALL RESISTOR VALUES ARE 10 OHMS.

2Mx72 SDRAM DIMM Block Diagram (1 Bank, x8 SDRAMs)



Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0, CK1	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0	Input	Level	Active High	Activates the CK0 and CK1 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0}$,$\overline{S2}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A8 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regardless of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	Level	—	Data and Check Bit Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V_{DD}, V_{SS}	Supply			Power and ground for the module.

Serial Presence Detect

Byte #	Description		SPD Entry Value	Serial PD Data Entry (Hexadecimal)
0	Number of Serial PD Bytes Written during Production		128	80
1	Total Number of Bytes in Serial PD device		256	08
2	Fundamental Memory Type		SDRAM	04
3	Number of Row Addresses on Assembly		11	0B
4	Number of Column Addresses on Assembly		9	09
5	Number of DIMM Banks		1	01
6 - 7	Data Width of Assembly	2M x 64	x64	4000
		2M x 72	x72	4800
8	Assembly Voltage Interface Levels		LVTTL	01
9	SDRAM Device Cycle Time	-10	10.0ns	A0
		-12	12.0ns	C0
10	SDRAM Device Access Time from Clock	-10	8.0ns	80
		-12	9.0ns	90
11	Assembly Error Detection/Correction Scheme	2M x 64	Non-Parity	00
		2M x 72	ECC	02
12	Assembly Refresh Rate/Type		SR/1X(15.625us)	80
13	SDRAM Device Width		x8	08
14	Error Checking SDRAM Device Width	2M x 64	N/A	00
		2M x 72	x8	08
15	SDRAM Device Attr: Min Clk Delay, Random Col Access		1 Clock	01
16	SDRAM Device Attributes: Burst Lengths Supported		1,2,4,8, Full Page	8F
17	SDRAM Device Attributes: Number of Device Banks		2	02
18	SDRAM Device Attributes: $\overline{CAS}$ Latency		1, 2, 3	07
19	SDRAM Device Attributes: $\overline{CS}$ Latency		0	01
20	SDRAM Device Attributes: $\overline{WE}$ Latency		0	01
21	SDRAM Module Attributes		Unbuffered	00
22	SDRAM Device Attributes: General		Write-1/Read Burst, Precharge All, Auto-Precharge	0E
23 - 62	Reserved		Undefined	Not Specified
63	Checksum for bytes 0 - 62		Checksum Data	cc
64 - 71	Manufacturers' JEDEC ID Code		IBM	A400000000000000
72	Assembly Manufacturing Location		Toronto, Canada	91
			Vimercate, Italy	53
73 - 90	Assembly Part Number	2M x 64, -10	ASCII '13N2649JC"R"-10T'	31334E323634394A43rr2D31305420202020
		2M x 64, -12	ASCII '13N2649JC"R"-12T'	31334E323634394A43rr2D31325420202020
		2M x 72, -10	ASCII '13N2739JC"R"-10T'	31334E323733394A43rr2D31305420202020
		2M x 72, -12	ASCII '13N2739JC"R"-12T'	31334E323733394A43rr2D31325420202020
91 - 92	Assembly Revision Code		"R" plus ASCII blank	rr20
93 - 94	Assembly Manufacturing Date		Week/Year Code	wwyy
95 - 98	Assembly Serial Number		Serial Number	ssssssss
99 - 127	Reserved		Undefined	Not Specified

cc = Checksum Data byte, 00-FF (Hex)
"R" = Alphanumeric revision code, A-Z, 0-9
rr = ASCII coded revision code byte "R"
ww = Binary coded decimal week code, 00-53 (Decimal) → 00-35 (Hex)
yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex)
ss = Serial number data byte, 00-FF (Hex)

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
V_{OUT}	Output Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T_{OPR}	Operating Temperature		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation		9.0	W	1
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

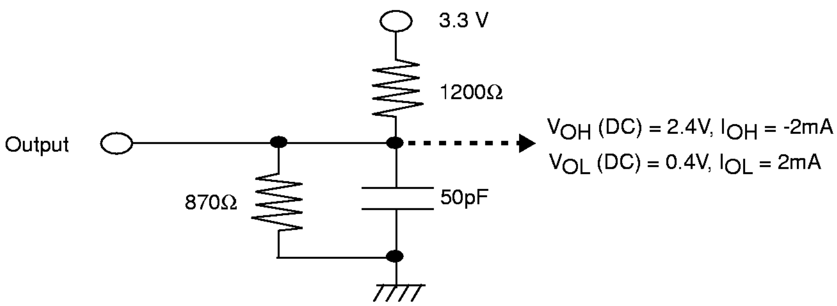
Recommended DC Operating Conditions (T_A= 0 to 70˚C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS} .

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V $\pm$ 0.3V)

Symbol	Parameter	Organization		Units
		x64 Max.	x72 Max.	
C_{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	50	53	pF
C_{I2}	Input Capacitance (CKE0)	50	53	pF
C_{I3}	Input Capacitance ($\overline{S0}$, $\overline{S2}$)	27	30	pF
C_{I4}	Input Capacitance (CK0, CK1)	40	40	pF
C_{I5}	Input Capacitance (CK2, CK3)	25	25	pF
C_{I6}	Input Capacitance (DQMB0 - DQMB7)	15	18	pF
C_{I7}	Input Capacitance (SA0 - SA2, SCL)	9	9	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB15)	9	10	pF
C_{IO2}	Input/Output Capacitance (SDA)	11	11	pF



DC Output Load Circuit

Output Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter		x64		x72			
			Min.	Max.	Min.	Max.	Units	Notes
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, CKE0, CK0, A0-A9, A10/AP, BA0	-8	+8	-9	+9	μA	
		CK0	-4	+4	-5	+5		
		CK1	-4	+4	-4	+4		
		$\overline{S0}$	-4	+4	-5	+5		
		$\overline{S2}$	-4	+4	-4	+4		
		DQMB1	-1	+1	-2	+2		
		DQMB0, 2, 3, 4, 5, 6, 7	-1	+1	-1	+1		
		DQ0 - 63	-1	+1	-1	+1		
		CB0 - 7	0	0	-1	+1		
		SA0, SA1, SA2, SCL, SDA	-1	+1	-1	+1		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	DQ0 - 63, SDA	-1	+1	-1	+1	μA	
		CB0 - 7	0	0	-1	+1		
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2.0mA)		2.4	V_{DD}	2.4	V_{DD}	V	1
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = +2.0mA)		0.0	0.4	0.0	0.4		

1. See DC output load circuit.

Standby and Refresh Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Parameter	Symbol	Test Condition		Organization X64	Organization X72	Units	Notes
Precharge Standby Current in Power Down Mode	ICC_1P	CKE0 ≤ V_{IL}(max), t_{CK} = 15ns		24	27	mA	
	ICC_1PS	CKE0 ≤ V_{IL}(max), t_{CK} = Infinity		16	18	mA	
Precharge Standby Current in Non-Power Down Mode	ICC_1N	CKE0 ≥ V_{IH}(min), t_{CK} = 15ns Input Change every 30ns		240	270	mA	$\overline{S0}$, $\overline{S2}$ = High
	ICC_1NS	CKE0 ≥ V_{IH}(min), t_{CK} = Infinity No Input Change		120	135	mA	
Active Standby Current in Power Down Mode	ICC_2P	CKE0 ≤ V_{IL}(max), t_{CK} = 15ns		24	18	mA	
	ICC_2PS	CKE0 ≤ V_{IL}(max), t_{CK} = Infinity		16	10	mA	
Active Standby Current in Non-Power Down Mode	ICC_2N	CKE0 ≥ V_{IH}(min), t_{CK} = 15ns Input Change every 30ns		240	270	mA	$\overline{S0}$, $\overline{S2}$ = High
	ICC_2NS	CKE0 ≥ V_{IH}(min), t_{CK} = Infinity No Input Change		160	180	mA	
Auto (CBR) Refresh Current	ICC_3	$\overline{CAS}$ Latency = 1 $t_{RC} \geq t_{RC}$(min)	-10	680	765	mA	1,2,3
			-12	600	675	mA	
		$\overline{CAS}$ Latency = 2 $t_{RC} \geq t_{RC}$(min)	-10	840	945	mA	
			-12	720	810	mA	
		$\overline{CAS}$ Latency = 3 $t_{RC} \geq t_{RC}$(min)	-10	1000	1125	mA	
			-12	880	990	mA	
Self Refresh Current	ICC_4	CKE0 ≤ 0.2V		16	10	mA	
Serial PD Device Standby Current	I_{SB}	V_{IN} = GND or V_{DD}		10	10	µA	4

1. The specified values are valid when addresses are changed no more than once during t_{CK}(min).
2. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
3. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min).
4. V_{DD} = 3.3V

Operating Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Speed Sort	Organization X64	Organization X72	Units	Notes
I_{CC5}	Operating Current Burst Length = 1	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	90 ns	-10	760	855	mA	1, 2
				108 ns	-12	640	720		
			CL=2	75 ns	-10	1000	1125		
				90 ns	-12	880	990		
			CL=3	80 ns	-10	1120	1260		
				96 ns	-12	960	1080		
I_{CC6}	Operating Current Burst Length = 2	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	120 ns	-10	600	675	mA	1, 2, 3
				144 ns	-12	520	585		
			CL=2	90 ns	-10	920	1035		
				108 ns	-12	800	900		
			CL=3	90 ns	-10	1120	1260		
				108 ns	-12	960	1080		
I_{CC7}	Operating Current Burst Length = 4	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	180 ns	-10	520	585	mA	1, 2, 3
				216 ns	-12	440	495		
			CL=2	120 ns	-10	840	945		
				144 ns	-12	720	810		
			CL=3	110 ns	-10	1080	1215		
				132 ns	-12	960	1080		
I_{CC8}	Operating Current Burst Length = 8	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	300 ns	-10	480	540	mA	1, 2, 3
				360 ns	-12	400	450		
			CL=2	180 ns	-10	760	855		
				216 ns	-12	680	765		
			CL=3	150 ns	-10	1040	1170		
				180 ns	-12	880	990		
I_{CC9}	Operating Current Burst Length = Full Page	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	$t_{RC} = \infty$ t_{CK}=30 ns	-10	360	405	mA	1, 2, 3
				$t_{RC} = \infty$ t_{CK}=36 ns	-12	320	360		
			CL=2	$t_{RC} = \infty$ t_{CK}=15 ns	-10	600	675		
				$t_{RC} = \infty$ t_{CK}=18 ns	-12	520	585		
			CL=3	$t_{RC} = \infty$ t_{CK}=10 ns	-10	840	945		
				$t_{RC} = \infty$ t_{CK}=12 ns	-12	760	855		

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQ's are changed no more than once during t_{CK}(min).
3. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
4. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL = 100pf.

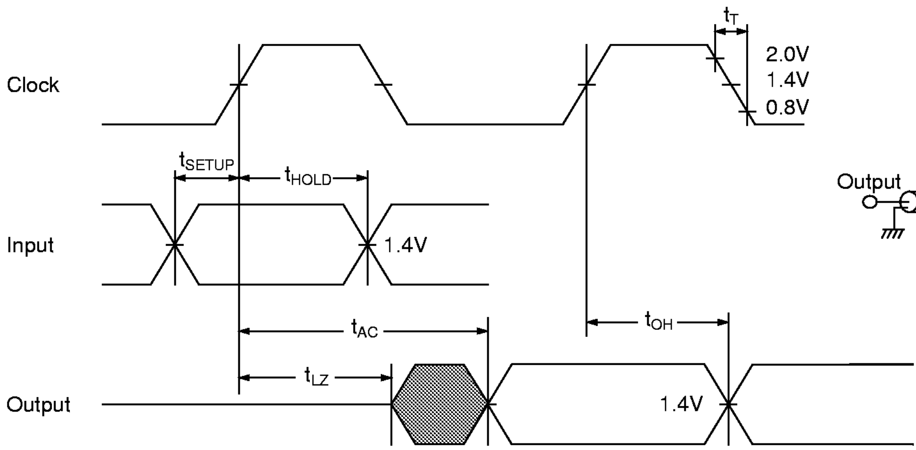
Operating Currents (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

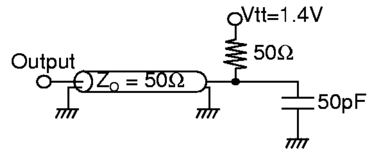
Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Speed Sort	Organization X64	Organization X72	Units	Notes
I_{CC10}	Operating Current 1-N Rule (Continuous Read/Write cycles with new column address registered each clock cycle)	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	$t_{RC} = \infty$ t_{CK}=30 ns	-10	680	765	mA	1, 2
				$t_{RC} = \infty$ t_{CK}=36 ns	-12	640	720		
			CL=2	$t_{RC} = \infty$ t_{CK}=15 ns	-10	1040	1170		
				$t_{RC} = \infty$ t_{CK}=18 ns	-12	920	1035		
			CL=3	$t_{RC} = \infty$ t_{CK}=10 ns	-10	1400	1575		
				$t_{RC} = \infty$ t_{CK}=12 ns	-12	1200	1350		
I_{CCA}	Serial PD Device Active Power Supply Current	SCL Clock Frequency = 100kHz				1.0	1.0	mA	4

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQ's are changed no more than once during t_{CK}(min).
3. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
4. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL = 100pf.

AC Characteristics (T_A= 0 to +70˚C, V_{DD}= 3.3V ± 0.3V)

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.





AC Output Load Circuit

3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1ns.
5. In addition to meeting the transition rate specification, the clock and CKEn must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Note: All AC timing information below refers to the timings at the SDRAM devices. DIMM level XTK/IBIS models are available to perform system level modeling and timing analysis.

Clock and Clock Enable Parameters

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	10	**100MHz**	12	**83MHz**	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	15	**66MHz**	18	**56MHz**	ns	
t_{CK1}	Clock Cycle Time, $\overline{CAS}$ Latency = 1	30	**33MHz**	36	**28MHz**	ns	
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	8	—	9	ns	1, 2
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	9	—	10	ns	1, 2
t_{AC1}	Clock Access Time, $\overline{CAS}$ Latency = 1	—	27	—	27	ns	1, 2
t_{CKH}	Clock High Pulse Width	3.5	—	4	—	ns	3
t_{CKL}	Clock Low Pulse Width	3.5	—	4	—	ns	3
t_{CES}	Clock Enable Set-up Time	3	—	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	1	—	ns	
t_{CESP}	CKE Set-up Time (Power down mode)	3	—	3	—	ns	
t_T	Transition Time (Rise and Fall)	1	30	1	30	ns	

1. Access time is measured at 1.4V. See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then (trise/2-0.5)ns should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional [(trise+tfall)/2-1]ns.

Common Parameters

Symbol	Parameter	-10		-12		Units
		Min.	Max.	Min.	Max.	
t_{CS}	Command Setup Time	3	—	3	—	ns
t_{CH}	Command Hold Time	1	—	1	—	ns
t_{AS}	Address and Bank Select Set-up Time	3	—	3	—	ns
t_{AH}	Address and Bank Select Hold Time	1	—	1	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	36	—	ns
t_{RC}	Bank Cycle Time	75	120000	96	120000	ns
t_{RAS}	Active Command Period	45	120000	60	120000	ns
t_{RP}	Precharge Time	30	—	36	—	ns
t_{RRD}	Bank to Bank Delay Time	20	—	24	—	ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	1	—	1	—	CLK

Refresh Cycle

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{SREX}	Self Refresh Exit Time	2CLK + t_{RC}	—	2CLK + t_{RC}	—	ns	3
t_{REF}	Refresh Period	—	64	—	64	ms	1, 2

1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
3. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to tRC is satisfied once the Self Refresh Exit command is registered.

Read Cycle

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	3	—	3	—	ns	
t_{HZ3}	Data Out to High Impedance Time, CL= 3	3	8	3	8	ns	1
t_{HZ2}	Data Out to High Impedance Time, CL= 2	3	8	3	10	ns	1
t_{HZ1}	Data Out to High Impedance Time, CL= 1	3	15	3	18	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	-10		-12		Units
		Min.	Max.	Min.	Max.	
t_{DS}	Data In Set-up Time	3	—	3	—	ns
t_{DH}	Data In Hold Time	1	—	1	—	ns
t_{DPL}	Data input to Precharge	15	—	15	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	0	—	CLK

Clock Frequency and Latency

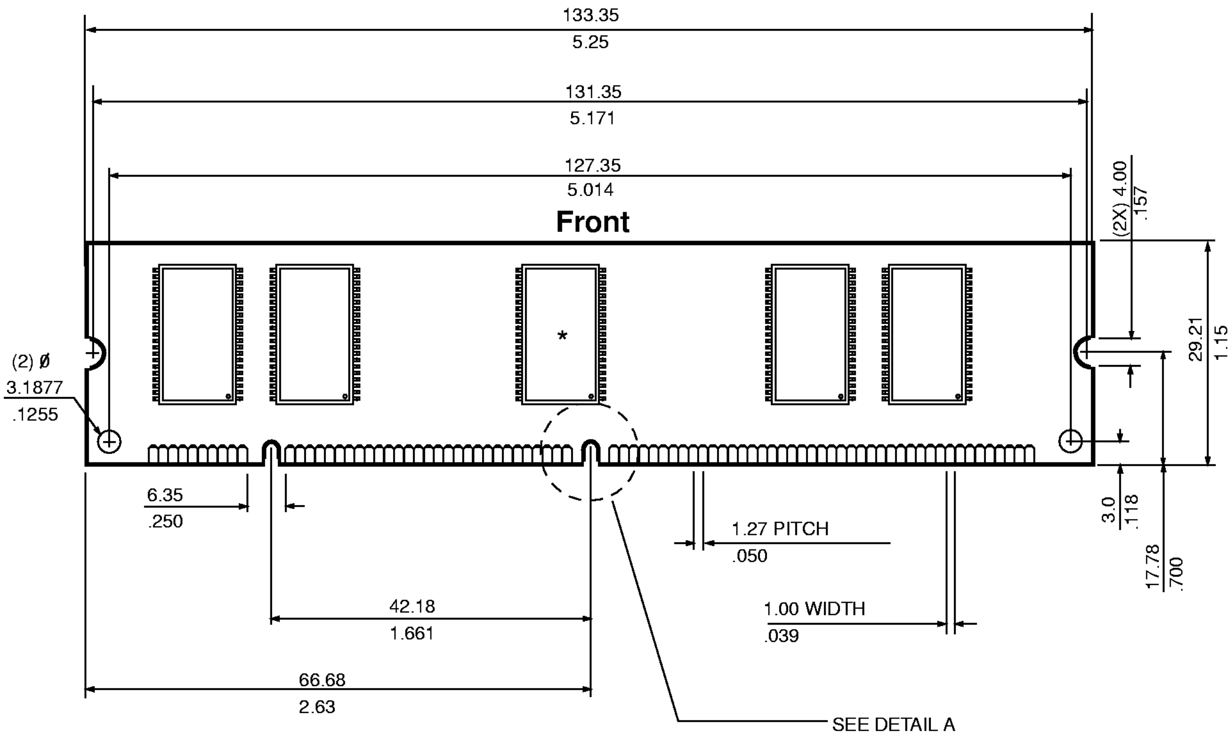
Symbol	Parameter	Speed Sort						Units
		-10			-12			
fCK	**Clock Frequency**	**100**	**66**	**33**	**83**	**56**	**28**	**MHz**
t_{CK}	Clock Cycle Time	10	15	30	12	18	36	ns
t_{AA}	$\overline{\text{CAS}}$ Latency	3	2	1	3	2	1	CLK
t_{RCD}	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	3	2	1	3	2	1	CLK
t_{RL}	$\overline{\text{RAS}}$ Latency	6	4	2	6	4	2	CLK
t_{RC}	Bank Cycle Time	8	5	3	8	5	3	CLK
t_{RAS}	Minimum Bank Active Time	5	3	2	5	3	2	CLK
t_{RP}	Precharge Time	3	2	1	3	2	1	CLK
t_{DPL}	Data In to Precharge	2	1	1	2	1	1	CLK
t_{DAL}	Data In to Active/Refresh	5	3	2	5	3	2	CLK
t_{RRD}	Bank to Bank Delay Time	2	2	1	2	2	1	CLK
t_{CCD}	$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ Delay Time	1	1	1	1	1	1	CLK
t_{WL}	Write Latency	0	0	0	0	0	0	CLK
t_{DQW}	DQM Write Mask Latency	0	0	0	0	0	0	CLK
t_{DQZ}	DQM Data Disable Latency	2	2	2	2	2	2	CLK
t_{CSL}	Clock Suspend Latency	1	1	1	1	1	1	CLK

Functional Description and Timing Diagrams

Refer to the IBM 16Mb Synchronous DRAM data sheet, document SA14-4711-04 (Revised 10/96), for the functional description and timing diagrams for SDRAM operation.

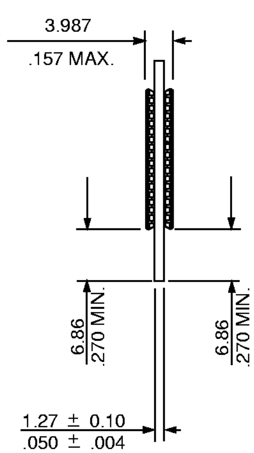
Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

Layout Drawing

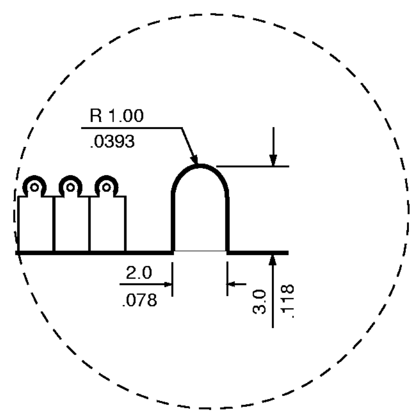


* Note: on x72 Module Only

Side



Detail A
SCALE 4/1



Note: All dimensions are typical unless otherwise stated. Millimeters / Inches