

PRELIMINARY

4M x 64/72 1 Bank Unbuffered SDRAM Module

Features

- 168 Pin (emerging) JEDEC Standard, Unbuffered 8 Byte Dual In-line Memory Module
- 4Mx64/72 Synchronous DRAM DIMM
- Performance:

		10	12	Units
	CAS Latency	3	3	
f _{CK}	Clock Frequency	100	83	MHz
t _{CK}	Clock Cycle	10	12	ns
t _{AC}	Clock Access Time	8	9	ns

- All inputs and outputs are LVTTTL (3.3V) compatible
- Single 3.3V $\pm$ 0.3V Power Supply
- Single Pulsed $\overline{\text{RAS}}$ interface
- SDRAMs have 2 internal banks
- Module has 1bank
- Fully Synchronous to positive Clock Edge

- Programmable Operation:
 - CAS Latency: 1, 2, 3
 - Burst Type: Sequential or Interleave
 - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
 - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 11/10/1 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 5.25" x 1.15" x 0.157"
- Au contacts
- SDRAMs in TSOP Type II Package

Description

IBM13N4649C/ IBM13N4739C are unbuffered 168-pin Synchronous DRAM Dual In-line Memory Modules (DIMMs) which are organized as 4Mx64 and 4Mx72 high-speed memory arrays. The DIMMs use 16 (4Mx64) or 18 (4Mx72) 4Mx4 SDRAMs in 400mil TSOP II packages. The DIMMs achieve high speed data transfer rates of up to 100MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1-N rule while allowing very low burst power.

The DIMMs are intended to comply with all JEDEC standards set for 168 pin unbuffered SDRAM DIMMs.

All control, address, and data input/output circuits (except CKE0 and CKE1) are synchronized with the positive edge of the externally supplied clock inputs.

All inputs are sampled at the positive edge of each externally supplied clock (CK0 - CK3). Internal operating modes are defined by combinations the $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$,

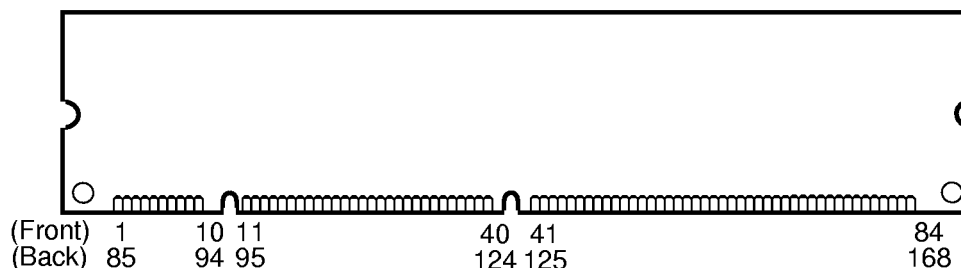
$\overline{\text{S0}}$ - $\overline{\text{S3}}$, DQMB, and CKE - CKE1 signals. A command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{\text{CAS}}$ latency, burst type, burst length, and burst operation type must be programmed into the DIMM by address inputs A0-A9 during the mode register set cycle.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products include both EDO DRAM and SDRAM unbuffered DIMMs in both non-parity x64 and ECC-Optimized x72 configurations.

Card Outline



Pin Description

CK0 - CK3	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0 - CKE1	Clock Enables	CB0 - CB7	Check Bit Data Input/Output
$\overline{\text{RAS}}$	Row Address Strobe	DQMB0 - DQMB7	Data Mask
$\overline{\text{CAS}}$	Column Address Strobe	V_{DD}	Power (3.3V)
$\overline{\text{WE}}$	Write Enable	V_{SS}	Ground
$\overline{\text{S0}}, \overline{\text{S2}}$	Chip Selects	NC	No Connect
A0 - A9	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0	SDRAM Bank Address	SA0-2	Serial Presence Detect Address Inputs

Pinout

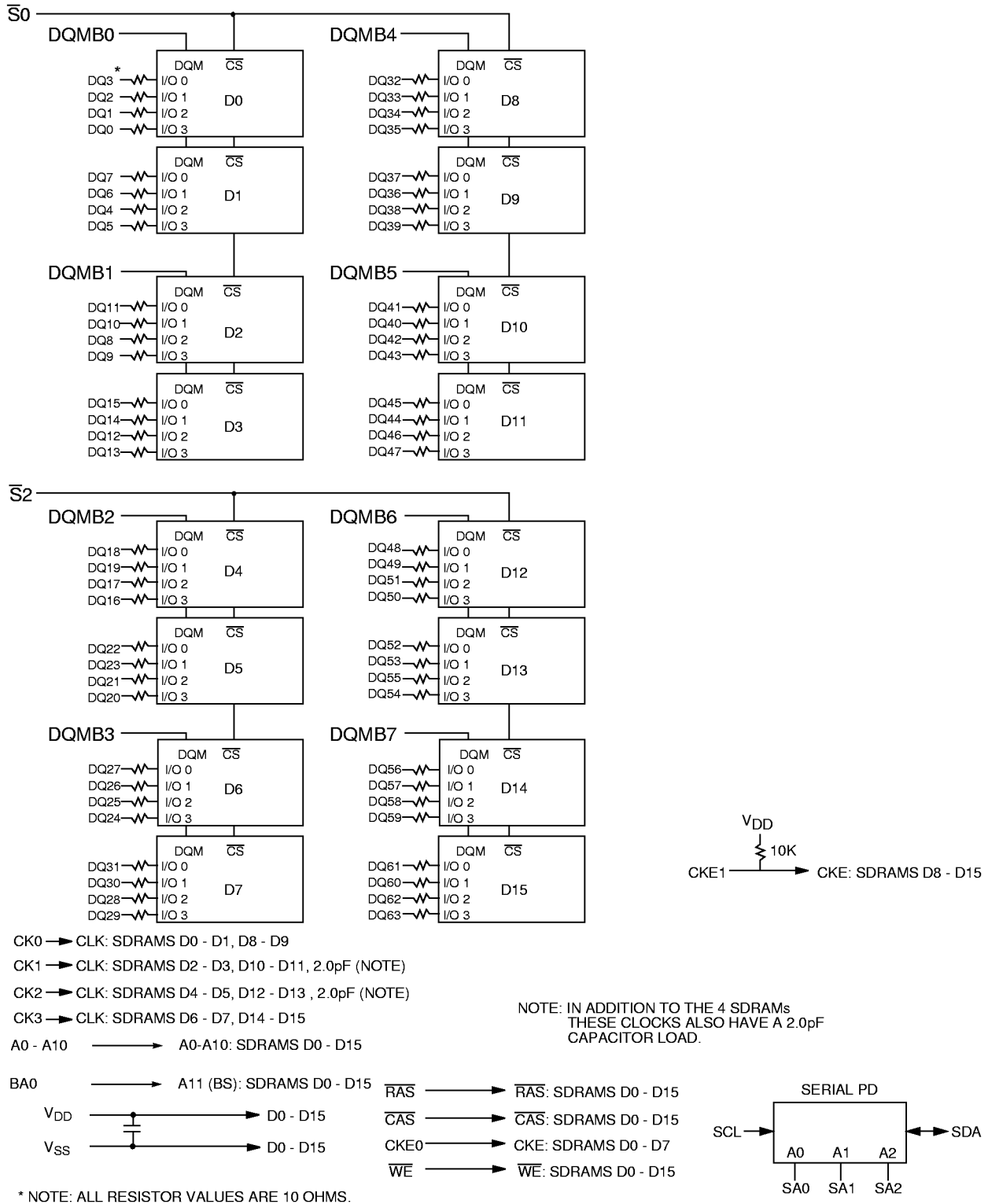
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{\text{S2}}$	129	NC	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	$\overline{\text{WE}}$	111	$\overline{\text{CAS}}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{\text{S0}}$	114	NC	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	$\overline{\text{RAS}}$	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	NC	63	*CKE1	147	NC	84	V_{DD}	168	V_{DD}

Note: All pin assignments are consistent for all 8 Byte unbuffered versions. Check Bits (CB0 - CB7) are applicable only to the X72 DIMM, for the x64 DIMM these pins are no connects (NC). *CKE1 is terminated with a 10K ohm pull-up resistor.

Ordering Information

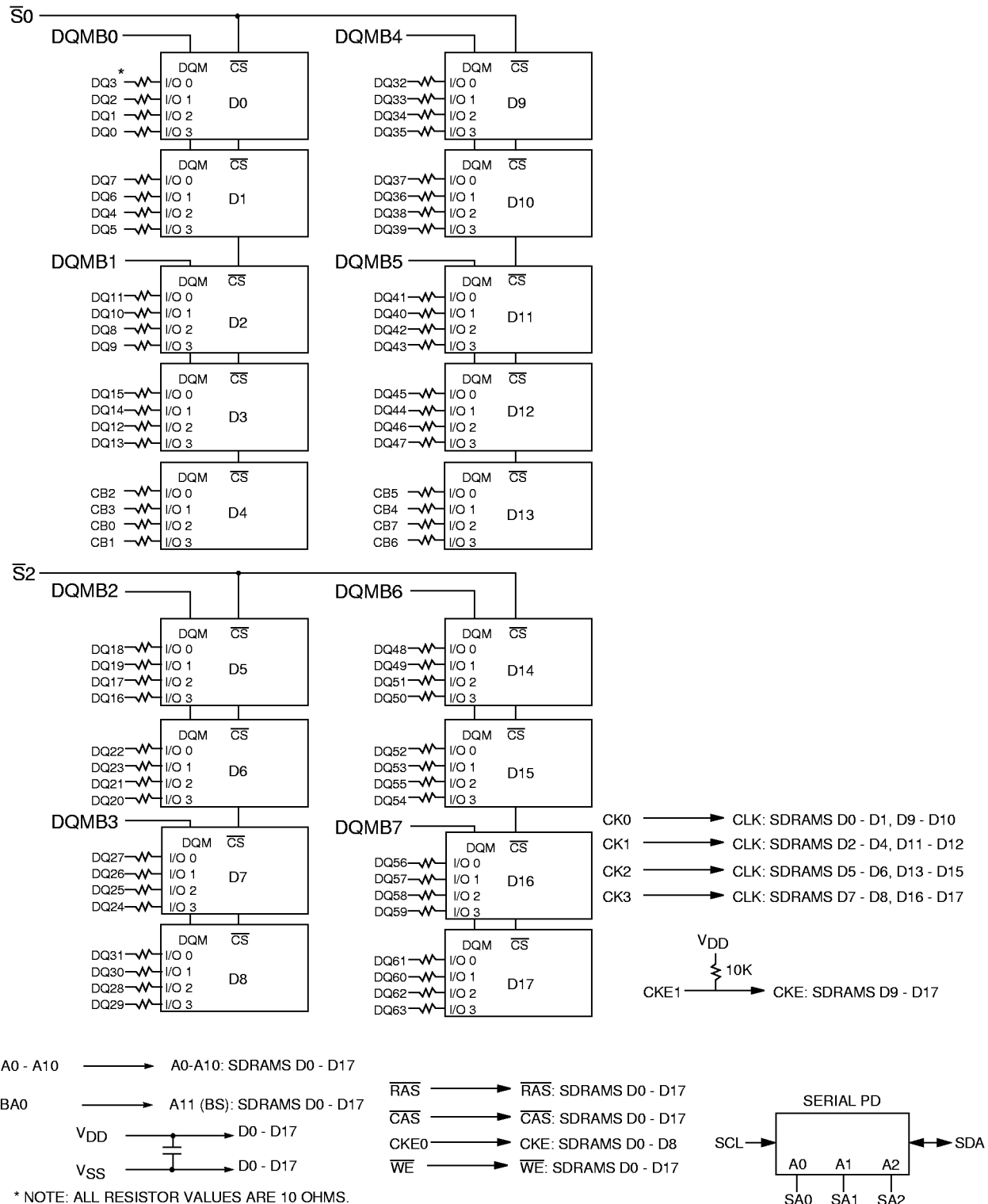
Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13N4649CC-10T	4Mx64	10ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N4649CC-12T	4Mx64	12ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N4739CC-10T	4Mx72	10ns	Au	5.25"x1.15"x0.157"	3.3V
IBM13N4739CC-12T	4Mx72	12ns	Au	5.25"x1.15"x0.157"	3.3V

4Mx64 SDRAM DIMM Block Diagram (1 Bank, x4 SDRAMs)



* NOTE: ALL RESISTOR VALUES ARE 10 OHMS.

4Mx72 SDRAM DIMM Block Diagram (1 Bank, x4 SDRAMs)





Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0 - CK3	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0, CKE1	Input	Level	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0}$, $\overline{S2}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regardless of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	Level	—	Data and Check Bit Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
V _{DD} , V _{SS}	Supply			Power and ground for the module.

Serial Presence Detect

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)
0	Number of Serial PD Bytes Written during Production	128	80
1	Total Number of Bytes in Serial PD device	256	08
2	Fundamental Memory Type	SDRAM	04
3	Number of Row Addresses on Assembly	11	0B
4	Number of Column Addresses on Assembly	10	0A
5	Number of DIMM Banks	1	01
6 - 7	Data Width of Assembly	4M x 64	x64
		4M x 72	x72
8	Assembly Voltage Interface Levels	LVTTL	01
9	SDRAM Device Cycle Time	-10	10.0ns
		-12	12.0ns
10	SDRAM Device Access Time from Clock	-10	8.0ns
		-12	9.0ns
11	Assembly Error Detection/Correction Scheme	4M x 64	Non-Parity
		4M x 72	ECC
12	Assembly Refresh Rate/Type	SR/1X(15.625us)	80
13	SDRAM Device Width	x4	04
14	Error Checking SDRAM Device Width	4M x 64	N/A
		4M x 72	x4
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F
17	SDRAM Device Attributes: Number of Device Banks	2	02
18	SDRAM Device Attributes: CAS Latency	1, 2, 3	07
19	SDRAM Device Attributes: CS Latency	0	01
20	SDRAM Device Attributes: WE Latency	0	01
21	SDRAM Module Attributes	Unbuffered	00
22	SDRAM Device Attributes: General	Write-1/Read Burst, Precharge All, Auto-Precharge	0E
23 - 62	Reserved	Undefined	Not Specified
63	Checksum for bytes 0 - 62	Checksum Data	cc
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000
72	Assembly Manufacturing Location	Toronto, Canada	91
		Vimercate, Italy	53
73 - 90	Assembly Part Number	4M x 64, -10	ASCII '13N4649CC"R"-10T'
		4M x 64, -12	ASCII '13N4649CC"R"-12T'
		4M x 72, -10	ASCII '13N4739CC"R"-10T'
		4M x 72, -12	ASCII '13N4739CC"R"-12T'
91 - 92	Assembly Revision Code	"R" plus ASCII blank	rr20
93 - 94	Assembly Manufacturing Date	Week/Year Code	wwyy
95 - 98	Assembly Serial Number	Serial Number	ssssssss
99 - 127	Reserved	Undefined	Not Specified

cc = Checksum Data byte, 00-FF (Hex)
 "R" = Alphanumeric revision code, A-Z, 0-9
 rr = ASCII coded revision code byte "R"
 ww = Binary coded decimal week code, 00-53 (Decimal) → 00-35 (Hex)
 yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex)
 ss = Serial number data byte, 00-FF (Hex)



Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V _{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V _{IN}	Input Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
V _{OUT}	Output Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T _{OPR}	Operating Temperature		0 to +70	°C	1
T _{STG}	Storage Temperature		-55 to +125	°C	1
P _D	Power Dissipation		18.0	W	1
I _{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

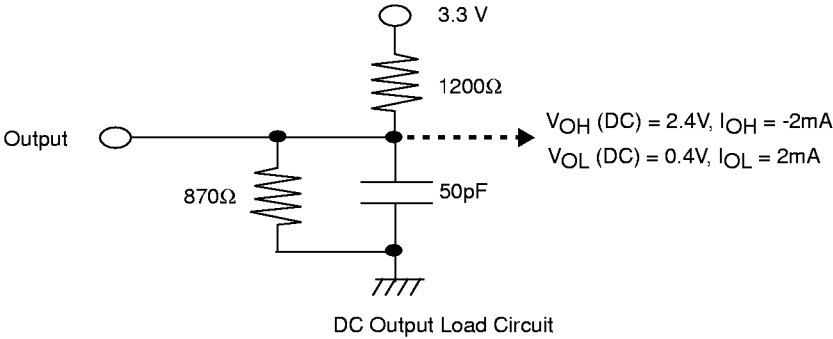
Recommended DC Operating Conditions (T_A = 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V _{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V _{IH}	Input High Voltage	2.0	—	V _{DD} + 0.3	V	1
V _{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A = 25°C, f = 1MHz, V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	Organization		Units
		x64 Max.	x72 Max.	
C _{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	80	86	pF
C _{I2}	Input Capacitance (CKE0 - CKE1)	46	50	pF
C _{I3}	Input Capacitance ($\overline{\text{S0}}$, $\overline{\text{S2}}$)	42	46	pF
C _{I4}	Input Capacitance (CK0 - CK3)	40	40	pF
C _{I5}	Input Capacitance (DQMB0 - DQMB7)	18	20	pF
C _{I6}	Input Capacitance (SA0 - SA2, SCL)	9	9	pF
C _{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	10	10	pF
C _{IO2}	Input/Output Capacitance (SDA)	11	11	pF



Output Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter		x64		x72		Units	Notes
			Min.	Max.	Min.	Max.		
I _{I(L)}	Input Leakage Current, any input (0.0V ≤ V _{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	RAS, CAS, WE, A0-A9, A10/AP, BA0	-16	+16	-18	+18	μA	
		CK0, CK3	-4	+4	-4	+4		
		CK1, CK2	-4	+4	-5	+5		
		CKE0, CKE1	-8	+8	-9	+9		
		S0	-8	+8	-10	+10		
		S2	-8	+8	-8	+8		
		DQMB1, 5	-2	+2	-3	+3		
		DQMB0, 2, 3, 4, 6, 7	-2	+2	-2	+2		
		DQ0 - 63	-1	+1	-1	+1		
		CB0 - 7	0	0	-1	+1		
	SA0, SA1, SA2, SCL, SDA	-1	+1	-1	+1			
I _{O(L)}	Output Leakage Current (D _{OUT} is disabled, 0.0V ≤ V _{OUT} ≤ 3.6V)	DQ0 - 63	-1	+1	-1	+1	μA	
		CB0 - 7	0	0	-1	+1		
		SDA	-1	+1	-1	+1		
V _{OH}	Output Level Output "H" Level Voltage (I _{OUT} = -2.0mA)		2.4	V _{DD}	2.4	V _{DD}	V	1
V _{OL}	Output Level Output "L" Level Voltage (I _{OUT} = +2.0mA)		0.0	0.4	0.0	0.4		

1. See DC output load circuit.

**Standby and Refresh Currents** ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Test Condition		Organization		Units	Notes
				X64	X72		
Precharge Standby Current in Power Down Mode	ICC _{1P}	CKE0, 1 ≤ V _{IL} (max), t _{CK} = 15ns		48	54	mA	
	ICC _{1PS}	CKE0, 1 ≤ V _{IL} (max), t _{CK} = Infinity		32	36	mA	
Precharge Standby Current in Non-Power Down Mode	ICC _{1N}	CKE0, 1 ≥ V _{IH} (min), t _{CK} = 15ns Input Change every 30ns		480	540	mA	S0 - S3 = High
	ICC _{1NS}	CKE0, 1 ≥ V _{IH} (min), t _{CK} = Infinity No Input Change		240	270	mA	
Active Standby Current in Power Down Mode	ICC _{2P}	CKE0, 1 ≤ V _{IL} (max), t _{CK} = 15ns		48	54	mA	
	ICC _{2PS}	CKE0, 1 ≤ V _{IL} (max), t _{CK} = Infinity		32	36	mA	
Active Standby Current in Non-Power Down Mode	ICC _{2N}	CKE0, 1 ≥ V _{IH} (min), t _{CK} = 15ns Input Change every 30ns		480	540	mA	S0 - S3 = High
	ICC _{2NS}	CKE0, 1 ≥ V _{IH} (min), t _{CK} = Infinity No Input Change		320	360	mA	
Auto (CBR) Refresh Current	ICC ₃	CAS Latency = 1 t _{RC} ≥ t _{RC} (min)	-10	1360	1530	mA	1,2,3
			-12	1200	1350	mA	
		CAS Latency = 2 t _{RC} ≥ t _{RC} (min)	-10	1680	1890	mA	
			-12	1440	1620	mA	
		CAS Latency = 3 t _{RC} ≥ t _{RC} (min)	-10	2000	2250	mA	
			-12	1760	1980	mA	
Self Refresh Current	ICC ₄	CKE0, 1 ≤ 0.2V		32	36	mA	
Serial PD Device Standby Current	I _{SB}	V _{IN} = GND or V _{DD}		10	10	μA	4
1. The specified values are valid when addresses are changed no more than once during t_{CK}(min). 2. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min). 3. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min). 4. V_{DD} = 3.3V							

Operating Currents ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Test Condition	CAS Latency	$t_{RC}(\text{min})$	Speed Sort	Organization		Units	Notes
						X64	X72		
I_{CC5}	Operating Current Burst Length = 1	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	90 ns	-10	1520	1710	mA	1, 2
				108 ns	-12	1280	1440		
			CL=2	75 ns	-10	2000	2250		
				90 ns	-12	1760	1980		
			CL=3	80 ns	-10	2240	2520		
				96 ns	-12	1920	2160		
I_{CC6}	Operating Current Burst Length = 2	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	120 ns	-10	1200	1350	mA	1, 2, 3
				144 ns	-12	1040	1170		
			CL=2	90 ns	-10	1840	2070		
				108 ns	-12	1600	1800		
			CL=3	90 ns	-10	2240	2520		
				108 ns	-12	1920	2160		
I_{CC7}	Operating Current Burst Length = 4	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	180 ns	-10	1040	1170	mA	1, 2, 3
				216 ns	-12	880	990		
			CL=2	120 ns	-10	1600	1800		
				144 ns	-12	1360	1530		
			CL=3	110 ns	-10	2080	2340		
				132 ns	-12	1840	2070		
I_{CC8}	Operating Current Burst Length = 8	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	300 ns	-10	880	990	mA	1, 2, 3
				360 ns	-12	720	810		
			CL=2	180 ns	-10	1440	1620		
				216 ns	-12	1280	1440		
			CL=3	150 ns	-10	2000	2250		
				180 ns	-12	1680	1890		
I_{CC9}	Operating Current Burst Length = Full Page	$t_{RC} = \text{Infinity}$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	$t_{RC} = \infty$ $t_{CK}=30$ ns	-10	640	720	mA	1, 2, 3
				$t_{RC} = \infty$ $t_{CK}=36$ ns	-12	560	630		
			CL=2	$t_{RC} = \infty$ $t_{CK}=15$ ns	-10	1120	1260		
				$t_{RC} = \infty$ $t_{CK}=18$ ns	-12	960	1080		
			CL=3	$t_{RC} = \infty$ $t_{CK}=10$ ns	-10	1600	1800		
				$t_{RC} = \infty$ $t_{CK}=12$ ns	-12	1360	1530		

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQ's are changed no more than once during $t_{CK}(\text{min})$.
3. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
4. Input pulse levels $V_{DD} \times 0.1$ to $V_{DD} \times 0.9$, input rise and fall times 10ns, input and output timing levels $V_{DD} \times 0.5$, output load 1 TTL gate and CL = 100pf.

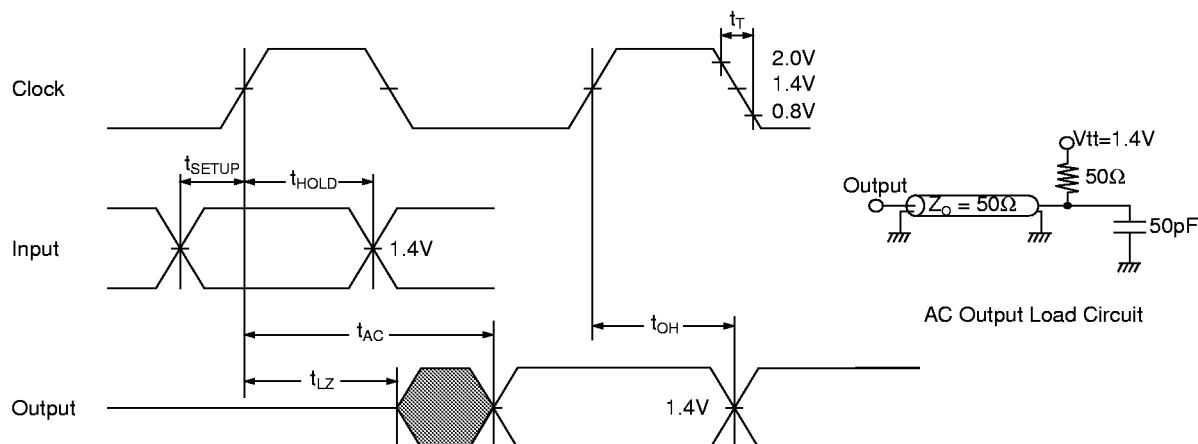
**Operating Currents** ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Test Condition	CAS Latency	t _{RC} (min)	Speed Sort	Organization		Units	Notes
						X64	X72		
I _{CC10}	Operating Current 1-N Rule (Continuous Read/Write cycles with new column address registered each clock cycle)	t _{RC} = Infinity t _{CK} ≥ t _{CK} (min) I _O = 0mA	CL=1	t _{RC} = ∞ t _{CK} =30 ns	-10	1360	1530	mA	1, 2
				t _{RC} = ∞ t _{CK} =36 ns	-12	1280	1440		
			CL=2	t _{RC} = ∞ t _{CK} =15 ns	-10	2080	2340		
				t _{RC} = ∞ t _{CK} =18 ns	-12	1840	2070		
			CL=3	t _{RC} = ∞ t _{CK} =10 ns	-10	2800	3150		
				t _{RC} = ∞ t _{CK} =12 ns	-12	2400	2700		
I _{CCA}	Serial PD Device Active Power Supply Current	SCL Clock Frequency = 100kHz				1.0	1.0	mA	4

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQ's are changed no more than once during $t_{CK}(\text{min})$.
3. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
4. Input pulse levels $V_{DD} \times 0.1$ to $V_{DD} \times 0.9$, input rise and fall times 10ns, input and output timing levels $V_{DD} \times 0.5$, output load 1 TTL gate and CL = 100pf.

AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

1. An initial pause of $100\mu\text{s}$ is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have $V_{IL} = 0.8\text{V}$ and $V_{IH} = 2.0\text{V}$ with the timing referenced to the 1.40V crossover point.



3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume $t_T = 1\text{ns}$.
5. In addition to meeting the transition rate specification, the clock and CKEn must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Note: All AC timing information below refers to the timings at the SDRAM devices. DIMM level XTK/IBIS models are available to perform system level modeling and timing analysis.

Clock and Clock Enable Parameters

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 3	10	100MHz	12	83MHz	ns	
t_{CK2}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 2	15	66MHz	18	56MHz	ns	
t_{CK1}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 1	30	33MHz	36	28MHz	ns	
t_{AC3}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 3	—	8	—	9	ns	1, 2
t_{AC2}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 2	—	9	—	10	ns	1, 2
t_{AC1}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 1	—	27	—	27	ns	1, 2
t_{CKH}	Clock High Pulse Width	3.5	—	4	—	ns	3
t_{CKL}	Clock Low Pulse Width	3.5	—	4	—	ns	3
t_{CES}	Clock Enable Set-up Time	3	—	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	1	—	ns	
t_{CESP}	CKE Set-up Time (Power down mode)	3	—	3	—	ns	
t_{T}	Transition Time (Rise and Fall)	1	30	1	30	ns	

1. Access time is measured at 1.4V . See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns . If clock rise time is longer than 1ns , then $(\text{trise}/2 - 0.5)\text{ns}$ should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns . If rise or fall time exceeds 1ns , then other AC parameters under consideration should be compensated by an additional $[(\text{trise} + \text{tfall})/2 - 1]\text{ns}$.



PRELIMINARY

IBM13N4649CC
IBM13N4739CC
4M x 64/72 1 Bank Unbuffered SDRAM Module

Common Parameters

Symbol	Parameter	-10		-12		Units
		Min.	Max.	Min.	Max.	
t_{CS}	Command Setup Time	3	—	3	—	ns
t_{CH}	Command Hold Time	1	—	1	—	ns
t_{AS}	Address and Bank Select Set-up Time	3	—	3	—	ns
t_{AH}	Address and Bank Select Hold Time	1	—	1	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	36	—	ns
t_{RC}	Bank Cycle Time	75	120000	96	120000	ns
t_{RAS}	Active Command Period	45	120000	60	120000	ns
t_{RP}	Precharge Time	30	—	36	—	ns
t_{RRD}	Bank to Bank Delay Time	20	—	24	—	ns
t_{CCD}	CAS to $\overline{CAS}$ Delay Time (Same Bank)	1	—	1	—	CLK

Refresh Cycle

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{SREX}	Self Refresh Exit Time	$2CLK + t_{RC}$	—	$2CLK + t_{RC}$	—	ns	3
t_{REF}	Refresh Period	—	64	—	64	ms	1, 2

1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
3. Self Refresh Exit is a synchronous operation and begins on the 2nd positive clock edge after CKE returns high. Self Refresh Exit is not complete until a time period equal to t_{RC} is satisfied once the Self Refresh Exit command is registered.

Read Cycle

Symbol	Parameter	-10		-12		Units	Notes
		Min.	Max.	Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	3	—	3	—	ns	
t_{HZ3}	Data Out to High Impedance Time, CL= 3	3	8	3	8	ns	1
t_{HZ2}	Data Out to High Impedance Time, CL= 2	3	8	3	10	ns	1
t_{HZ1}	Data Out to High Impedance Time, CL= 1	3	15	3	18	ns	1
t_{DOZ}	DQM Data Out Disable Latency	2	—	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	-10		-12		Units
		Min.	Max.	Min.	Max.	
t_{DS}	Data In Set-up Time	3	—	3	—	ns
t_{DH}	Data In Hold Time	1	—	1	—	ns
t_{DPL}	Data input to Precharge	15	—	15	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	0	—	CLK

Clock Frequency and Latency

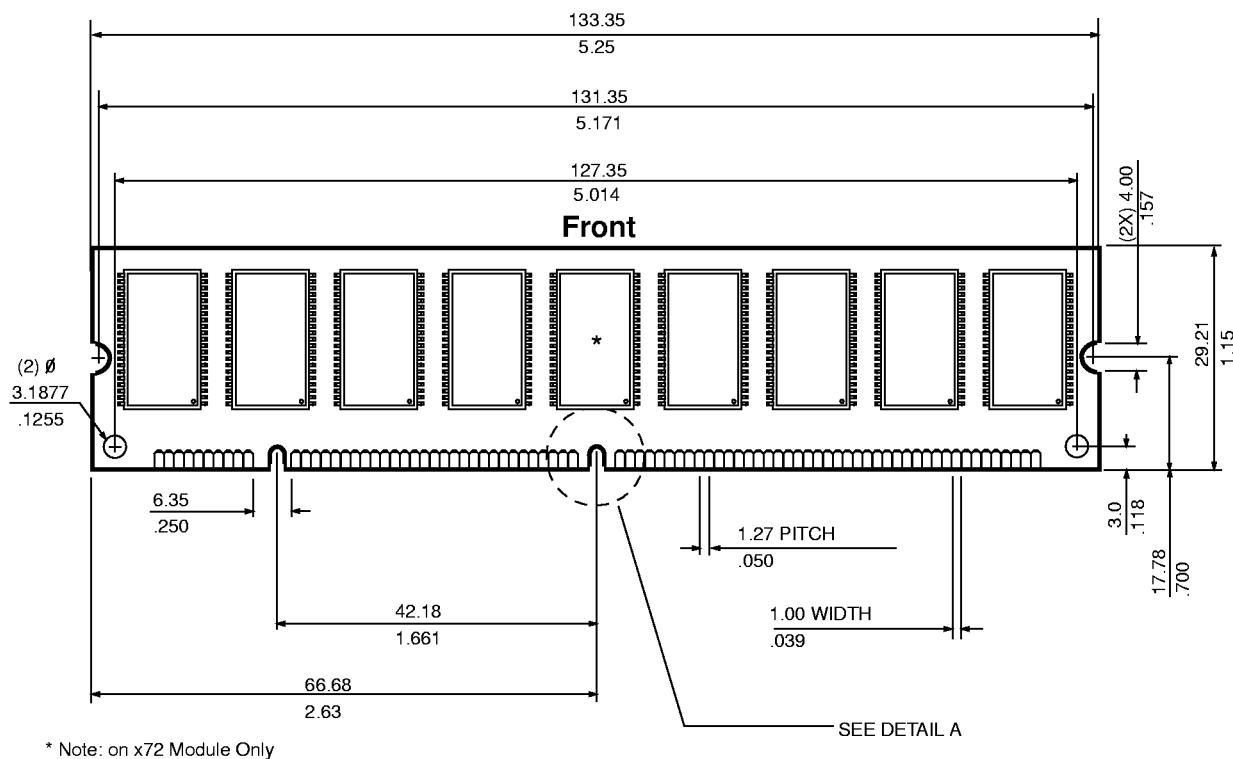
Symbol	Parameter	Speed Sort						Units
		-10			-12			
f _{CK}	Clock Frequency	100	66	33	83	56	28	MHz
t _{CK}	Clock Cycle Time	10	15	30	12	18	36	ns
t _{AA}	CAS Latency	3	2	1	3	2	1	CLK
t _{RCD}	RAS to CAS Delay	3	2	1	3	2	1	CLK
t _{RL}	RAS Latency	6	4	2	6	4	2	CLK
t _{RC}	Bank Cycle Time	8	5	3	8	5	3	CLK
t _{RAS}	Minimum Bank Active Time	5	3	2	5	3	2	CLK
t _{RP}	Precharge Time	3	2	1	3	2	1	CLK
t _{DPL}	Data In to Precharge	2	1	1	2	1	1	CLK
t _{DAL}	Data In to Active/Refresh	5	3	2	5	3	2	CLK
t _{RRD}	Bank to Bank Delay Time	2	2	1	2	2	1	CLK
t _{CCD}	CAS to CAS Delay Time	1	1	1	1	1	1	CLK
t _{WL}	Write Latency	0	0	0	0	0	0	CLK
t _{DQW}	DQM Write Mask Latency	0	0	0	0	0	0	CLK
t _{DQZ}	DQM Data Disable Latency	2	2	2	2	2	2	CLK
t _{CSL}	Clock Suspend Latency	1	1	1	1	1	1	CLK

Functional Description and Timing Diagrams

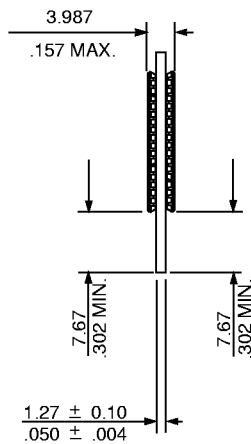
Refer to the IBM 16Mb Synchronous DRAM data sheet, document SA14-4711-04 (Revised 10/96), for the functional description and timing diagrams for SDRAM operation.

Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

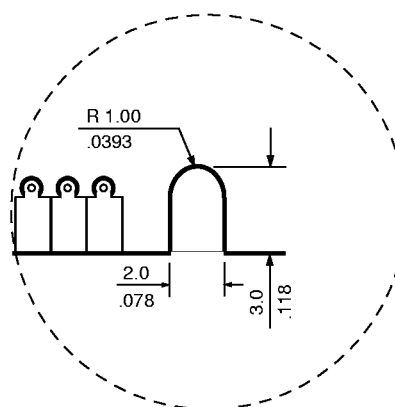
Layout Drawing



Side



Detail A SCALE 4/1



Note: All dimensions are typical unless otherwise stated.

Millimeters
Inches