8M x 72 2 Bank Unbuffered SDRAM Module

Features

- 168-Pin Unbuffered 8-Byte Dual In-Line Memory Module
- 8Mx72 Synchronous DRAM DIMM
- Performance:

		10	Units
	$\overline{CAS}$ Latency	3	
f_{CK}	Clock Frequency	100	MHz
t_{CK}	Clock Cycle	10	ns
t_{AC}	Clock Access Time	8	ns

- All inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- Single Pulsed $\overline{RAS}$ interface
- SDRAMs have 2 internal banks
- Module has 2 banks
- Fully Synchronous to positive Clock Edge
- Programmable Operation:
  - CAS Latency: 1, 2, 3
  - Burst Type: Sequential or Interleave
  - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  - Operation: Burst Read and Write, or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge commands
- Suspend Mode and Power Down Mode
- 11/10/1 Addressing (Row/Column/Bank)
- 4096 Refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 5.25" x 1.15" x 0.320"
- Gold contacts
- SDRAMs in stacked TSOJ Package

Description

IBM13N8739CC is an unbuffered 168-pin Synchronous DRAM Dual In-Line Memory Module (DIMM) which is organized as an 8Mx72 high-speed memory array. The DIMM uses 8Mx4 SDRAM stacks in 400mil TSOJ packages. The 8Mx4 stack consists of two 4Mx4 SDRAM devices in a two-high stack configuration.

The DIMMs achieve high-speed data-transfer rates of up to 83MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

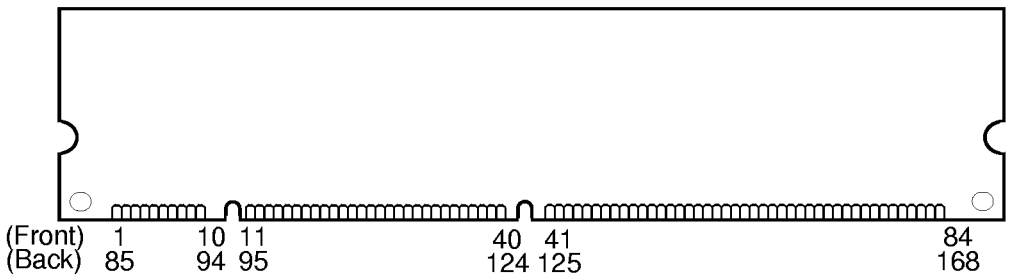
All inputs are sampled at the positive edge of each externally supplied clock (CK0 - CK3). Internal operating modes are defined by combinations of the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$ - $\overline{S3}$, DQMB, and CKE - CKE1 signals. A command decoder initiates the necessary timings for each operation. A 12-bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 168-pin DIMMs provide a high performance, flexible 8-byte interface in a 5.25" long space-saving footprint. Related products include both EDO DRAM and SDRAM unbuffered DIMMs in both non-parity x64 and ECC-Optimized x72 configurations.

Card Outline



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Pin Description

CK0 - CK3	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0 - CKE1	Clock Enables	CB0 - CB7	Check Bit Data Input/Output
$\overline{RAS}$	Row Address Strobe	DQMB0 - DQMB7	Data Mask
$\overline{CAS}$	Column Address Strobe	V_{DD}	Power (3.3V)
$\overline{WE}$	Write Enable	V_{SS}	Ground
$\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$	Chip Selects	NC	No Connect
A0 - A9	Address Inputs	SCL	Serial Presence Detect Clock Input
A10/AP	Address Input/Autoprecharge	SDA	Serial Presence Detect Data Input/Output
BA0	SDRAM Bank Address Input	SA0-2	Serial Presence Detect Address Inputs

Pinout

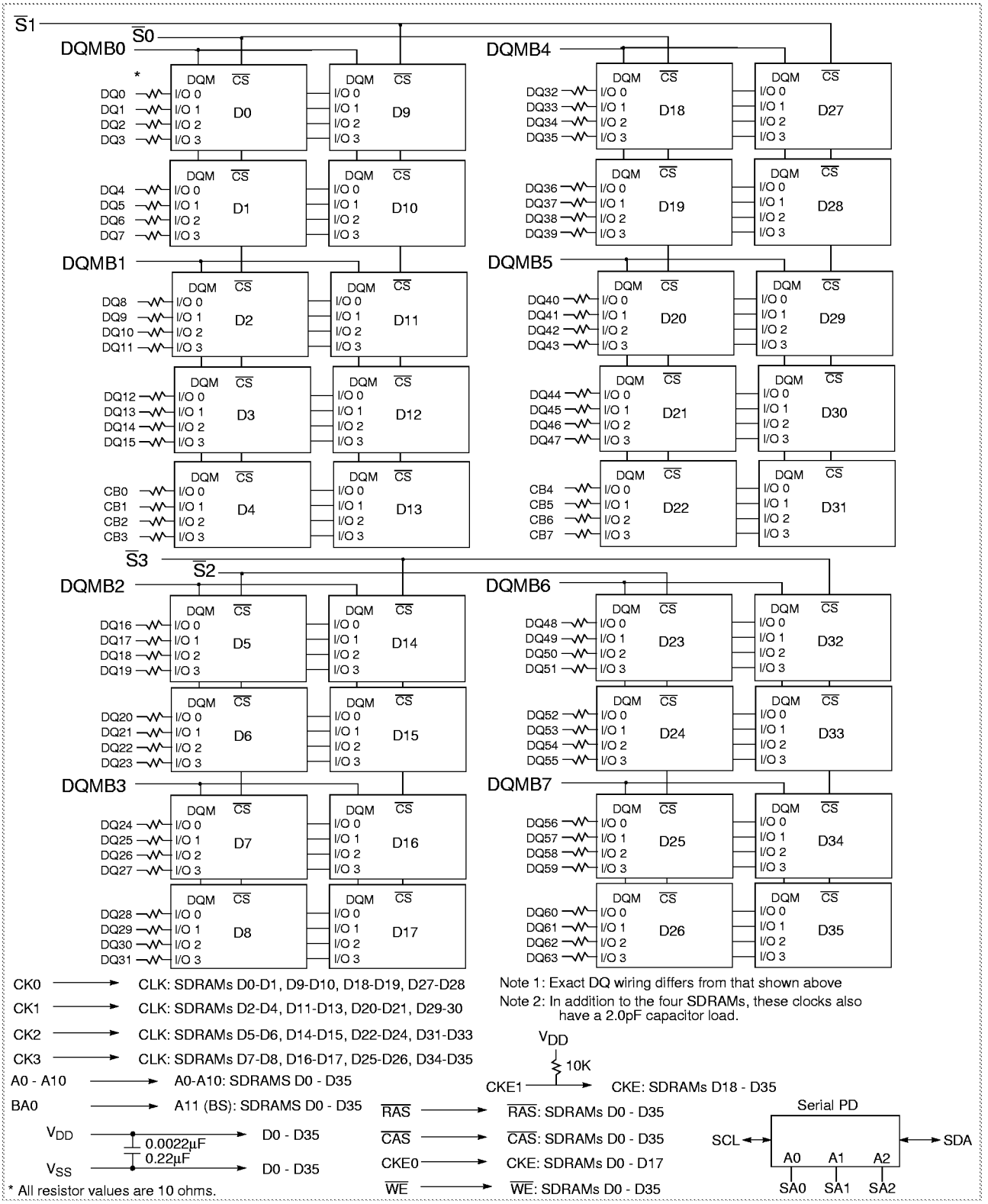
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	85	V_{SS}	22	CB1	106	CB5	43	V_{SS}	127	V_{SS}	64	V_{SS}	148	V_{SS}
2	DQ0	86	DQ32	23	V_{SS}	107	V_{SS}	44	NC	128	CKE0	65	DQ21	149	DQ53
3	DQ1	87	DQ33	24	NC	108	NC	45	$\overline{S2}$	129	$\overline{S3}$	66	DQ22	150	DQ54
4	DQ2	88	DQ34	25	NC	109	NC	46	DQMB2	130	DQMB6	67	DQ23	151	DQ55
5	DQ3	89	DQ35	26	V_{DD}	110	V_{DD}	47	DQMB3	131	DQMB7	68	V_{SS}	152	V_{SS}
6	V_{DD}	90	V_{DD}	27	$\overline{WE}$	111	$\overline{CAS}$	48	NC	132	NC	69	DQ24	153	DQ56
7	DQ4	91	DQ36	28	DQMB0	112	DQMB4	49	V_{DD}	133	V_{DD}	70	DQ25	154	DQ57
8	DQ5	92	DQ37	29	DQMB1	113	DQMB5	50	NC	134	NC	71	DQ26	155	DQ58
9	DQ6	93	DQ38	30	$\overline{S0}$	114	$\overline{S1}$	51	NC	135	NC	72	DQ27	156	DQ59
10	DQ7	94	DQ39	31	NC	115	$\overline{RAS}$	52	CB2	136	CB6	73	V_{DD}	157	V_{DD}
11	DQ8	95	DQ40	32	V_{SS}	116	V_{SS}	53	CB3	137	CB7	74	DQ28	158	DQ60
12	V_{SS}	96	V_{SS}	33	A0	117	A1	54	V_{SS}	138	V_{SS}	75	DQ29	159	DQ61
13	DQ9	97	DQ41	34	A2	118	A3	55	DQ16	139	DQ48	76	DQ30	160	DQ62
14	DQ10	98	DQ42	35	A4	119	A5	56	DQ17	140	DQ49	77	DQ31	161	DQ63
15	DQ11	99	DQ43	36	A6	120	A7	57	DQ18	141	DQ50	78	V_{SS}	162	V_{SS}
16	DQ12	100	DQ44	37	A8	121	A9	58	DQ19	142	DQ51	79	CK2	163	CK3
17	DQ13	101	DQ45	38	A10/AP	122	BA0	59	V_{DD}	143	V_{DD}	80	NC	164	NC
18	V_{DD}	102	V_{DD}	39	NC	123	NC	60	DQ20	144	DQ52	81	NC	165	SA0
19	DQ14	103	DQ46	40	V_{DD}	124	V_{DD}	61	NC	145	NC	82	SDA	166	SA1
20	DQ15	104	DQ47	41	V_{DD}	125	CK1	62	NC	146	NC	83	SCL	167	SA2
21	CB0	105	CB4	42	CK0	126	NC	63	*CKE1	147	NC	84	V_{DD}	168	V_{DD}

Note: All pin assignments are consistent for all 8-byte unbuffered versions. *CKE1 is terminated with a 10K ohm pullup resistor.

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13N8739CC-10Y	8Mx72	10ns	Gold	5.25" x 1.15" x 0.320"	3.3V

8Mx72 SDRAM DIMM Block Diagram (2 Bank, 8Mx4 SDRAMs)



Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0 - CK3	Input	Pulse	Positive Edge	The system clock inputs. All the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0, CKE1	Input	Level	Active High	Activates the associated SDRAM CLK signals when high and deactivates them when low. By deactivating the clocks, CKE0/CKE1 low initiates the Power Down mode, the Suspend mode, or the Self Refresh mode.
$\overline{S0}$ - $\overline{S3}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$ $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A9 defines the column address (CA0-CA9) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke Autoprecharge operation at the end of the Burst Read or Write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regardless of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63, CB0 - CB7	Input Output	Level	—	Data and Check Bit Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocking the Write operation if it is high.
SA0 - SA2	Input	Level	—	Address inputs. Connected to either V_{DD} or V_{SS} on the system board to configure the Serial Presence Detect EEPROM address.
SDA	Input Output	Level	—	Serial Data. Bidirectional signal used to transfer data into and out of the Serial Presence Detect EEPROM. Since the SDA signal is Open Drain/Open Collector at the EEPROM, a pullup resistor is required on the system board.
SCL	Input	Pulse	—	Serial Clock. Used to clock all Serial Presence Detect data into and out of the EEPROM. Since the SCL signal is inactive in the “high” state, a pullup resistor is recommended on the system board.
V_{DD}, V_{SS}	Supply			Power and ground for the module.

Serial Presence Detect

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	11	0B	
4	Number of Column Addresses on Assembly	10	0A	
5	Number of DIMM Banks	2	02	
6 - 7	Data Width of Assembly	x72	4800	
8	Voltage Interface Level of this Assembly	LVTTL	01	
9	SDRAM Device Cycle Time at CL=3	10.0ns	A0	
10	SDRAM Device Access Time from Clock at CL=3	8.0ns	80	1
11	DIMM Configuration Type	ECC	02	
12	Refresh Rate/Type	SR/1x(15.625us)	80	
13	Primary SDRAM Device Width	x4	04	
14	Error Checking SDRAM Device Width	x4	04	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	2	02	
18	SDRAM Device Attributes: $\overline{CAS}$ Latencies Supported	1, 2, 3	07	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	Unbuffered	00	
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Precharge All, Auto-Precharge, V_{DD} +/- 10%	0E	
23	Minimum Clock Cycle at CL=2	15.0ns	F0	
24	Maximum Data Access Time (t_{AC}) from Clock at CL=2	9.0ns	90	1
25	Minimum Clock Cycle Time at CL=1	30.0ns	78	
26	Maximum Data Access Time (t_{AC}) from Clock at CL=1	27.0ns	6C	1
27	Minimum Row Precharge Time (t_{RP})	30ns	1E	
28	Minimum Row Active to Row Active delay (t_{RRD})	20ns	14	
29	Minimum $\overline{RAS}$ to $\overline{CAS}$ delay (t_{RCD})	30ns	1E	
30	Minimum $\overline{RAS}$ Pulse width (t_{RAS})	60ns	3C	
31	Module Bank Density	32MB	08	
32 - 61	Reserved	Undefined	00	
62	SPD Revision	01	01	
63	Checksum for bytes 0 - 62	Checksum Data	cc	2
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	
73 - 90	Module Part Number	ASCII '13N8739CC"R"-10T'	31334E383733394343rr2D3 1305420202020	3, 4
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	5, 6
95 - 98	Module Serial Number	Serial Number	ssssssss	7
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	66 MHz	66	
127	$\overline{CAS}$ Latencies Supported for Clock Frequency defined in byte 126	2, 3	06	
128 - 255	Open for Customer Use	Undefined	00	

1. See the AC output load circuit in the AC Characteristics section below
2. cc = Checksum Data byte, 00-FF (Hex)
3. "R" = Alphanumeric revision code, A-Z, 0-9
4. rr = ASCII coded revision code byte "R"
5. yy = Binary coded decimal year code, 00-99 (Decimal) 00-63 (Hex)
6. ww = Binary coded decimal week code, 01-52 (Decimal) 01-34 (Hex)
7. ss = Serial number data byte, 00-FF (Hex)

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
V_{OUT}	Output Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T_A	Operating Temperature (Ambient)		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation		36.0	W	1
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions (T_A= 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{DD} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS}.

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Max.	Units
C_{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	140	pF
C_{I2}	Input Capacitance (CKE0 - CKE1)	80	pF
C_{I3}	Input Capacitance ($\overline{S0}$ - $\overline{S3}$)	55	pF
C_{I4}	Input Capacitance (CK0 - CK3)	70	pF
C_{I5}	Input Capacitance (DQMB0 - DQMB7)	30	pF
C_{I6}	Input Capacitance (SA0 - SA2, SCL)	9	pF
C_{IO1}	Input/Output Capacitance (DQ0 - DQ63, CB0 - CB7)	15	pF
C_{IO2}	Input/Output Capacitance (SDA)	11	pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter		x72		Units
			Min.	Max.	
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V); All Other Pins Not Under Test = 0V	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, A0-A9, A10/AP, BA0	-36	+36	µA
		CK0, CK3	-8	+8	
		CK1, CK2	-10	+10	
		CKE0, CKE1	-18	+18	
		$\overline{S0}$, $\overline{S1}$	-10	+10	
		$\overline{S2}$, $\overline{S3}$	-8	+8	
		DQMB1, 5	-6	+6	
		DQMB0, 2, 3, 4, 6, 7	-4	+4	
		DQ0 - 63, CB0 - 7	-2	+2	
		SA0, SA1, SA2, SCL, SDA	-1	+1	
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	DQ0 - 63, CB0 - 7	-2	+2	µA
		SDA	-1	+1	
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2.0mA)		2.4	V_{DD}	V
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = +2.0mA)		0.0	0.4	

Standby and Refresh Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Parameter	Symbol	Test Condition	Organization	Units	Notes
Precharge Standby Current in Power Down Mode	ICC_1P	CKE0, 1 ≤ V_{IL}(max), t_{CK} = 15ns	108	mA	1
	ICC_1PS	CKE0, 1 ≤ V_{IL}(max), t_{CK} = Infinity	72	mA	1
Precharge Standby Current in Non-Power Down Mode	ICC_1N	CKE0, 1 ≥ V_{IH}(min), t_{CK} = 15ns, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$ ≥ V_{IH}(min) Input Change every 30ns	900	mA	1
	ICC_1NS	CKE0, 1 ≥ V_{IH}(min), t_{CK} = Infinity No Input Change	360	mA	1
Active Standby Current in Power Down Mode	ICC_2P	CKE0, 1 ≤ V_{IL}(max), t_{CK} = 15ns	108	mA	1, 2
	ICC_2PS	CKE0, 1 ≤ V_{IL}(max), t_{CK} = Infinity	72	mA	1, 2
Active Standby Current in Non-Power Down Mode	ICC_2N	CKE0, 1 ≥ V_{IH}(min), t_{CK} = 15ns, $\overline{S0}$, $\overline{S1}$, $\overline{S2}$, $\overline{S3}$ ≥ V_{IH}(min) Input Change every 30ns	900	mA	1
	ICC_2NS	CKE0, 1 ≥ V_{IH}(min), t_{CK} = Infinity No Input Change	540	mA	1
Auto (CBR) Refresh Current	ICC_3	$\overline{CAS}$ Latency = 1 t_{RC} ≥ t_{RC}(min)	1980	mA	3, 4, 5, 6
		$\overline{CAS}$ Latency = 2 t_{RC} ≥ t_{RC}(min)	2070	mA	
		$\overline{CAS}$ Latency = 3 t_{RC} ≥ t_{RC}(min)	2430	mA	
Self Refresh Current	ICC_4	CKE0, 1 ≤ 0.2V	72	mA	1
Serial PD Device Standby Current	I_{SB}	V_{IN} = GND or V_{DD}	10	µA	7

1. The specified values are for both DIMM banks operating in the specified mode.
2. Active Standby current will be higher if Clock Suspend is entered during a Burst Read cycle (add 1ma per DQ).
3. The specified values are valid when addresses are changed no more than once during t_{CK}(min).
4. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).
5. The specified values are valid when data inputs (DQs) are stable during t_{RC}(min).
6. The specified values are for one DIMM bank in Auto (CBR) Refresh and the other DIMM bank in Precharge Standby (ICC_1N).
7. V_{DD} = 3.3V

Operating Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Organization x72	Units	Notes
I_{CC5}	Operating Current Burst Length = 1	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	90 ns	2160	mA	1, 2, 3
			CL=2	90 ns	2340		
			CL=3	90 ns	2700		
I_{CC6}	Operating Current Burst Length = 2	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	120 ns	1800	mA	1, 2, 3, 4
			CL=2	105 ns	2250		
			CL=3	100 ns	2700		
I_{CC7}	Operating Current Burst Length = 4	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	180 ns	1620	mA	1, 2, 3, 4
			CL=2	135 ns	2070		
			CL=3	120 ns	2610		
I_{CC8}	Operating Current Burst Length = 8	$t_{RC} = t_{RC}$(min) $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	300 ns	1440	mA	1, 2, 3, 4
			CL=2	195 ns	1980		
			CL=3	160 ns	2610		
I_{CC9}	Operating Current Burst Length = Full Page	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	$t_{RC} = \infty$ $t_{CK=30\ ns}$	1170	mA	1, 2, 3, 4
			CL=2	$t_{RC} = \infty$ $t_{CK=15\ ns}$	1710		
			CL=3	$t_{RC} = \infty$ $t_{CK=10\ ns}$	2250		
I_{CC10}	Operating Current 1N Rule (Continuous Read/Write cycles with new column address registered each clock cycle)	t_{RC} = Infinity $t_{CK} \geq t_{CK}$(min) I_O = 0mA	CL=1	$t_{RC} = \infty$ $t_{CK=30\ ns}$	1980	mA	1, 2, 3
			CL=2	$t_{RC} = \infty$ $t_{CK=15\ ns}$	2790		
			CL=3	$t_{RC} = \infty$ $t_{CK=10\ ns}$	3600		
I_{CCA}	Serial PD Device Active Power Supply Current	SCL Clock Frequency = 100kHz			1.0	mA	5

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQs are changed no more than once during t_{CK}(min).
3. The specified values are for one DIMM bank in Operating Mode and the other DIMM bank in Active Standby (ICC2N).
4. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
5. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL = 100pf.

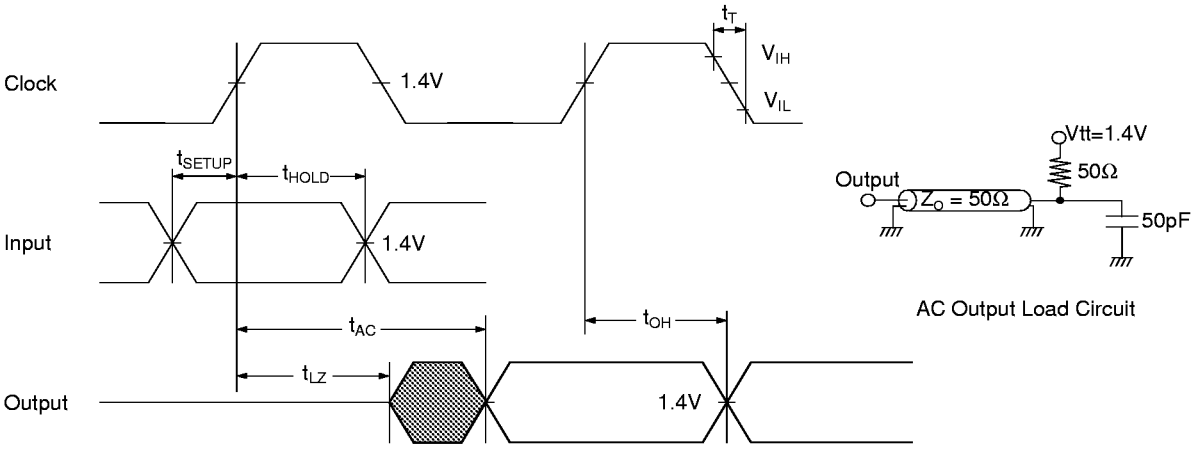
Operating Currents (T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	t_{RC}(min)	Organization x72	Units	Notes

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQs are changed no more than once during t_{CK}(min).
3. The specified values are for one DIMM bank in Operating Mode and the other DIMM bank in Active Standby (ICC2N).
4. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
5. Input pulse levels V_{DD} x 0.1 to V_{DD} x 0.9, input rise and fall times 10ns, input and output timing levels V_{DD} x 0.5, output load 1 TTL gate and CL = 100pf.

AC Characteristics T_A= 0 to +70°C, V_{DD}= 3.3V ± 0.3V

1. An initial pause of 100µs is required after power-up, then a Precharge All Banks command must be given, followed by a minimum of two Auto (CBR) Refresh cycles, before the Mode Register Set operation can begin.
2. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with the timing referenced to the 1.40V crossover point.



3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume t_T=1ns.
5. In addition to meeting the transition rate specification, the clock and CKE0, 1 must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Clock and Clock Enable Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
t_{CK3}	Clock Cycle Time, $\overline{CAS}$ Latency = 3	10	100 MHz	ns	
t_{CK2}	Clock Cycle Time, $\overline{CAS}$ Latency = 2	15	66 MHz	ns	
t_{CK1}	Clock Cycle Time, $\overline{CAS}$ Latency = 1	30	33 MHz	ns	
t_{AC3}	Clock Access Time, $\overline{CAS}$ Latency = 3	—	8	ns	1, 2

1. Access time is measured at 1.4V. See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then (t_{RISE}/2-0.5)ns should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional [(t_{RISE}+t_{FALL})/2-1]ns.

Clock and Clock Enable Parameters

Symbol	Parameter	Min.	Max.	Units	Notes
t_{AC2}	Clock Access Time, $\overline{CAS}$ Latency = 2	—	9	ns	1, 2
t_{AC1}	Clock Access Time, $\overline{CAS}$ Latency = 1	—	27	ns	1, 2
t_{CKH}	Clock High Pulse Width	3.5	—	ns	3
t_{CKL}	Clock Low Pulse Width	3.5	—	ns	3
t_{CES}	Clock Enable Set-up Time	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	ns	
t_{CESP}	CKE Set-up Time (Power down mode)	3	—	ns	
t_T	Transition Time (Rise and Fall)	1	30	ns	

1. Access time is measured at 1.4V. See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then (t_{RISE}/2-0.5)ns should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional [(t_{RISE}+t_{FALL})/2-1]ns.

Common Parameters

Symbol	Parameter	Min.	Max.	Units
t_{CS}	Command Setup Time	3	—	ns
t_{CH}	Command Hold Time	1	—	ns
t_{AS}	Address and Bank Select Set-up Time	3	—	ns
t_{AH}	Address and Bank Select Hold Time	1	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	ns
t_{RC}	Bank Cycle Time	90	120k	ns
t_{RAS}	Active Command Period	60	120k	ns
t_{RP}	Precharge Time	30	—	ns
t_{RRD}	Bank to Bank Delay Time	20	—	ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	1	—	CLK

Refresh Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
t_{REF}	Refresh Period	—	64	ms	1, 2
t_{SREX}	Self Refresh Exit Time	$10ns+t_{RC}$	—	ns	3

1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.
3. Self Refresh Exit is an asynchronous operation. Self Refresh Exit is accomplished by starting the clock (CK0 - CK3) and then asserting CKE0/CKE1 high. During the exit time (t_{SREX}), no commands may be issued until t_{RC} is satisfied and CKE0/CKE1 must remain high. It is recommended to hold $\overline{S0}$, $\overline{S2}/\overline{S1}$, $\overline{S3}$ high during the self-refresh exit time, but NOP commands may be issued with each rising clock edge during this period as an alternative. To prevent erroneous exit of Self Refresh operation, a glitch-suppressor circuit is incorporated into the CKE0/CKE1 receiver. If CKE0/CKE1 is asserted high (system noise) for less than 10ns (approximately), the device will not exit Self Refresh operation.

Read Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
t_{OH}	Data Out Hold Time	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	3	—	ns	
t_{HZ3}	Data Out to High Impedance Time, CL= 3	3	8	ns	1
t_{HZ2}	Data Out to High Impedance Time, CL= 2	3	8	ns	1
t_{HZ1}	Data Out to High Impedance Time, CL= 1	3	15	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	Min.	Max.	Units
t_{DS}	Data In Set-up Time	3	—	ns
t_{DH}	Data In Hold Time	1	—	ns
t_{DPL}	Data input to Precharge	10	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	CLK

Clock Frequency and Latency

Symbol	Parameter	-10			Units
f_{CK}	Clock Frequency	100	66	33	MHz
t_{CK}	Clock Cycle Time	10	15	30	ns
t_{AA}	$\overline{CAS}$ Latency	3	2	1	CLK
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	3	2	1	CLK
t_{RL}	$\overline{RAS}$ Latency	6	4	2	CLK
t_{RC}	Bank Cycle Time	9	6	3	CLK
t_{RAS}	Minimum Bank Active Time	6	4	2	CLK
t_{RP}	Precharge Time	3	2	1	CLK
t_{DPL}	Data In to Precharge	1	1	1	CLK
t_{DAL}	Data In to Active/Refresh	4	3	2	CLK
t_{RRD}	Bank to Bank Delay Time	2	2	1	CLK
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time	1	1	1	CLK
t_{WL}	Write Latency	0	0	0	CLK
t_{DQW}	DQM Write Mask Latency	0	0	0	CLK
t_{DQZ}	DQM Data Disable Latency	2	2	2	CLK
t_{CSL}	Clock Suspend Latency	1	1	1	CLK

Presence Detect Read and Write Cycle

Symbol	Parameter	Min.	Max.	Units	Notes
f_{SCL}	SCL Clock Frequency		100	kHZ	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs		100	ns	
t_{AA}	SCL Low to SDA Data Out Valid	0.3	3.5	µs	
t_{BUF}	Time the Bus Must Be Free before a New Transmission Can Start	4.7		µs	
$t_{HD:STA}$	Start Condition Hold Time	4.0		µs	
t_{LOW}	Clock Low Period	4.7		µs	
t_{HIGH}	Clock High Period	4.0		µs	
$t_{SU:STA}$	Start Condition Setup Time (for a Repeated Start Condition)	4.7		µs	
$t_{HD:DAT}$	Data in Hold Time	0		µs	
$t_{SU:DAT}$	Data in Setup Time	250		ns	
t_r	SDA and SCL Rise Time		1	µs	
t_f	SDA and SCL Fall Time		300	ns	
$t_{SU:STO}$	Stop Condition Setup Time	4.7		µs	
t_{DH}	Data Out Hold Time	300		ns	
t_{WR}	Write Cycle Time		15	ms	1

1. The Write cycle time (t_{WR}) is the time from a valid stop condition of a write sequence to the end of the internal Erase/Program cycle. During the Write cycle, the bus interface circuits are disabled, SDA is allowed to remain high per the bus-level pullup resistor, and the device does not respond to its slave address.

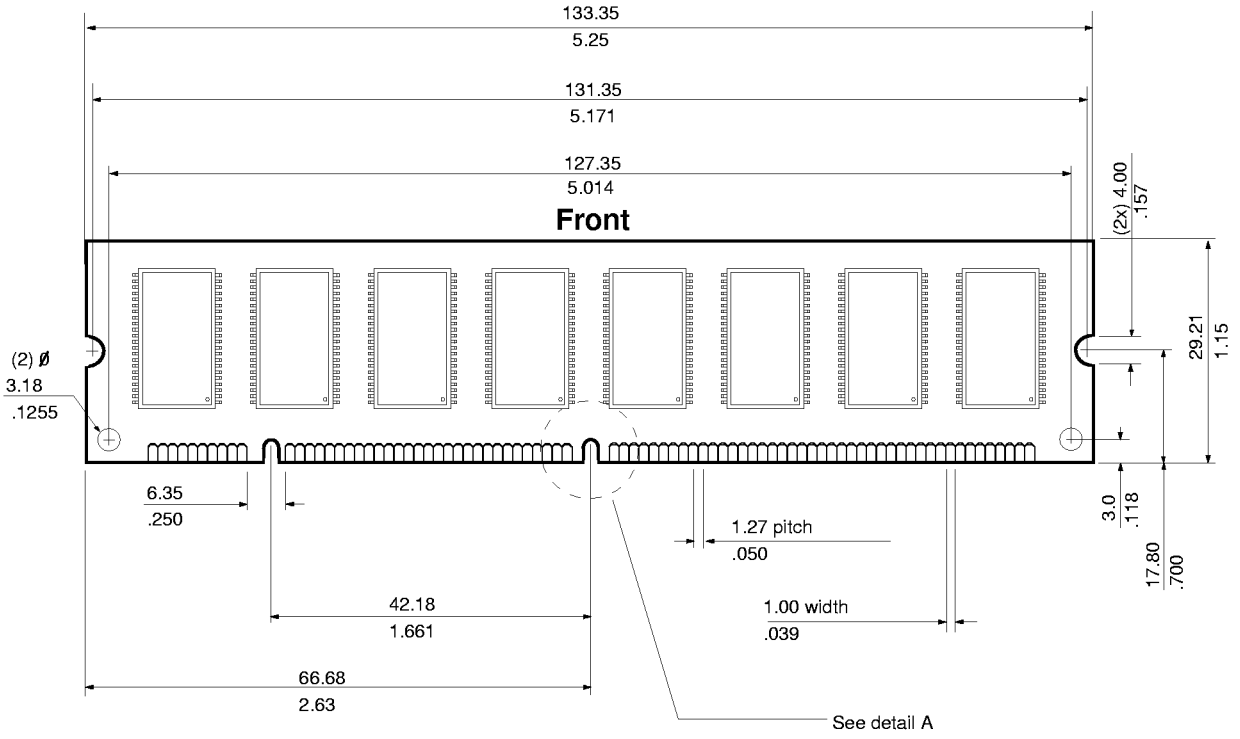
Functional Description and Timing Diagrams

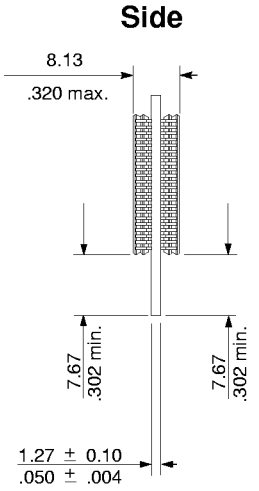
Refer to the IBM 16Mb Synchronous DRAM data sheet, document 08J0511.E35853 (Revised 5/98), for the functional description and timing diagrams for SDRAM operation.

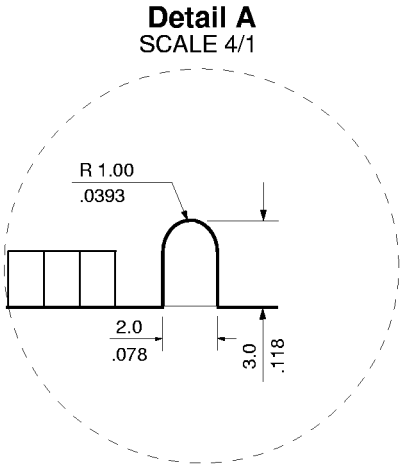
Refer to the IBM Application Notes *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.

Layout Drawing







Note: All dimensions are typical unless otherwise stated. Millimeters / Inches

Revision Log

Rev	Contents of Modification
4/98	Initial release
8/98	Updated Capacitance table to relfect current change on C_{13} from 50 to 55.

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