

Features

- 144 Pin (emerging) JEDEC Standard, 8 Byte Small Outline Dual-In-line Memory Module
- 2Mx64 Synchronous DRAM SO DIMM
- Performance:

		10	Units
	CAS Latency	3	
f _{CK}	Clock Frequency	100	MHz
t _{CK}	Clock Cycle	10	ns
t _{AC}	Clock Access Time	8	ns

- All inputs and outputs are LVTTTL (3.3V) compatible
- Single 3.3V $\pm$ 0.3V Power Supply
- Single Pulsed RAS interface
- SDRAMs have 2 internal banks
- Module has 1 bank
- Fully Synchronous to positive Clock Edge

- Programmable Operation:
 - CAS Latency: 1, 2, 3
 - Burst Type: Sequential or Interleave
 - Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
 - Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Data Mask for Byte Read/Write control
- Auto Refresh (CBR) and Self Refresh
- Automatic and controlled Precharge Commands
- Suspend Mode and Power Down Mode
- 11/9/1 Addressing (Row/Column/Bank)
- 4096 refresh cycles distributed across 64ms
- Serial Presence Detect
- Card size: 2.66" x 1.0" x 0.149"
- Au contacts
- SDRAMs in TSOP Type II Package

Description

IBM13T2649JC is a 144-pin Synchronous DRAM Small Outline Dual In-line Memory Module (SO DIMM) which is organized as a 2Mx64 high-speed memory array. The SO DIMM uses 8 2Mx8 SDRAMs in 400mil TSOP II packages. It achieves high speed data transfer rates of up to 100MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power.

The SO DIMM is intended to comply with all JEDEC standards set for 144 pin SDRAM SO DIMMs.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations of the RAS, CAS, WE, S0, DQMB, and CKE0 signals. A

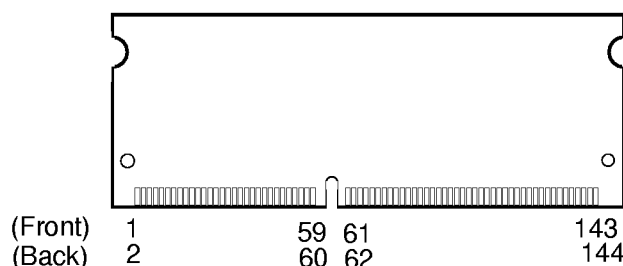
command decoder initiates the necessary timings for each operation. A 12 bit address bus accepts address information in a row/column multiplexing arrangement.

Prior to any access operation, the CAS latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the Mode Register Set cycle.

The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two pin IIC protocol. The first 128 bytes of serial PD data are used by the DIMM manufacturer. The last 128 bytes are available to the customer.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.65" long space-saving footprint. Related products are in the EDO DRAM SO DIMM family.

Card Outline





IBM13T2649JC
2M x 64 SDRAM SO DIMM

Pin Description

CK0, CK1	Clock Inputs	DQ0 - DQ63	Data Input/Output
CKE0	Clock Enable	DQMB0 - DQMB7	Data Mask
RAS	Row Address Strobe	V _{DD}	Power (3.3V)
CAS	Column Address Strobe	V _{SS}	Ground
WE	Write Enable	NC	No Connect
S0	Chip Selects	SCL	Serial Presence Detect Clock Input
A0 - A9	Address Inputs	SDA	Serial Presence Detect Data Input/Output
A10 /AP	Address Input/Autoprecharge	SA0-2	Serial Presence Detect Address Inputs
BA0	SDRAM Bank Address		

Pinout

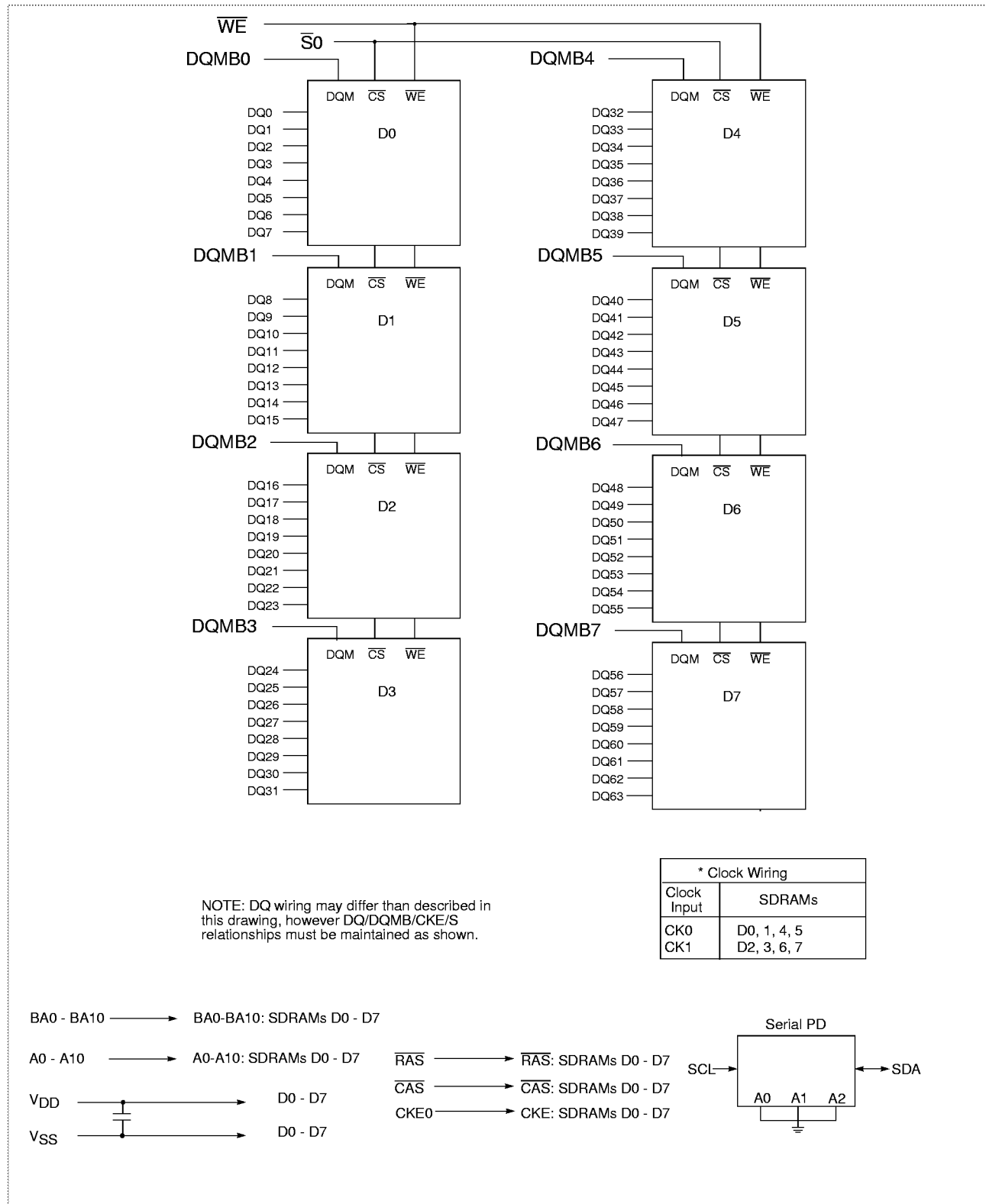
Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V _{SS}	2	V _{SS}	37	DQ8	38	DQ40	71	NC	72	NC	107	V _{SS}	108	V _{SS}
3	DQ0	4	DQ32	39	DQ9	40	DQ41	73	DU	74	CK1	109	A9	110	NC
5	DQ1	6	DQ33	41	DQ10	42	DQ42	75	V _{SS}	76	V _{SS}	111	A10/AP	112	NC
7	DQ2	8	DQ34	43	DQ11	44	DQ43	77	NC	78	NC	113	V _{DD}	114	V _{DD}
9	DQ3	10	DQ35	45	V _{DD}	46	V _{DD}	79	NC	80	NC	115	DQMB2	116	DQMB6
11	V _{DD}	12	V _{DD}	47	DQ12	48	DQ44	81	V _{DD}	82	V _{DD}	117	DQMB3	118	DQMB7
13	DQ4	14	DQ36	49	DQ13	50	DQ45	83	DQ16	84	DQ48	119	V _{SS}	120	V _{SS}
15	DQ5	16	DQ37	51	DQ14	52	DQ46	85	DQ17	86	DQ49	121	DQ24	122	DQ56
17	DQ6	18	DQ38	53	DQ15	54	DQ47	87	DQ18	88	DQ50	123	DQ25	124	DQ57
19	DQ7	20	DQ39	55	V _{SS}	56	V _{SS}	89	DQ19	90	DQ51	125	DQ26	126	DQ58
21	V _{SS}	22	V _{SS}	57	NC	58	NC	91	V _{SS}	92	V _{SS}	127	DQ27	128	DQ59
23	DQMB0	24	DQMB4	59	NC	60	NC	93	DQ20	94	DQ52	129	V _{DD}	130	V _{DD}
25	DQMB1	26	DQMB5	VOLTAGE KEY				95	DQ21	96	DQ53	131	DQ28	132	DQ60
27	V _{DD}	28	V _{DD}	61	CK0	62	CKE0	97	DQ22	98	DQ54	133	DQ29	134	DQ61
29	A0	30	A3	63	V _{DD}	64	V _{DD}	99	DQ23	100	DQ55	135	DQ30	136	DQ62
31	A1	32	A4	65	RAS	66	CAS	101	V _{DD}	102	V _{DD}	137	DQ31	138	DQ63
33	A2	34	A5	67	WE	68	NC	103	A6	104	A7	139	V _{SS}	140	V _{SS}
35	V _{SS}	36	V _{SS}	69	S0	70	NC	105	A8	106	BA0	141	SDA	142	SCL
												143	V _{DD}	144	V _{DD}

Note: All pin assignments are consistent for all 8 Byte versions.

Ordering Information

Part Number	Organization	Clock Cycle	Leads	Dimension	Power
IBM13T2649JC-10T	2Mx64	10ns	Au	2.66" x 1.0" x 0.149"	3.3V

2Mx64 SDRAM DIMM Block Diagram (x8 SDRAMs)



Input/Output Functional Description

Symbol	Type	Signal	Polarity	Function
CK0, CK1	Input	Pulse	Positive Edge	The system clock inputs. All of the SDRAM inputs are sampled on the rising edge of their associated clock.
CKE0	Input	Level	Active High	Activates the CK0 and CK1 signals when high and deactivates them when low. By deactivating the clocks, CKE0 low initiates the Power Down mode, Suspend mode, or the Self Refresh mode.
$\overline{S0}$	Input	Pulse	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{CAS}$, $\overline{RAS}$, and $\overline{WE}$ define the operation to be executed by the SDRAM.
BA0	Input	Level	—	Selects which SDRAM bank is to be active.
A0 - A9 A10/AP	Input	Level	—	During a Bank Activate command cycle, A0-A10 defines the row address (RA0-RA10) when sampled at the rising clock edge. During a Read or Write command cycle, A0-A8 defines the column address (CA0-CA8) when sampled at the rising clock edge. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0 defines the bank to be precharged (low=bank A, high=bank B). If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0 to control which bank(s) to precharge. If AP is high, both bank A and bank B will be precharged regardless of the state of BA0. If AP is low, then BA0 is used to define which bank to precharge.
DQ0 - DQ63	Input Output	Level	—	Data Input/Output pins operate in the same manner as on conventional DRAMs.
DQMB0 - DQMB7	Input	Pulse	Active High	The Data Input/Output mask places the DQ buffers in a high impedance state when sampled high. In Read mode, DQM has a latency of two clock cycles and controls the output buffers like an output enable. In Write mode, DQM has a latency of zero and operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if DQM is high.
VDD, VSS	Supply			Power and ground for the module.



Serial Presence Detect (Part 1 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
0	Number of Serial PD Bytes Written during Production	128	80	
1	Total Number of Bytes in Serial PD device	256	08	
2	Fundamental Memory Type	SDRAM	04	
3	Number of Row Addresses on Assembly	11	0B	
4	Number of Column Addresses on Assembly	9	09	
5	Number of DIMM Banks	1	01	
6 - 7	Data Width of Assembly	x64	4000	
8	Voltage Interface Level of this Assembly	LVTTL	01	
9	SDRAM Device Cycle Time	10.0ns	A0	
10	SDRAM Device Access Time from Clock	8.0ns	80	
11	DIMM Configuration Type	Non-Parity	00	
12	Refresh Rate/Type	SR/1X(15.625us)	80	
13	Primary SDRAM Device Width	x8	08	
14	Error Checking SDRAM Device Width	N/A	00	
15	SDRAM Device Attr: Min Clk Delay, Random Col Access	1 Clock	01	
16	SDRAM Device Attributes: Burst Lengths Supported	1,2,4,8, Full Page	8F	
17	SDRAM Device Attributes: Number of Device Banks	2	02	
18	SDRAM Device Attributes: CAS Latencies Supported	1, 2, 3	07	
19	SDRAM Device Attributes: $\overline{CS}$ Latency	0	01	
20	SDRAM Device Attributes: $\overline{WE}$ Latency	0	01	
21	SDRAM Module Attributes	Unbuffered	00	
22	SDRAM Device Attributes: General	Wr-1/Rd Burst, Precharge All, Auto-Precharge, V_{DD}	0E	
23	Minimum Clock Cycle at CLX-1	15.0ns	F0	
24	Maximum Data Access Time (t_{AC}) from Clock at CLX-1	9.0ns	90	
25	Minimum Clock Cycle Time at CLX-2	30.0ns	78	
26	Maximum Data Access Time (t_{AC}) from Clock at CLX-2	27.0ns	6C	
27	Minimum Row Precharge Time (t_{RP})	30ns	1E	
28	Minimum Row Active to Row Active delay (t_{RRD})	20ns	14	
29	Minimum RAS to CAS delay (t_{RCD})	30ns	1E	
30	Minimum RAS Pulse width (t_{RAS})	60ns	3C	
31	Module Bank Density	16MB	04	
32 - 61	Reserved	Undefined	00	
62	SPD Revision	01	01	
63	Checksum for bytes 0 - 62	Checksum Data	cc	1
64 - 71	Manufacturers' JEDEC ID Code	IBM	A400000000000000	
72	Module Manufacturing Location	Toronto, Canada	91	
		Vimercate, Italy	53	

1. cc = Checksum Data byte, 00-FF (Hex)
2. "R" = Alphanumeric revision code, A-Z, 0-9
3. rr = ASCII coded revision code byte "R"
4. yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex)
5. ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex)
6. ss = Serial number data byte, 00-FF (Hex)



IBM13T2649JC
2M x 64 SDRAM SO DIMM

Serial Presence Detect (Part 2 of 2)

Byte #	Description	SPD Entry Value	Serial PD Data Entry (Hexadecimal)	Notes
73 - 90	Assembly Part Number	ASCII '13T2649JC"R"-10T'	313354323634394A43rr2D31305420202020	2, 3
91 - 92	Module Revision Code	"R" plus ASCII blank	rr20	
93 - 94	Module Manufacturing Date	Year/Week Code	yyww	4, 5
95 - 98	Module Serial Number	Serial Number	ssssssss	6
99 - 125	Reserved	Undefined	00	
126	Module Supports this Clock Frequency	66 MHz	66	
127	CAS Latencies Supported for Clock Frequency defined in byte 126	2, 3	06	
128 - 255	Open for Customer Use	Undefined	00	
1. cc = Checksum Data byte, 00-FF (Hex) 2. "R" = Alphanumeric revision code, A-Z, 0-9 3. rr = ASCII coded revision code byte "R" 4. yy = Binary coded decimal year code, 00-99 (Decimal) → 00-63 (Hex) 5. ww = Binary coded decimal week code, 01-52 (Decimal) → 01-34 (Hex) 6. ss = Serial number data byte, 00-FF (Hex)				



Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V _{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V _{IN}	Input Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
V _{OUT}	Output Voltage	SDRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T _{OPR}	Operating Temperature		0 to +70	°C	1
T _{STG}	Storage Temperature		-55 to +125	°C	1
P _D	Power Dissipation		5.1	W	1
I _{OUT}	Short Circuit Output Current		50	mA	1
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.					

Recommended DC Operating Conditions (T_A= 0 to 70°C)

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V _{DD}	Supply Voltage	3.0	3.3	3.6	V	1
V _{IH}	Input High Voltage	2.0	—	V _{DD} + 0.3	V	1
V _{IL}	Input Low Voltage	-0.3	—	0.8	V	1
1. All voltages referenced to V _{SS} .						

Capacitance (T_A= 25°C, f=1MHz, V_{DD}= 3.3V ± 0.3V)

Symbol	Parameter	Organization	Units
		x64 Max.	
C _{I1}	Input Capacitance (A0 - A9, A10/AP, BA0, $\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$)	50	pF
C _{I2}	Input Capacitance (CKE0)	48	pF
C _{I3}	Input Capacitance ($\overline{\text{S0}}$)	48	pF
C _{I4}	Input Capacitance (CK0, CK1)	32	pF
C _{I5}	Input Capacitance (DQMB0 - DQMB7)	10	pF
C _{I6}	Input Capacitance (SCL)	9	pF
C _{IO1}	Input/Output Capacitance (DQ0 - DQ63)	9	pF
C _{IO2}	Input/Output Capacitance (SDA)	11	pF

Output Characteristics (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

Symbol	Parameter	x64		Units	
		Min.	Max.		
I _{I(L)}	Input Leakage Current, any input (0.0V ≤ V _{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	RAS, CAS, WE, CKE0, A0-A9, A10/AP, BA0	-8	+8	μA
		CK0, CK1	-4	+4	
		S0	-8	+8	
		DQMB0, - 7	-1	+1	
		DQ0 - 63	-1	+1	
		SCL, SDA	-1	+1	
I _{O(L)}	Output Leakage Current (D _{OUT} is disabled, 0.0V ≤ V _{OUT} ≤ 3.6V)	DQ0 - 63, SDA	-1	+1	μA
V _{OH}	Output Level Output "H" Level Voltage (I _{OUT} = -2.0mA)		2.4	V _{DD}	V
V _{OL}	Output Level Output "L" Level Voltage (I _{OUT} = +2.0mA)		0.0	0.4	

Standby and Refresh Currents (T_A = 0 to +70°C, V_{DD} = 3.3V ± 0.3V)

Parameter	Symbol	Test Condition		Organization	Units	Notes
				x64		
Precharge Standby Current in Power Down Mode	IDD _{1P}	CKE0 ≤ V _{IL} (max), t _{CK} = 15ns		24	mA	
	IDD _{1PS}	CKE0 ≤ V _{IL} (max), t _{CK} = Infinity		16	mA	
Precharge Standby Current in Non-Power Down Mode	IDD _{1N}	CKE0 ≥ V _{IH} (min), t _{CK} = 15ns Input Change every 30ns		200	mA	S ₀ = High
	IDD _{1NS}	CKE0 ≥ V _{IH} (min), t _{CK} = Infinity No Input Change		80	mA	
Active Standby Current in Power Down Mode	IDD _{2P}	CKE0 ≤ V _{IL} (max), t _{CK} = 15ns		24	mA	1
	IDD _{2PS}	CKE0 ≤ V _{IL} (max), t _{CK} = Infinity		16	mA	1
Active Standby Current in Non-Power Down Mode	IDD _{2N}	CKE0 ≥ V _{IH} (min), t _{CK} = 15ns Input Change every 30ns		200	mA	S ₀ = High
	IDD _{2NS}	CKE0 ≥ V _{IH} (min), t _{CK} = Infinity No Input Change		120	mA	
Auto (CBR) Refresh Current	IDD ₃	CAS Latency = 1 t _{RC} ≥ t _{RC} (min)	-10	680	mA	2, 3, 4
		CAS Latency = 2 t _{RC} ≥ t _{RC} (min)	-10	720	mA	
		CAS Latency = 3 t _{RC} ≥ t _{RC} (min)	-10	880	mA	
Self Refresh Current	IDD ₄	CKE0 ≤ 0.2V		16	mA	
Serial PD Device Standby Current	I _{SB}	V _{IN} = GND or V _{DD}		10	μA	5

1. Active Standby Current will be higher if Clock Suspend is entered during a Burst Read cycle (add 1mA per DQ).

2. The specified values are valid when addresses are changed no more than once during t_{CK}(min).

3. The specified values are valid when No Operation commands are registered on every rising clock edge during t_{RC}(min).

4. The specified values are valid when data inputs (DQ's) are stable during t_{RC}(min).

5. V_{DD} = 3.3V



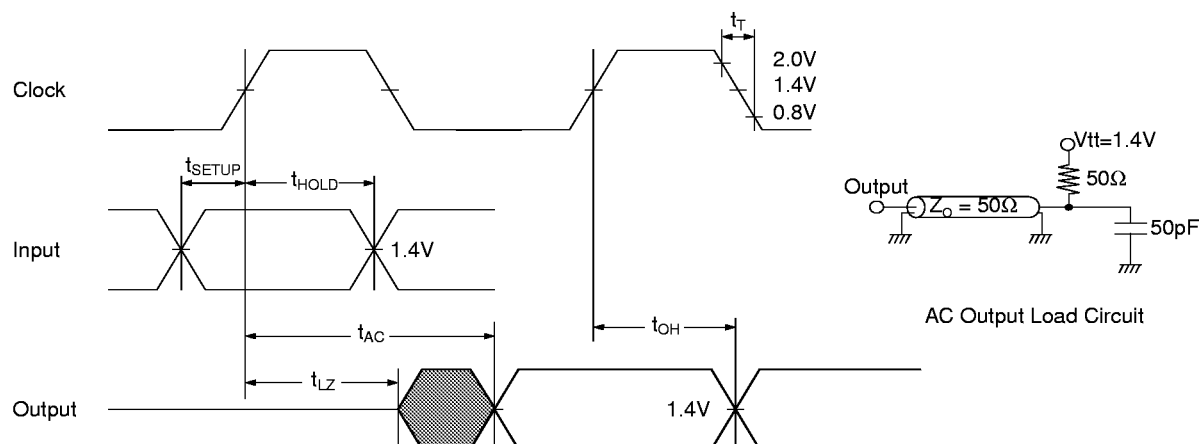
Operating Currents ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

Symbol	Parameter	Test Condition	CAS Latency	$t_{RC}(\text{min})$	Speed Sort	Organization	Units	Notes
I_{DD5}	Operating Current Burst Length = 1	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	90 ns	-10	760	mA	1, 2
			CL=2	90 ns	-10	840		
			CL=3	90 ns	-10	1000		
I_{DD6}	Operating Current Burst Length = 2	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	120 ns	-10	600	mA	1, 2, 3
			CL=2	105 ns	-10	800		
			CL=3	125 ns	-10	1000		
I_{DD7}	Operating Current Burst Length = 4	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	180 ns	-10	520	mA	1, 2, 3
			CL=2	135 ns	-10	760		
			CL=3	120 ns	-10	1000		
I_{DD8}	Operating Current Burst Length = 8	$t_{RC} = t_{RC}(\text{min})$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	300 ns	-10	480	mA	1, 2, 3
			CL=2	195 ns	-10	720		
			CL=3	160 ns	-10	1000		
I_{DD9}	Operating Current Burst Length = Full Page	$t_{RC} = \text{Infinity}$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	$t_{RC} = \infty$ $t_{CK} = 30\text{ ns}$	-10	360	mA	1, 2, 3
			CL=2	$t_{RC} = \infty$ $t_{CK} = 15\text{ ns}$	-10	600		
			CL=3	$t_{RC} = \infty$ $t_{CK} = 10\text{ ns}$	-10	840		
I_{DD10}	Operating Current 1N Rule (Continuous Read/Write cycles with new column address regis- tered each clock cycle)	$t_{RC} = \text{Infinity}$ $t_{CK} \geq t_{CK}(\text{min})$ $I_O = 0\text{mA}$	CL=1	$t_{RC} = \infty$ $t_{CK} = 30\text{ ns}$	-10	680	mA	1, 2
			CL=2	$t_{RC} = \infty$ $t_{CK} = 15\text{ ns}$	-10	1040		
			CL=3	$t_{RC} = \infty$ $t_{CK} = 10\text{ ns}$	-10	1400		
I_{DDA}	Serial PD Device Active Power Supply Current	SCL Clock Frequency = 100kHz				1.0	mA	4

1. The specified values are obtained with the output open.
2. The specified values are valid when addresses and DQ's are changed no more than once during $t_{CK}(\text{min})$.
3. The specified values are obtained when the programmed burst length is executed to completion without interruption by a subsequent burst Read or Write cycle.
4. Input pulse levels $V_{DD} \times 0.1$ to $V_{DD} \times 0.9$, input rise and fall times 10ns, input and output timing levels $V_{DD} \times 0.5$, output load 1 TTL gate and CL = 100pf.

AC Characteristics ($T_A = 0$ to $+70^\circ\text{C}$, $V_{DD} = 3.3\text{V} \pm 0.3\text{V}$)

1. An initial pause of $100\mu\text{s}$ is required after power-up, then a Precharge All Banks command must be given followed by a minimum of two Auto (CBR) Refresh cycles before the Mode Register Set operation can begin.
2. AC timing tests have $V_{IL} = 0.8\text{V}$ and $V_{IH} = 2.0\text{V}$ with the timing referenced to the 1.40V crossover point.



3. The Transition time is measured between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}).
4. AC measurements assume $t_T=1\text{ns}$.
5. In addition to meeting the transition rate specification, the clock and $\overline{\text{CKE}}$ n must transit between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.

Clock and Clock Enable Parameters

Symbol	Parameter	-10		Units	Notes
		Min.	Max.		
t_{CK3}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 3	10	100MHz	ns	
t_{CK2}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 2	15	66MHz	ns	
t_{CK1}	Clock Cycle Time, $\overline{\text{CAS}}$ Latency = 1	30	33MHz	ns	
t_{AC3}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 3	—	8	ns	1, 2
t_{AC2}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 2	—	9	ns	1, 2
t_{AC1}	Clock Access Time, $\overline{\text{CAS}}$ Latency = 1	—	27	ns	1, 2
t_{CKH}	Clock High Pulse Width	3.5	—	ns	3
t_{CKL}	Clock Low Pulse Width	3.5	—	ns	3
t_{CES}	Clock Enable Set-up Time	3	—	ns	
t_{CEH}	Clock Enable Hold Time	1	—	ns	
t_{CESP}	CKE Set-up Time (Power down mode)	3	—	ns	
t_{T}	Transition Time (Rise and Fall)	1	30	ns	

1. Access time is measured at 1.4V. See AC output load circuit.
2. Access time is measured assuming a clock rise time of 1ns. If clock rise time is longer than 1ns, then $(t_{\text{RISE}}/2-0.5)\text{ns}$ should be added to the parameter.
3. Assumes clock rise and fall times are equal to 1ns. If rise or fall time exceeds 1ns, then other AC parameters under consideration should be compensated by an additional $[(t_{\text{RISE}}+t_{\text{FALL}})/2-1]\text{ns}$.



Common Parameters

Symbol	Parameter	-10		Units
		Min.	Max.	
t_{CS}	Command Setup Time	3	—	ns
t_{CH}	Command Hold Time	1	—	ns
t_{AS}	Address and Bank Select Set-up Time	3	—	ns
t_{AH}	Address and Bank Select Hold Time	1	—	ns
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	30	—	ns
t_{RC}	Bank Cycle Time	90	120000	ns
t_{RAS}	Active Command Period	60	120000	ns
t_{RP}	Precharge Time	30	—	ns
t_{RRD}	Bank to Bank Delay Time	20	—	ns
t_{CCD}	$\overline{CAS}$ to $\overline{CAS}$ Delay Time (Same Bank)	1	—	CLK

Refresh Cycle

Symbol	Parameter	-10		Units	Notes
		Min.	Max.		
t_{SREX}	Self Refresh Exit Time	$10\text{ns} + t_{RC}$	—	ns	3
t_{REF}	Refresh Period	—	64	ms	1, 2

1. 4096 cycles.
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to “wake-up” the device.
3. Self Refresh Exit is an asynchronous operation. Self refresh exit is accomplished by starting the clock (CLK) and then asserting CKE high. During the exit time (t_{SREX}), no commands may be issued until t_{RC} is satisfied and CKE must remain high. It is recommended to hold $\overline{CS}$ high during the self refresh exit time, but NOP commands may be issued with each rising clock edge during this period as an alternative. To prevent erroneous exit of self refresh operation, a glitch suppressor circuit is incorporated into the CKE receiver. If CKE is asserted high (system noise) for less than 10ns (approximately), then the device will not exit self refresh operation.

Read Cycle

Symbol	Parameter	-10		Units	Notes
		Min.	Max.		
t_{OH}	Data Out Hold Time	3	—	ns	
t_{LZ}	Data Out to Low Impedance Time	3	—	ns	
t_{HZ3}	Data Out to High Impedance Time, CL= 3	3	8	ns	1
t_{HZ2}	Data Out to High Impedance Time, CL= 2	3	10	ns	1
t_{HZ1}	Data Out to High Impedance Time, CL= 1	3	18	ns	1
t_{DQZ}	DQM Data Out Disable Latency	2	—	CLK	

1. Referenced to the time at which the output achieves the open circuit condition, not to output voltage levels.

Write Cycle

Symbol	Parameter	-10		Units
		Min.	Max.	
t_{DS}	Data In Set-up Time	3	—	ns
t_{DH}	Data In Hold Time	1	—	ns
t_{DPL}	Data input to Precharge	10	—	ns
t_{DQW}	DQM Write Mask Latency	0	—	CLK

Clock Frequency and Latency

Symbol	Parameter	Speed Sort			Units
		-10			
f _{CK}	Clock Frequency	100	66	33	MHz
t _{CK}	Clock Cycle Time	10	15	30	ns
t _{AA}	CAS Latency	3	2	1	CLK
t _{RCD}	RAS to CAS Delay	3	2	1	CLK
t _{RL}	RAS Latency	6	4	2	CLK
t _{RC}	Bank Cycle Time	9	6	3	CLK
t _{RAS}	Minimum Bank Active Time	6	4	2	CLK
t _{RP}	Precharge Time	3	2	1	CLK
t _{DPL}	Data In to Precharge	1	1	1	CLK
t _{DAL}	Data In to Active/Refresh	4	3	2	CLK
t _{RRD}	Bank to Bank Delay Time	2	2	1	CLK
t _{CCD}	CAS to CAS Delay Time	1	1	1	CLK
t _{WL}	Write Latency	0	0	0	CLK
t _{DQW}	DQM Write Mask Latency	0	0	0	CLK
t _{DQZ}	DQM Data Disable Latency	2	2	2	CLK
t _{CSL}	Clock Suspend Latency	1	1	1	CLK

Functional Description and Timing Diagrams

Refer to the IBM 16Mb Synchronous DRAM data sheet, document SA14-4711-06 (Revised 5/97), for the functional description and timing diagrams for SDRAM operation.

Refer to the IBM Application Notes: *Serial Presence Detect on Memory DIMMs* and *SDRAM Presence Detect Definitions* for the Serial Presence Detect functional description and timings.

All AC timing information refers to the timings at the SDRAM devices.



Front

67.60
2.661

63.60
2.504

24.5
.9646

4.00
.157

(2X) Ø 1.800
.0709

2.00 MIN
.0787

25.4
1.00

20.00
.7874

6.00
.236

3.30
.1299

23.2
.9134

4.60
.1811

2.50
.0984

32.80
1.293

2M x 64 Side

3.80 MAX
0.1496

6.215
.2447 MIN

1.00 ± 0.10
.039 ± .0039

2.55
.1004

0.25 MAX
0.009

0.60 ± .05 WIDTH
.0236

0.80 TYP PITCH
.0315

Note: All dimensions are typical unless otherwise stated.

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INCHES

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IBM13T2649JC
2M x 64 SDRAM SO DIMM

Revision Log

Rev	Contents of Modification
12/96	Initial Release
3/97	Update Serial Presence Detect table Update power
11/97	Die Revision
3/98	Removed DC Output Load Circuit diagram.



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