256K/512K x 64 SGRAM SO DIMM

Features

- 144 Pin Graphics JEDEC Standard, 8 Byte Synchronous Small Outline Dual-In-line Memory Module
- Performance:

Speed Grade	7R5	10	Units
Clock Frequency	133	100	MHz
Clock Cycle	7.5	10	ns
Clock Access Time	7	9	ns

- All inputs and outputs are LVTTL (3.3V) compatible
- Single 3.3V ± 0.3V Power Supply
- SDRAMs have 2 internal banks; module has 2 banks
- 8 Column Block Write and Write-per-Bit mode
- Independent byte operation via DQM0-7
- Programmable Operation:
  -CAS Latency: 1, 2, 3
  -Burst Type: Sequential or Interleave
  -Burst Length: 1, 2, 4, 8, Full-Page (Full-Page supports Sequential burst only)
  -Operation: Burst Read and Write or Multiple Burst Read with Single Write
- Auto Refresh (CBR)
- Automatic and controlled Precharge Commands
- 9/8/1 Addressing (Row/Column/Bank)
- 1K refresh cycles in 16ms; 1K refresh cycles or 128ms for self refresh parts.
- Serial Presence Detect
- Card size:
  2.66" x 1.0" x 0.111"; gold contacts (256K x 64)
  2.66" x 1.15" x 0.179"; gold contacts (512K x 64)
- SGRAMS in 100-pin LQFP Package

Description

IBM13V51649AN is a 144-pin Synchronous GRAM Small Outline Dual In-line Memory Module (SO DIMM) organized as a 512Kx64 high-speed memory array. The SO DIMM uses four 256Kx32 SGRAMs in 20x14mil LQFP packages. The SO DIMM achieves high speed data transfer rates of up to 133MHz by employing a prefetch/pipeline hybrid architecture that supports the JEDEC 1N rule while allowing very low burst power. IBM13V51649AP is supplied with long retention, self-refresh devices.

All control, address, and data input/output circuits are synchronized with the positive edge of the externally supplied clock inputs.

All inputs are sampled at the positive edge of each externally supplied clock (CK0, CK1). Internal operating modes are defined by combinations the $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{S0}$, DQMB, and CKE signals. A command decoder initiates the necessary timings for each operation. A 10 bit address bus accepts address information in a row/column multiplexing arrangement.

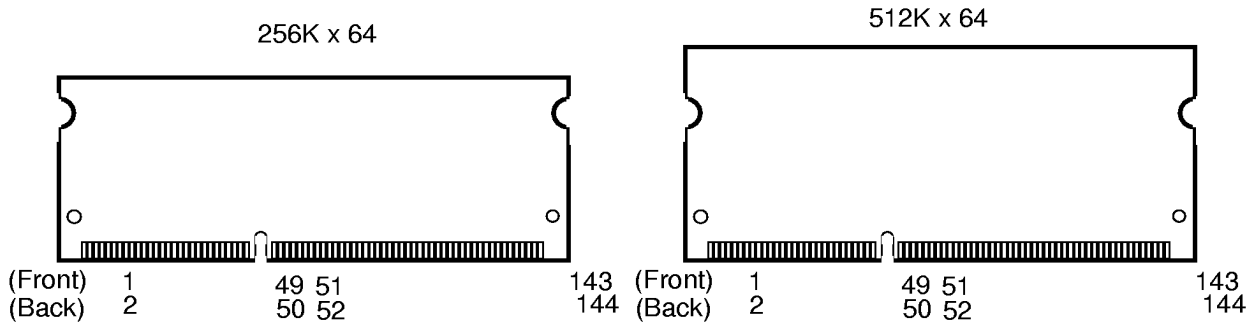
Prior to any access operation, the $\overline{CAS}$ latency, burst type, burst length, and burst operation type must be programmed into the SO DIMM by address inputs A0-A9 during the mode register set cycle.

SGRAMs differ from Synchronous DRAMs (SDRAMs) by providing 8 Column Block Write and Write-per-Bit (WPB) functions. The Block Write and WPB functions may be combined with individual byte enables (DQM0 - DQM7).

The SO DIMM uses serial presence detects implemented via a serial EEPROM using the two-pin IIC protocol. The first 128 bytes of serial PD data are used by the SO DIMM manufacturer. The last 128 bytes are available to the customer. In addition, resistor strapping on DQ31 - DQ29 indicate synchronous clock frequency and memory timings.

All IBM 144-pin SO DIMMs provide a high performance, flexible 8-byte interface in a 2.65” long space-saving footprint.

Card Outlines



Pin Description

A0 - A9	Address Inputs	DQMB0 - DQMB7	DQ Mask Enable
A0 - A8	Row Address Inputs	DSF	Special Function Enable
A0 - A7	Column Address Inputs	RSVD, RFU	No Connection
A9	Bank Select	V_{CC}	Supply Voltage
$\overline{CS0}$, $\overline{CS1}$	Chip Selects	V_{SS}	Ground
$\overline{CAS}$	Column Address Strobe	$\overline{WE}$	Write Enable
CKE	Clock Enable	SCL	Serial Presence Detect Clock Input
CK0, CK1	System Clock Inputs	SDA	Serial Presence Detect Data Input/Output
DQ0 - DQ63	Data Inputs/Outputs	SBA	Serial Presence Detect Address Input

Pinout

Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side	Pin#	Front Side	Pin#	Back Side
1	V_{SS}	2	V_{SS}	37	V_{SS}	38	V_{SS}	71	V_{SS}	72	V_{SS}	107	DQ21	108	DQ20
3	DQ63	4	DQ62	39	DQ39	40	DQ38	73	CK1	74	CK0	109	DQ19	110	DQ18
5	DQ61	6	DQ60	41	DQ37	42	DQ36	75	V_{CC}	76	V_{CC}	111	DQ17	112	DQ16
7	DQ59	8	DQ58	43	DQ35	44	DQ34	77	RSVD	78	RSVD	113	V_{CC}	114	V_{CC}
9	DQ57	10	DQ56	45	DQ33	46	DQ32	79	RSVD	80	RSVD	115	DQMB3	116	DQMB2
11	V_{CC}	12	V_{CC}	47	V_{CC}	48	V_{CC}	81	A9	82	A8	117	DQMB1	118	DQMB0
13	DQ55	14	DQ54	49	RSVD	50	RSVD	83	A7	84	A6	119	V_{SS}	120	V_{SS}
15	DQ53	16	DQ52	VOLTAGE KEY				85	V_{SS}	86	V_{SS}	121	DQ15	122	DQ14
17	DQ51	18	DQ50	51	RSVD	52	RSVD	87	A5	88	A4	123	DQ13	124	DQ12
19	DQ49	20	DQ48	53	RSVD	54	RSVD	89	A3	90	A2	125	DQ11	126	DQ10
21	V_{SS}	22	V_{SS}	55	V_{SS}	56	V_{SS}	91	A1	92	A0	127	DQ9	128	DQ8
23	DQMB7	24	DQMB6	57	DSF	58	RFU	93	V_{CC}	94	V_{CC}	129	V_{CC}	130	V_{CC}
25	DQMB5	26	DQMB4	59	RFU	60	RFU	95	DQ31	96	DQ30	131	DQ7	132	DQ6
27	V_{CC}	28	V_{CC}	61	RFU	62	SBA	97	DQ29	98	DQ28	133	DQ5	134	DQ4
29	DQ47	30	DQ46	63	V_{CC}	64	V_{CC}	99	DQ27	100	DQ26	135	DQ3	136	DQ2
31	DQ45	32	DQ44	65	$\overline{CS1}$	66	$\overline{CS0}$	101	DQ25	102	DQ24	137	DQ1	138	DQ0
33	DQ43	34	DQ42	67	$\overline{RAS}$	68	$\overline{CAS}$	103	V_{SS}	104	V_{SS}	139	V_{SS}	140	V_{SS}
35	DQ41	36	DQ40	69	$\overline{WE}$	70	CKE	105	DQ23	106	DQ22	141	SDA	142	SCL
												143	V_{CC}	144	V_{CC}

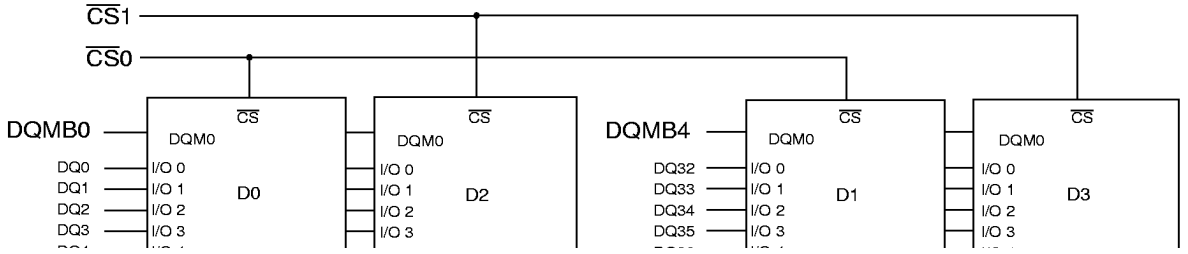
Note: Assignments are consistent for all 8 Byte densities.

Ordering Information

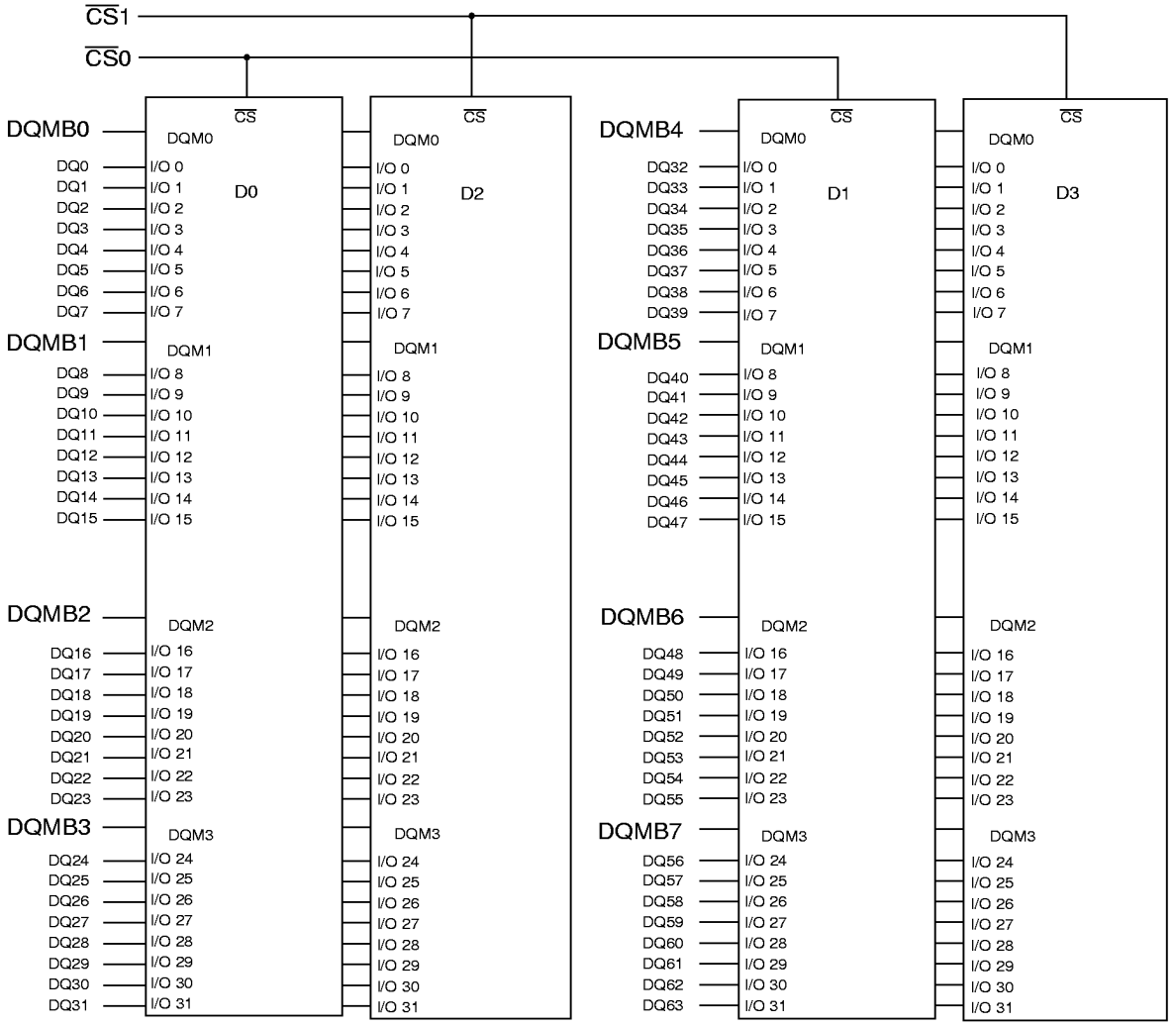
Part Number	Organization	Clock Cycle	Leads	Dimension	Supply Voltage	Notes
IBM13V25649AN-7R5T	256Kx64	7.5ns		2.66"x1.0"x0.111"		
IBM13V25649AN-10T		10ns				1
IBM13V51649AN-7R5T	512Kx64	7.5ns		2.66"x1.15"x0.175"		
IBM13V51649AN-10T		10ns	Au		3.3V	

IBM13V25649AP IBM13V51649AN
IBM13V25649AN IBM13V51649AP
256K/512K x 64 SGRAM SO DIMM

512Kx64 SGRAM DIMM Block Diagram

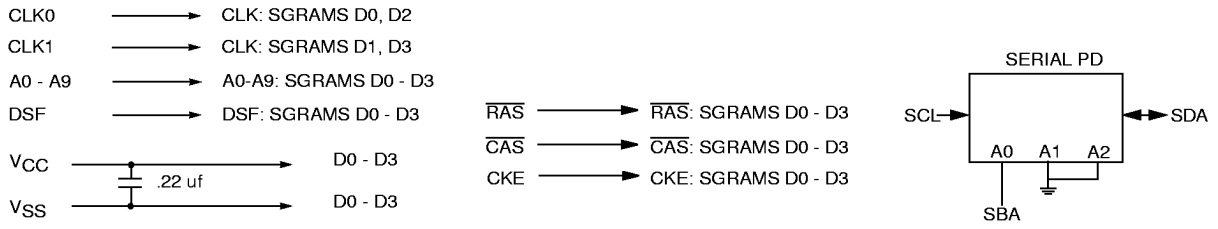


512Kx64 SGRAM DIMM Block Diagram



NOTE: D2 and D3 not present on 256K x 64 DIMM

NOTE: DQ Wiring may differ from that described in this drawing. However, DQ/DQMB/CLK/CS are maintained as shown.



Signal Descriptions

Name	I/O	Function
A_0-A_8, (A_9)	I	Address bits A_0-A_8 are row addresses when Active command is activated. Address bits A_0-A_7 are column addresses when $\overline{CAS}$ is active. Address bit A_8, when $\overline{CAS}$ is active, enables/disables Auto Precharge. Address bit A_9 selects which of the two memory banks is to be used.
$\overline{CAS}$	I	$\overline{CAS}$ is part of the input command to the SGRAM.
CKE	I	Clock Enable disables the SGRAM clock internally, thus allowing data to remain on the output for several CLK cycles. Clock Enable is also used as part of the input command to specify self-refresh.
CK0, CK1	I	CKn is driven by the system clock. All SGRAM input signals are sampled on the positive edge of CKn. CKn also increments the internal burst counter and controls the output registers.
$\overline{CS0}$, $\overline{CS1}$	I	Chip Select indicates that the command on the input lines is for this device. If $\overline{CS}$n are high, the input command(s) will be ignored.
DQ_0-DQ_{63}	I/O	Data Input/Output lines transfer data between the memory array and the system bus. These are also input mask bits for Write-per-Bit. When Block Write is activated, DQs provide column address mask.
DQM_0-DQM_7	I	During Read, DQM=1 turns off the output buffers. During Write, DQM=1 prevents a write to the current memory location. DQM_0 corresponds to the lowest byte (DQ_0-DQ_7). DQM_1 corresponds to $DQ_{8\text{-}15}$. DQM_2 corresponds to $DQ_{16\text{-}23}$. DQM_3 corresponds to $DQ_{24\text{-}31}$. DQM_4 corresponds to $DQ_{32\text{-}39}$. DQM_5 corresponds to $DQ_{40\text{-}47}$. DQM_6 corresponds to $DQ_{48\text{-}55}$. DQM_7 corresponds to $DQ_{56\text{-}63}$.
$\overline{RAS}$	I	$\overline{RAS}$ is part of the input command to the SGRAM.
$\overline{WE}$	I	Write Enable is part of the input command.

Resistor Strapping Options

Resistor Strapping Options

Three resistor straps are used to indicate the synchronous clock frequency (period) and memory timing.

Cycle Time	DQ31	DQ30	DQ29
15 ns	0	0	0
12 ns	0	0	1
10 ns*	0	1	0
7.5 ns*	0	1	1
reserved	1	0	0
reserved	1	0	1
reserved	1	1	0
reserved	1	1	1

* Supported by IBM SGRAM SO DIMMs.
Note: A logic low (i.e. 0) indicates that the resistor strapping is tied to ground (V_{SS}). A logic high (i.e. 1) indicates that the resistor strapping is tied to V_{CC}. Resistors are 4.7K on the DQ lines.

Serial Presence Detect

Note: As of 4/4/97, the initial release of the specification, SPD definition for SGRAM SO DIMMs is not yet finalized. Upon final approval by JEDEC this specification will be revised to reflect the completed SPD defini-

IBM13V25649AP IBM13V51649AN
IBM13V25649AN IBM13V51649AP
256K/512K x 64 SGRAM SO DIMM

Absolute Maximum Ratings

Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Notes
V_{DD}	Power Supply Voltage		-0.3 to +4.6	V	1
V_{IN}	Input Voltage	SGRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
V_{OUT}	Output Voltage	SGRAM Devices	-1.0 to +4.6		
		Serial PD Device	-0.3 to +6.5		
T_{OPR}	Operating Temperature		0 to +70	°C	1
T_{STG}	Storage Temperature		-55 to +125	°C	1
P_D	Power Dissipation		2, 2MB / 4, 4MB	W	1
I_{OUT}	Short Circuit Output Current		50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

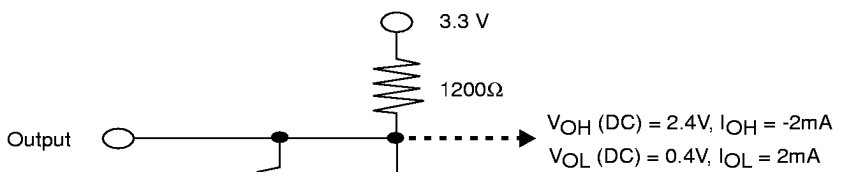
Recommended DC Operating Conditions (T_A= 0 to 70˚C)

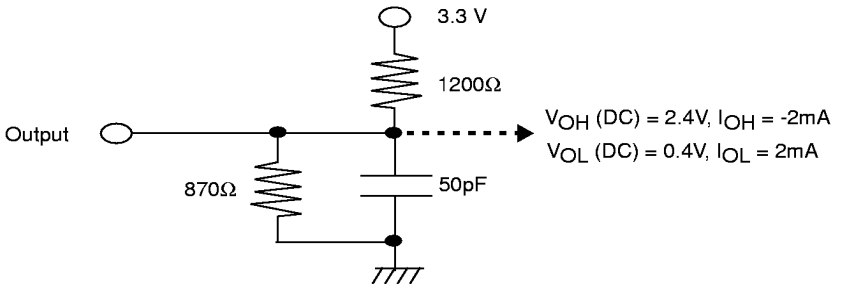
Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{CC}	Supply Voltage	3.0	3.3	3.6	V	1
V_{IH}	Input High Voltage	2.0	—	V_{CC} + 0.3	V	1
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	1

1. All voltages referenced to V_{SS} .

Capacitance (T_A= 25°C, f=1MHz, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter	256Kx64	512Kx64	Units
C_{I1}	Input Capacitance (A0 - A9)	21	36	pF
C_{I2}	Input Capacitance (CKE, CS, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF)	20	34	pF
C_{I3}	Input Capacitance (CK0, CK1)	17	17	pF
C_{I4}	Input Capacitance (DQMB0 - DQMB7)	10	18	pF





DC Output Load Circuit

Output Characteristics (T_A= 0 to +70˚C, V_{CC}= 3.3V ± 0.3V)

Symbol	Parameter		256Kx64		512Kx64		Units	Notes
			Min.	Max.	Min.	Max.		
$I_{I(L)}$	Input Leakage Current, any input (0.0V ≤ V_{IN} ≤ 3.6V), All Other Pins Not Under Test = 0V	All Inputs	-6	6	-12	12	µA	
		CLK0	-6	6	-6	6		
		CLK1	-	-	-6	6		
		$\overline{CS0}$	-6	6	-6	6		
		$\overline{CS1}$	-	-	-6	6		
		DQMB0, - 7	-3	3	-6	6		
		DQ0 - 63	-3	3	-6	6		
		SCL, SDA	-1	1	-1	1		
$I_{O(L)}$	Output Leakage Current (D_{OUT} is disabled, 0.0V ≤ V_{OUT} ≤ 3.6V)	DQ0 - 63, SDA	-3	3	-6	6	µA	
V_{OH}	Output Level Output "H" Level Voltage (I_{OUT} = -2.0mA)		2.4	V_{DD}	2.4	V_{CC}	V	1
V_{OL}	Output Level Output "L" Level Voltage (I_{OUT} = +2.0mA)		0.0	0.4	0.0	0.4		

1. See DC output load circuit.

I_{CC} Specifications ($0°C \le T_A \le 70°C$; V_{CC}/V_{CCQ} = 3.3V 0.3V)

Symbol	Parameter	Test Condition	$\overline{CAS}$ Latency	Maximum 256Kx64		Maximum 512Kx64		Unit	Notes
				-7R5	-10	-7R5	-10		
I_{CC1}	Operating Current	Burst Length = 1 $t_{RC} \ge t_{RC}$(Min) $t_{CK} \ge t_{CK}$(Min) I_O = 0mA	3	450	370	550	470	mA	1, 5
			2	420	350	520	450		
$I_{CC2}P$	Precharge Standby Current in Power Down Mode	CKE ≤ VIL(Max) t_{CK} =15ns		6	6	12	12	mA	1, 5
$I_{CC2}PS$		CKE ≤ VIL(Max) t_{CK} = Infinity		6	6	12	12		
$I_{CC2}N$	Precharge Standby Current in Non Power Down Mode	CKE ≥ VIH(Min) t_{CK} =15ns Input change every 30ns		90	90	190	190	mA	6
$I_{CC2}NS$		CKE ≥ VIH(Min) t_{CK} =Infinity No input change		40	40	90	90		7
$I_{CC3}P$	Active Standby Current in Power Down Mode	CKE ≤ VIL(Max) t_{CK} =15ns		6	6	12	12	mA	
$I_{CC3}PS$		CKE ≤ VIL(Max) t_{CK} = Infinity		6	6	12	12		
$I_{CC3}N$	Active Standby Current in Non Power Down Mode	CKE ≥ VIH(Min) t_{CK} =15ns Input change every 30ns		100	100	200	200	mA	
$I_{CC3}NS$		CKE ≥ VIH(Min) t_{CK} =Infinity No input change		50	50	100	100		
I_{CC4}	Operating Current (Burst Mode)	t_{RC} =Infinity I_O = 0mA Dual Bank Interleave Continuous	3	400	380	500	480	mA	2, 8
			2	300	280	400	380		
I_{CC5}	Auto Refresh Current	$t_{RC} \ge t_{RC}$(Min)	3	420	370	840	740	mA	3, 4
			2	340	310	680	610		
I_{CC6}	Self Refresh Current	CKE = 0.2V		6	6	12	12	mA	4, 9
I_{CCA}	Serial PD Device Active Power Supply Current	SCL Clock Frequency = 100kHz		1	1	1	1	mA	9

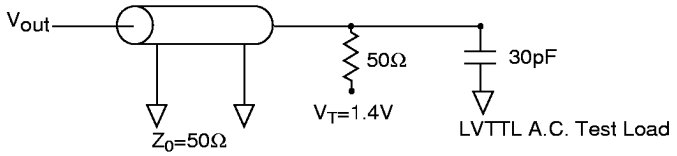
1. Measured with outputs open, inputs 0-3V.
2. Assumes minimum column address update cycle.
3. Refresh period is 16ms.
4. Assumes all SGRAMs in Self-refresh.
5. One bank operating; if 512Kx64, one bank in active standby, non-power down mode.
6. One bank precharge; if 512Kx64, one bank in active standby, non-power down mode.
7. One bank precharge; if 512Kx64, one bank in active standby, no input change.
8. One bank in burst; if 512Kx64, one bank in active standby.

Timing Specifications and Conditions ($0°C \le t_A \le 70°C$; V_{CC}/V_{CCQ} = 3.3V ± 0.3V)

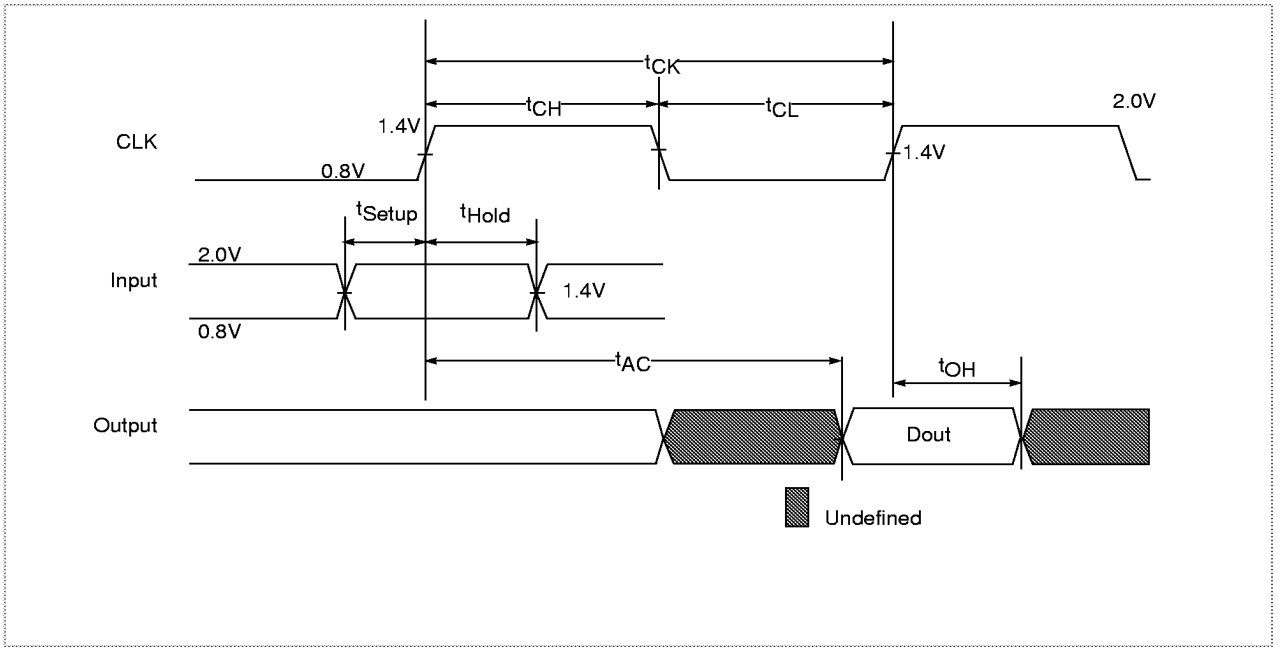
1. All voltages are referenced to V_{SS} (GND).
2. I_{CC} depends on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.

Timing Specifications and Conditions ($0°C \le t_A \le 70°C$; $V_{CC}/V_{CCQ} = 3.3V \pm 0.3V$)

1. All voltages are referenced to V_{SS} (GND).
2. Icc depends on output loading and cycle rates. Specified values are obtained with minimum cycle time and the outputs open.
3. Enables on-chip refresh and address counters.
4. The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range ($0°C \le T_A \le 70°C$).
5. An initial pause of 100ms is required after power up, followed by two Auto Refresh commands to ensure proper device operation.
6. The timing specifications assume a transition time (t_T = 1ns).
7. AC timing tests have V_{IL} = 0.8V and V_{IH} = 2.0V with timing reference to 1.4V crossover point.



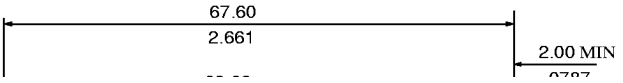
I/O Timing Diagrams



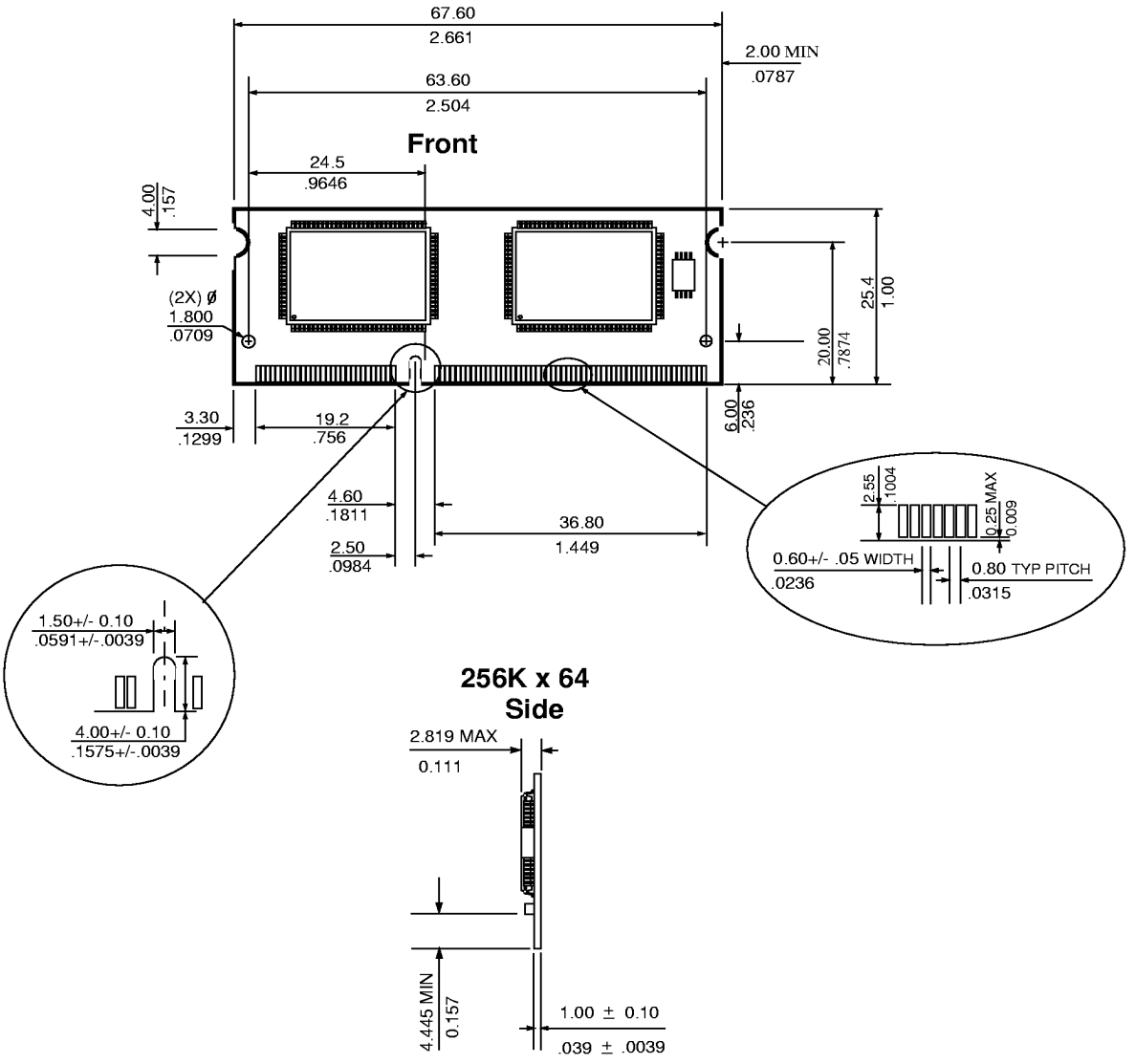
Timing Specifications

Note: all AC timing information below refers to SGRAM device timings. So DIMM level XTK/IBIS models are available to perform system level simulation and timing analysis.		$\overline{CAS}$ Latency	-7R5		-10		Units
Symbol	Parameter		Min	Max	Min	Max	
t_{AC3} for 50 pF load	Access time from CLK (positive edge)	3	-	7	-	9	ns
t_{AC2} for 50 pF load		2	-	10	-	12	
t_{AH}	Address hold time		1.5	-	1.5	-	ns
t_{AS}	Address setup time		2.5	-	2.5	-	ns
t_{BPL}	Block Write to Precharge delay		7.5	-	10	-	ns
t_{BWC}	Block Write cycle time		7.5	-	10	-	ns
t_{CH}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM hold time		1.0	-	1.0	-	ns
t_{CHI}	CLK high level width		3	-	3.5	-	ns
t_{CK3}	System clock cycle time	3	7.5	-	10	-	ns
t_{CK2}		2	12	-	15	-	
t_{CKH}	CKE hold time		1.0	-	1.0	-	ns
t_{CKS}	CKE setup time		2.5	-	2.5	-	ns
t_{CL}	CLK low level width		3	-	3.5	-	ns
t_{CS}	$\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, DSF, DQM setup time		2.5	-	2.5	-	ns
t_{DH}	Date-in hold time		1.5	-	1.5	-	ns
t_{DS}	Data-in setup time		2.5	-	2.5	-	ns
t_{HZ}	Data-out high impedance time		3.5	10	3.5	10	ns
t_{LZ}	Data-out low impedance time		3	-	3	-	ns
t_{MTC}	Load Mode Register command to command		1	-	1	-	t_{CK}
t_{OH}	Data-out hold time		3.5	-	3.5	-	ns
t_{RAS}	Active to Precharge command period		45	120K	60	120K	ns
t_{RC}	Auto Refresh and Active to Active command period		67.5	-	90	-	ns
t_{RCD}	Active to Read, Write or Block Write delay		22.5	-	30	-	ns
t_{REF}	Refresh Period (1024 cycles) for Non Self-Refresh parts		-	16	-	16	ms
t_{REF}	Refresh Period (1024 cycles) for Self-Refresh parts		-	128	-	128	ms
t_{RP}	Row Precharge time		22.5	-	30	-	ns
t_{RRD}	Active bank A to Active bank B command period		7.5	-	10	-	ns
t_{SML}	Load Special Mode Register command to command		1	-	1	-	t_{CK}
t_T	Transition time		1	30	1	30	ns
t_{WR}	Write recovery time		7.5	-	10	-	ns
t	Exit Self-Refresh to Active command		100		100		ns

Layout Drawing (IBM13A25649AP/N)

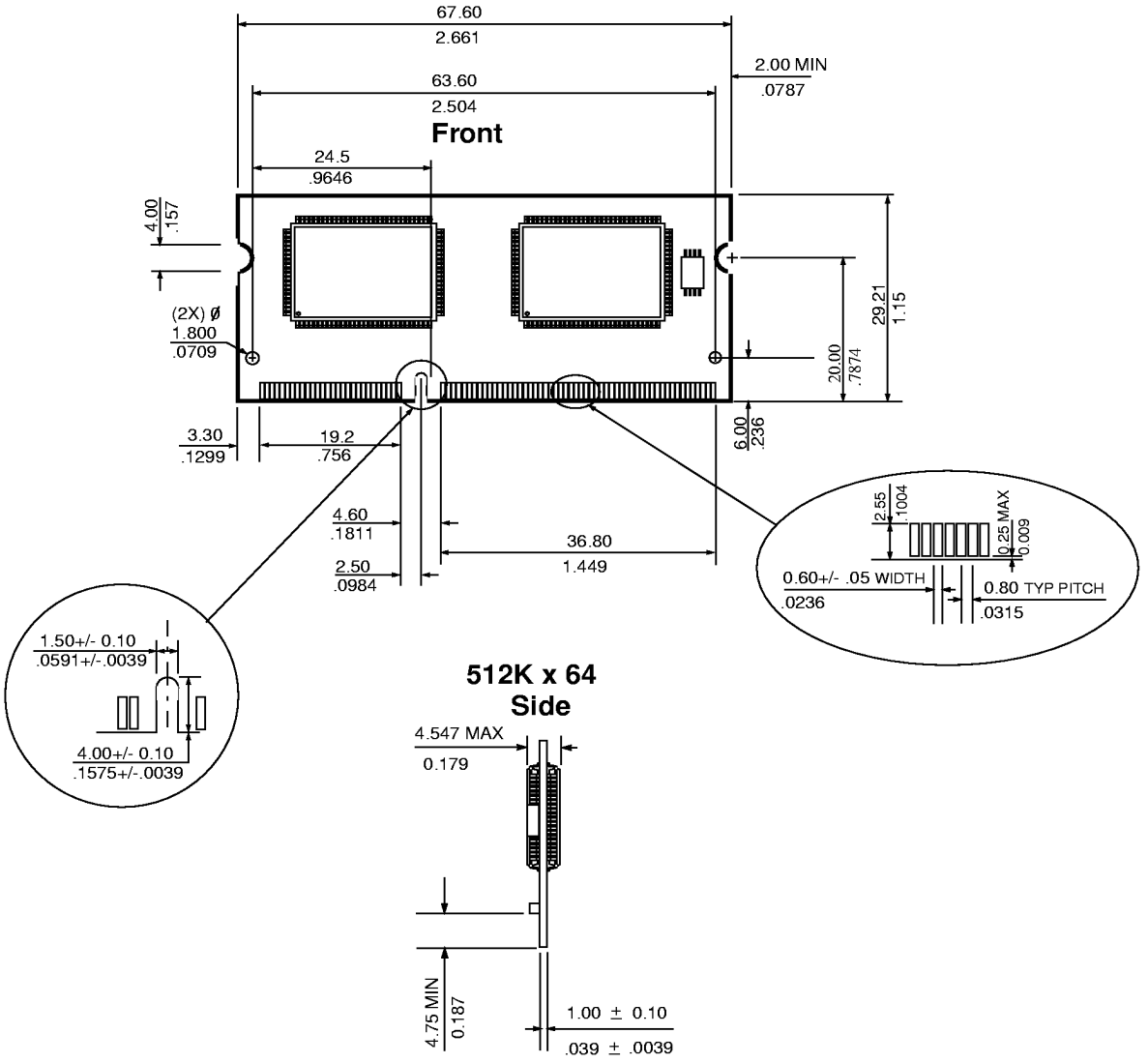


Layout Drawing (IBM13A25649AP/N)



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Layout Drawing (IBM13A51649AP/N)



Note: All dimensions are typical unless otherwise stated. MILLIMETERS / INCHES

Revision Log

Rev	Contents of Modification
4/97	Initial Release