Features

- 256KB and 512KB secondary cache module family for Intel Triton chip set.
- Organized as a 32K or 64K x 64 package on a 4.34" x 1.13", 160-lead, Dual Read-out DIMM
- Available in interleaved (i486/Pentium™) burst mode and asynchronous SRAMs.
- Operation from 50 MHz to 75 MHz supported.
- Low capacitive address, control, clock, and data bus loading
- Dual +3.3V and +5V, +/- 5% power supplies
- 5V-tolerant common data I/O
- Uses Burndy connector partnumber CELP2X80SC-3Z48

Description

The IBM family of 256KB and 512KB synchronous SRAM modules use IBM's burstable, high performance 0.5 micron, CMOS Static RAMs that are versatile and can achieve up to 5ns access using pipeline parts. The 512KB modules integrate four 32K x 36 burst SRAMs while the 256KB version integrates two 32K x 36 burst SRAMs. The burst mode operation of these modules supports i486/Pentium.

A 8K x 8 SRAM functions as a Tag RAM for every 256KB of data RAM.

The module pinout supports burst, pipelined burst and asynchronous SRAM options, including byte-write and global write features of 32K x 32 burst SRAM (in development).

The module is operated with dual +3.3V and +5V power supplies. Inputs and outputs are 5V tolerant and LVTTL compatible.

50H7428
SA14-4702-02
Revised 3/96

Connector Pin Assignment

GND	81	1	GND
TIO1	82	2	TIO0
TIO7	83	3	TIO2
TIO5	84	4	TIO6
TIO3	85	5	TIO4
RSVD	86	6	RSVD
VCC5	87	7	VCC3
RSVD	88	8	$\overline{\text{TWE}}$
$\overline{\text{CADV}}$/CAA4	89	9	$\overline{\text{CADS}}$/CAA3
GND	90	10	GND
$\overline{\text{COE}}$	91	11	$\overline{\text{CWE4}}$
$\overline{\text{CWE5}}$	92	12	$\overline{\text{CWE6}}$
$\overline{\text{CWE7}}$	93	13	$\overline{\text{CWE0}}$
$\overline{\text{CWE1}}$	94	14	$\overline{\text{CWE2}}$
VCC5	95	15	VCC3
$\overline{\text{CWE3}}$	96	16	$\overline{\text{CCS}}$/CAB4
CAB3	97	17	$\overline{\text{GWE}}$
CALE	98	18	$\overline{\text{BWE}}$
GND	99	19	GND
RSVD	100	20	A3
A4	101	21	A7
A6	102	22	A5
A8	103	23	A11
A10	104	24	A16
VCC5	105	25	VCC3
A17	106	26	A18
GND	107	27	GND
A9	108	28	A12
A14	109	29	A13
A15	110	30	$\overline{\text{ADSP}}$
RSVD	111	31	$\overline{\text{ECS1}}$/($\overline{\text{CS}}$)
PD0	112	32	$\overline{\text{ECS2}}$
PD2	113	33	PD1
PD4	114	34	PD3
GND	115	35	GND
CLK0	116	36	CLK1
GND	117	37	GND
D63	118	38	D62
VCC5	119	39	VCC3
D61	120	40	D60
D59	121	41	D58
D57	122	42	D56
GND	123	43	GND
D55	124	44	D54
D53	125	45	D52
D51	126	46	D50
D49	127	47	D48
GND	128	48	GND
D47	129	49	D46
D45	130	50	D44
D43	131	51	D42
VCC5	132	52	VCC3
D41	133	53	D40
D39	134	54	D38
D37	135	55	D36
GND	136	56	GND
D35	137	57	D34
D33	138	58	D32
D31	139	59	D30
VCC5	140	60	VCC3
D29	141	61	D28
D27	142	62	D26
D25	143	63	D24
GND	144	64	GND
D23	145	65	D22
D21	146	66	D20
D19	147	67	D18
VCC5	148	68	VCC3
D17	149	69	D16
D15	150	70	D14
D13	151	71	D12
GND	152	72	GND
D11	153	73	D10
D9	154	74	D8
D7	155	75	D6
VCC5	156	76	VCC3
D5	157	77	D4
D3	158	78	D2
D1	159	79	D0
GND	160	80	GND

Pin Definition and Description

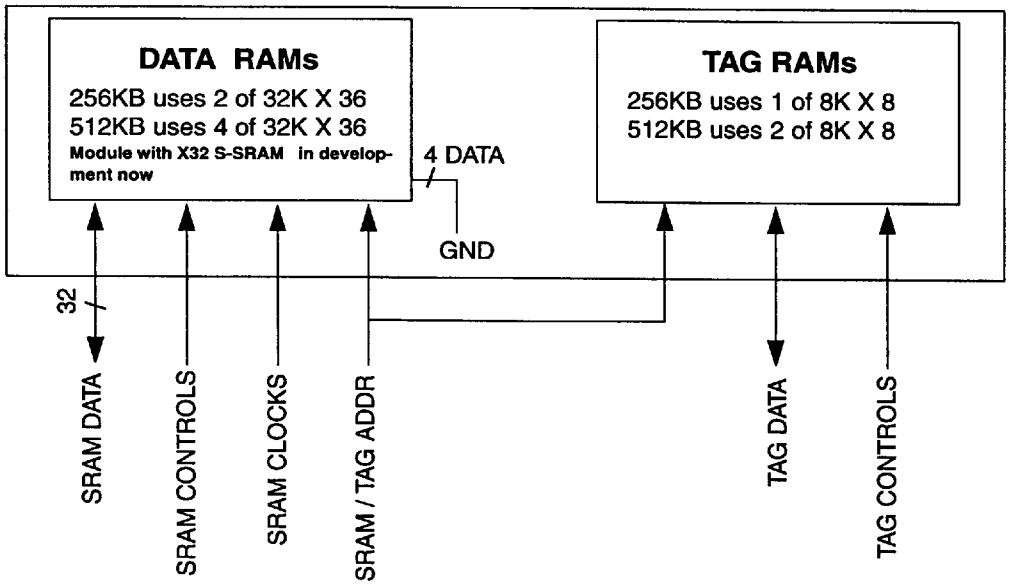
Signal	I/O	Number of Pins	Description
A3-A18	I	16	Address inputs; A3-A18 S-SRAM addresses; A5-A18 A-SRAM addresses
D0-D63	I/O	64	Cache data inputs/outputs
PD0-PD4	O	5	Presence detect pins
$\overline{CWE0}$-$\overline{CWE7}$	I	8	Write enable inputs
$\overline{TIO0}$-$\overline{TIO7}$	I	8	Tag inputs/outputs
$\overline{ECS1}$/($\overline{CS}$)-$\overline{ECS2}$	I	2	Expansion chip select inputs; NC (No Connect) on IBM14N32642 & IBM14N64642 $\overline{ECS1}$ used as $\overline{CS}$ & $\overline{ECS2}$ is NC on IBM14N32646
$\overline{CADS}$/CAA3	I	1	Controller address status (burst SRAM only/)/Address A3 (1st copy; A-SRAM only)
$\overline{CADV}$/CAA4	I	1	Burst address advance (burst SRAM only)/Address A4 (1st copy; A-SRAM only)
$\overline{CCS}$/CAB4	I	1	Chip enable (burst SRAM only)/Address A4 (2nd copy; A-SRAM only)
$\overline{COE}$	I	1	Burst data output enable
$\overline{ADSP}$	I	1	Processor address status (burst SRAM only)
$\overline{BWE}$	I	1	Byte write enable input (burst SRAM only)
$\overline{GWE}$	I	1	Global write enable input (burst SRAM only)
$\overline{TWE}$	I	1	Tag write enable input
CAB3	I	1	Address A3 (2nd copy; A-SRAM only)
CALE	I	1	Address latch enable input (A-SRAM only)
RSVD	I	5	Reserved
CLK0-CLK1	I	2	Clock inputs (burst SRAM only)
GND	I	24	Ground.
VCC3	I	8	+3.3V Power Supply.
VCC5	I	8	+5V Power Supply.

Ordering Information

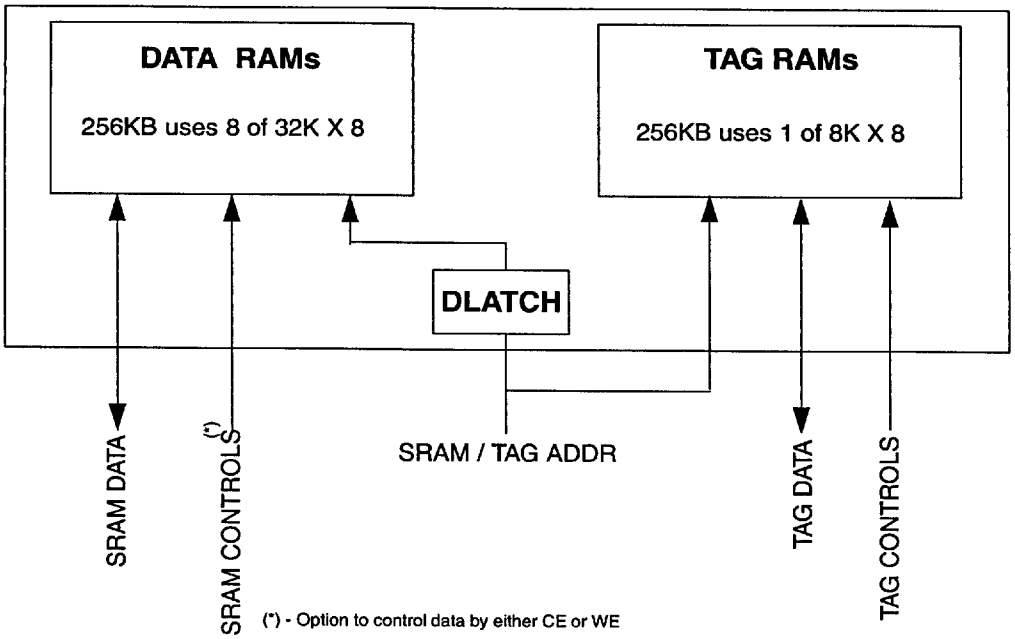
Part Number	Organization	Speed	Leads	Type	Availability
IBM14N32643FPA-9	32K x 64	9 ns Access / 15 ns Cycle	160	Pentium	Now
IBM14N32643FPA-11	32K x 64	11 ns Access / 15 ns Cycle	160	Pentium	Now
IBM14N32646BPA-12	32K x 64	12 ns Access / 15 ns Cycle	160	Async	Now
IBM14N64643FPA-9	64K x 64	9 ns Access / 15 ns Cycle	160	Pentium	Now
IBM14N64643FPA-11	64K x 64	11 ns Access / 15 ns Cycle	160	Pentium	Now
IBM14N64646CPA-12	64K x 64	12 ns Access / 15 ns Cycle	160	Async	On request

Block Diagram

Synchronous module (256KB & 512KB):



Asynchronous module (256KB):



Burst Sequence Truth Table (Interleave Burst)

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(0,0)	(1,1)	(1,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(1,0)	(0,1)	(0,0)

Presence Detect Table

Part Number	Module Burst Type	Module Size	PD0	PD1	PD2	PD3	PD4
IBM14N32642FPA	Interleaved	256KB	GND	NC	GND	NC	GND
IBM14N64642FPA	Interleaved	512KB	GND	NC	NC	GND	GND
IBM14N32646BPA	Async	256KB	NC	GND	GND	NC	GND

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (3.3V)	V_{CC3}	-0.5 to 4.6	V	1
Power Supply Voltage (5V)	V_{CC5}	-0.5 to 7	V	1
Input Voltage	V_{IN}	-0.5 to 6.0	V	1, 2
Output Voltage	V_{OUT}	-0.5 to V_{CC3}+0.5	V	1, 2
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. See "Pin Definiton and Description" table on Page 5 for Input/Output voltage symbols and definitions.

Recommended DC Operating Conditions (T_A=0 to 70°C)

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	V_{CC3}	3.135	3.3	3.465	V	1, 4
Supply Voltage	V_{CC5}	4.75	5.0	5.25	V	1, 4
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
Output Current	I_{OUT}	—	5	8	mA	4

1. All voltages referenced to V_{SS}. All V_{DD} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)
4. Input Voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 nanosecond set-up and hold times.

Capacitance (T_A=0 to +70°C, V_{CC3}=3.3V ± 5%, V_{CC5}=5V ± 5%, f=1MHz) Maximum values

IBM14N32642FPA and IBM14N64642FPA					
Parameter	Symbol	Test Condition	256KB	512KB	Units
Input Capacitance (Address)	C_{IN1}	V_{IN} = 0V	15	25	pF
Input Capacitance (Control, $\overline{CE}$, $\overline{OE}$)	C_{IN2}	V_{IN} = 0V	15	20	pF
Input Capacitance ($\overline{WE}$, CLK)	C_{IN3}	V_{IN} = 0V	7	12	pF
Data I/O Capacitance (DQ0-DQ71)	C_{OUT}	V_{OUT} = 0V	10	10	pF

Capacitance (T_A=0 to +70°C, V_{CC3}=3.3V ± 5%, V_{CC5}=5V ± 5%, f=1MHz) Maximum values

IBM14N32646BPA					
Parameter		Symbol	Test Condition	256KB	Units
Input Capacitance (Address)	A3, A4	C_{IN1}	V_{IN} = 0V	35	pF
	All others			10	
Input Capacitance ($\overline{CE}$, $\overline{OE}$)		C_{IN2}	V_{IN} = 0V	64	pF
Input Capacitance ($\overline{WE}$)		C_{IN3}	V_{IN} = 0V	10	pF
Data I/O Capacitance (DQ0-DQ71)		C_{OUT}	V_{OUT} = 0V	10	pF

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC3}=3.3V ± 5%, V_{CC5}=5V ± 5%)

IBM14N32642FPA and IBM14N64642FPA						
Parameter		Symbol	Min.	Max.	Units	Notes
Operating Current @ 3.3V / 5.0V Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	IBM14N32642FPA	I_{DD15}		550 / 150	mA	1
	IBM14N64642FPA			1100 / 300		
Standby Current @ 3.3V / 5.0V Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}, All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	IBM14N32642FPA	I_{SB}		50 / 20	mA	1
	IBM14N64642FPA			100 / 40		
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	IBM14N32642FPA	I_{LI}		2	µA	
	IBM14N64642FPA			4		
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	IBM14N32642FPA	I_{LO}		2	µA	
	IBM14N64642FPA			4		
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)		V_{OH}	2.4		V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)		V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

DC Electrical Characteristics (T_A= 0 to +70°C, V_{CC3}=3.3V ± 5%,V_{CC5}=5V ± 5%)

IBM14N32646BPA					
Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current @ 3.3V / 5.0V Maximum Power Supply Operating Current (Maximum V_{CC3} and V_{CC5}, I_{out} = 0)	I_{CC12}		480 / 150	mA	1
Standby Current @ 3.3V / 5.0V Power Supply Standby Current (Maximum V_{CC3} and V_{CC5}, $V_{IH} \leq \overline{CS}$; All other inputs = V_{IH} or V_{IL}; I_{out}= 0)	I_{SB}		40 / 20	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{CC})	I_{LI}		40	µA	
Output Leakage Current (V_{OUT} =0 &V_{CC}, $\overline{OE}$ = V_{IH})	I_{LO}		40	µA	
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

AC Characteristics (T_A=0 to +70°C, V_{CC5}=5.0V ± 5%, Units in nsec)

Parameter	Symbol	-9		-11		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	15.0	—	15.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	9.0	—	11.0	3
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	3
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.5	1, 2, 3
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	1, 2, 3
Output Enable to High Z	t_{OHZ}	2.0	5.5	2.0	6.5	1, 3
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	1, 3
Output Enable to Output Valid	t_{OQ}	—	5.0	—	6.0	3

1. Transitions are measured ± 200 mV from steady state voltage.
2. At any given voltage and temperature, T_{CHZ} max is always less than T_{CLZ} min for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from HIZ to new RAM data.
3. See AC test loading figure on Page 12.

AC Test Loading

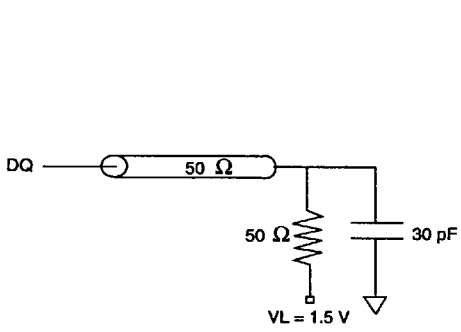


Fig. 1 Test Equivalent Load

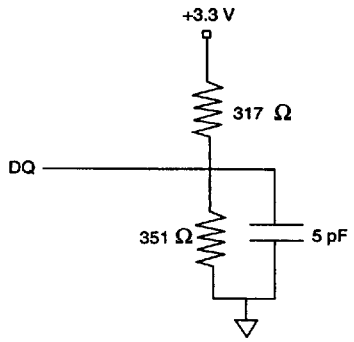
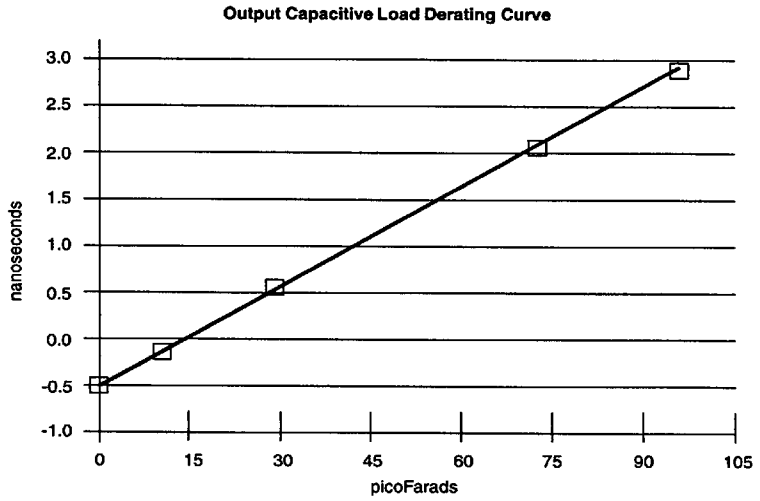
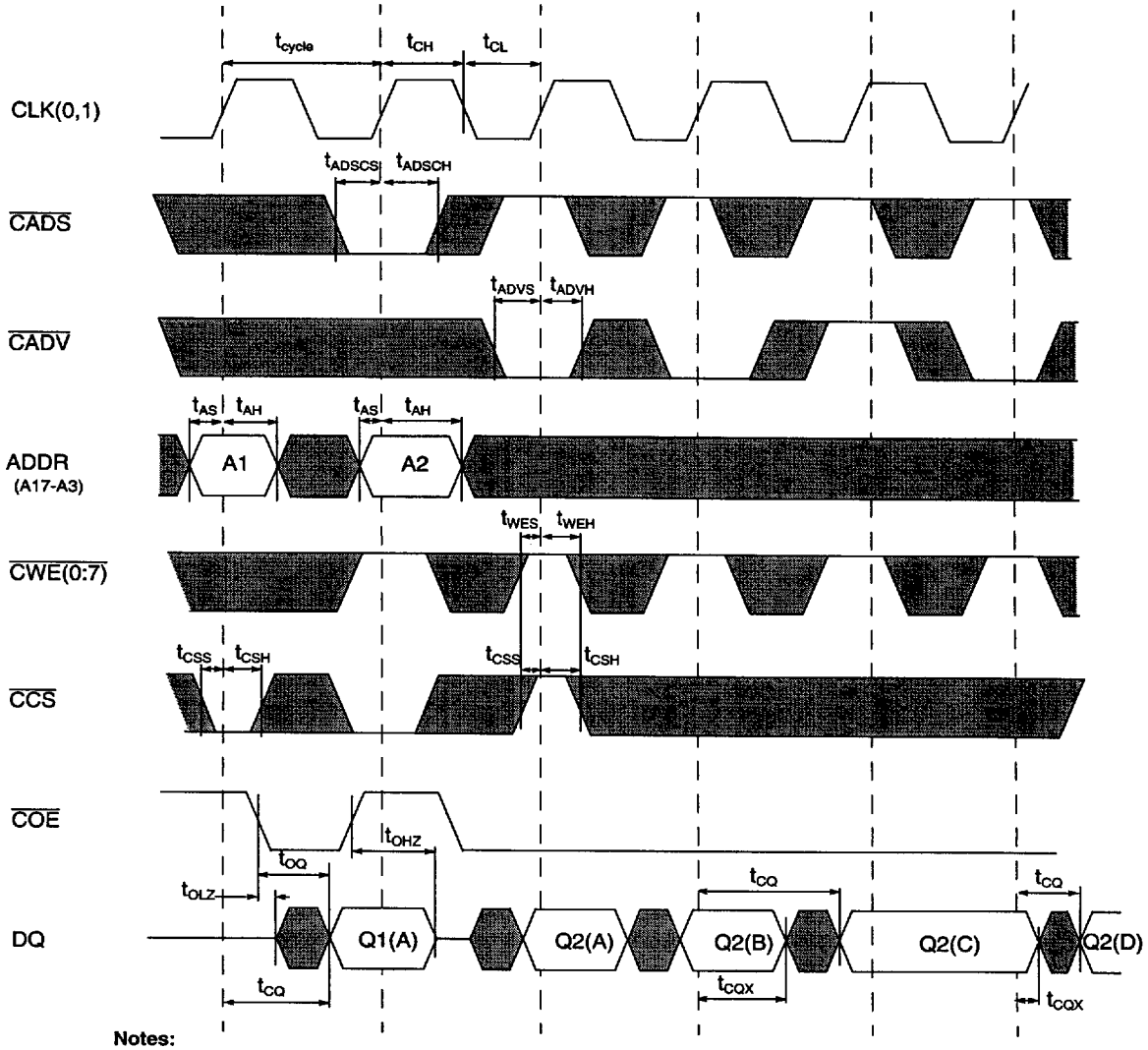


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access time guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters V_{cc} = 3.14 V, T_a = 70 °C.

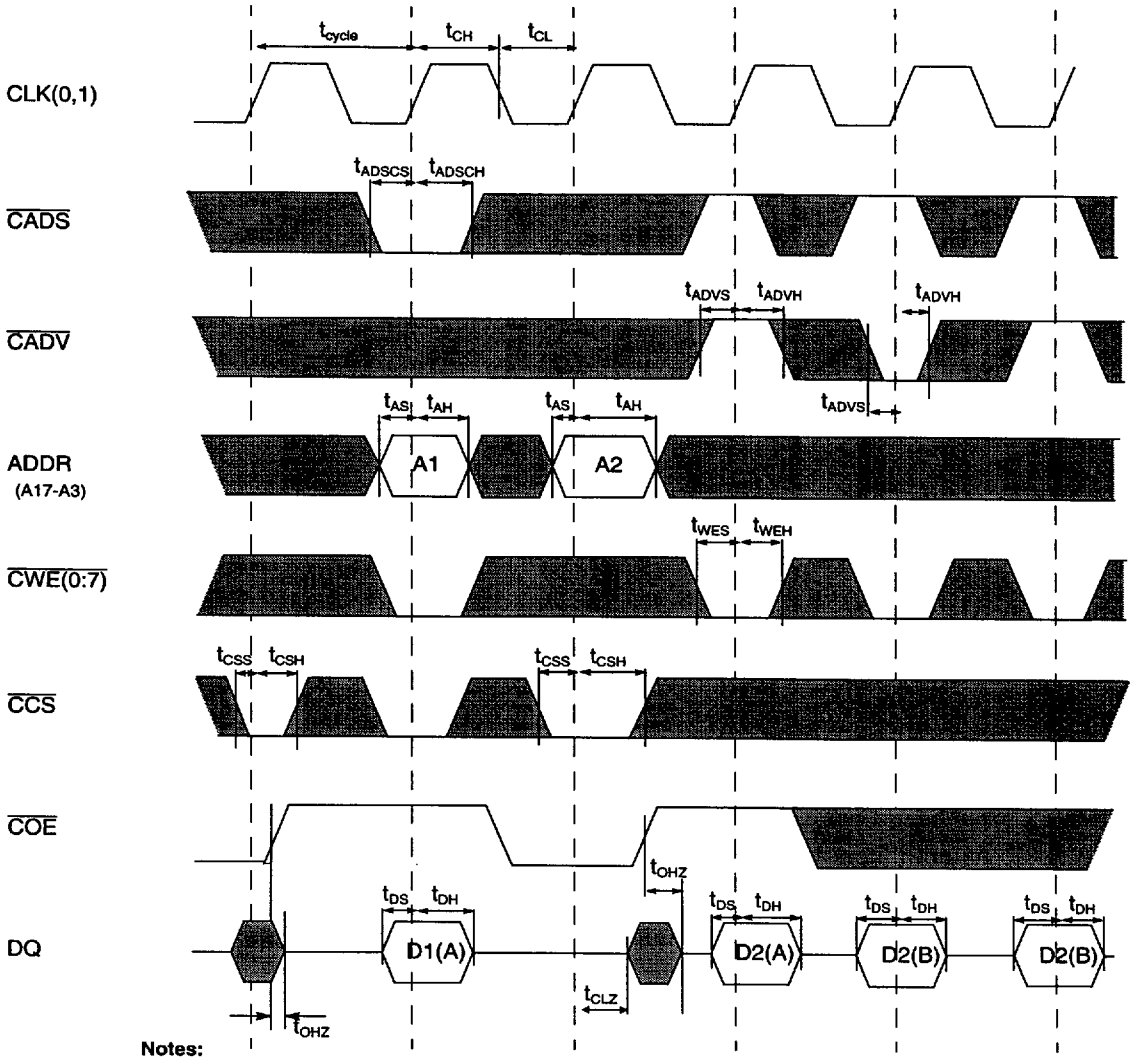
Synchronous SRAM Timing Diagram (Burst Read)



Notes:

1. Q1(A) and Q2(A) refer to output for Address A1 and A2 respectively.
2. Q2(B),Q2(C) and Q2(D) refer to output from subsequent internal burst counter addresses.

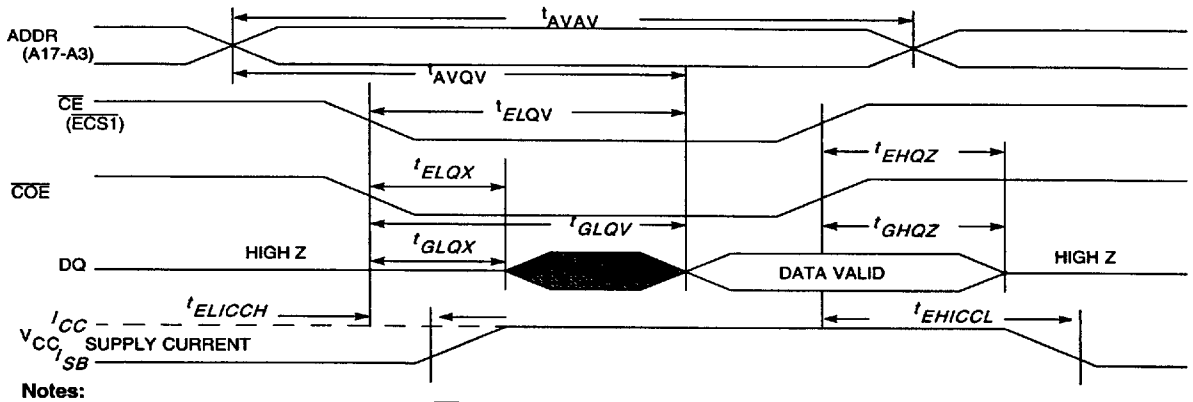
Synchronous SRAM Timing Diagram (Burst Write)



Notes:

1. D1(A) and D2(A) refer to data written to addresses A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.

Asynchronous SRAM Timing Diagram (Read)



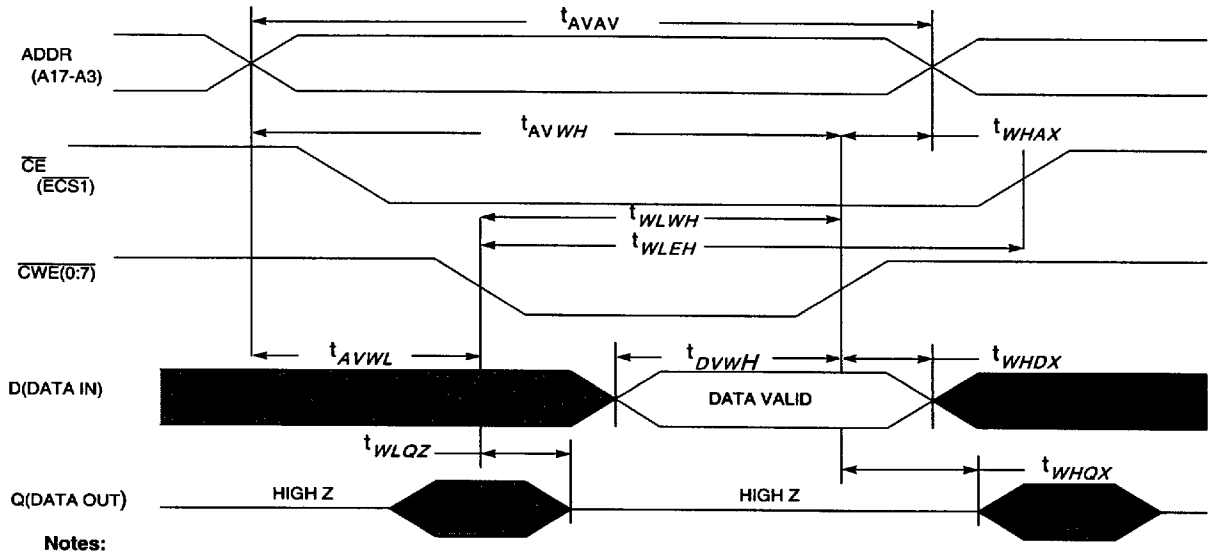
Notes:
.1. Addresses valid prior to or coincident with $\overline{CE}$ going low.

Read Cycle

Parameter	Symbol	Data		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{AVAV}	12		ns	2
Address Cycle Time	t_{AVQV}		12	ns	
Enable Access Time	t_{ELQV}		12	ns	3
Output Enable Access Time	t_{GLQV}		6	ns	
Output Hold from Address Change	t_{AXQX}	3		ns	4, 5, 6
Enable Low to Output Active	t_{ELQX}	4		ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	0	7	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0		ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	0	6	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0		ns	
Power Down Time	t_{EHICCL}		12	ns	

1. $\overline{CWE(0:7)}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{CE}$ going low
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mv from steady-state voltage.
6. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 1)



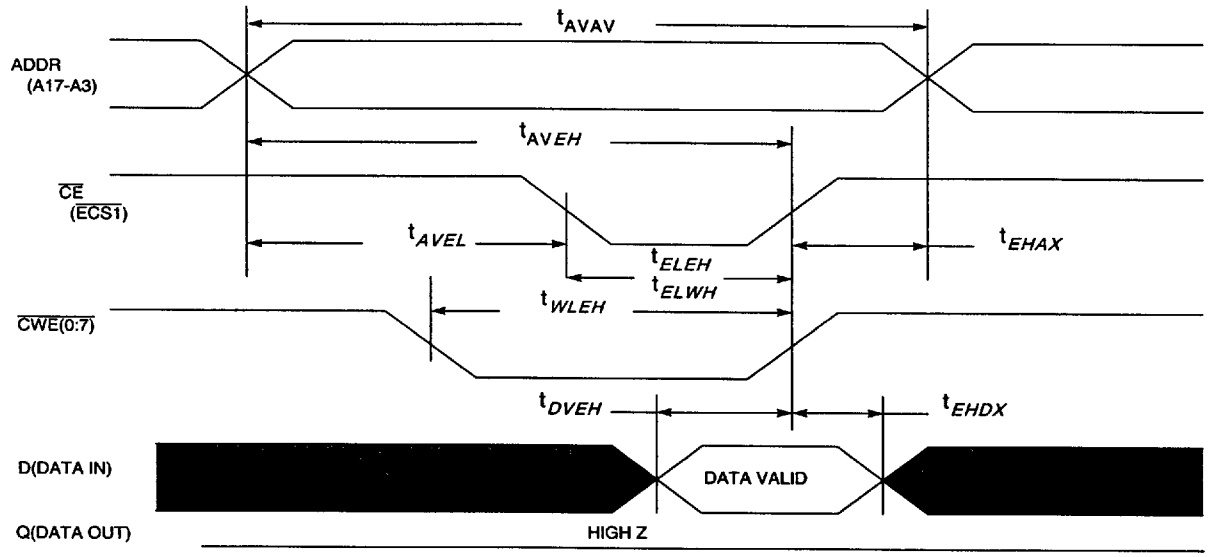
Notes:
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low..
2. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.

Write Cycle 1 ($\overline{WE}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	1
Address Setup Time	t_{AVWL}	0		ns	
Address Valid to End of Write	t_{AVWH}	10		ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	10		ns	
Write Pulse Width $\overline{G}$ High	t_{WLWH} t_{WLEH}	9		ns	2
Data Valid to End of Write	t_{DVWH}	6		ns	
Data Hold Time	t_{WHDX}	0		ns	
Write Low to Output High-Z	t_{WLQZ}	0	6	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	2		ns	3, 4, 5
Write Recovery Time	t_{WHAX}	0		ns	

1. All timings are referenced from the last valid address to the first transitioning address.
2. If $V_{IH} \leq \overline{COE}$, the output will remain in a high impedance state
3. At any given voltage and temperature , t_{WLQZ} (max) < t_{WHQX} (min), both for a given device and from device to device.
4. Transition is measured ±500 mv from steady state voltage.
5. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 2)



Notes:
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low.

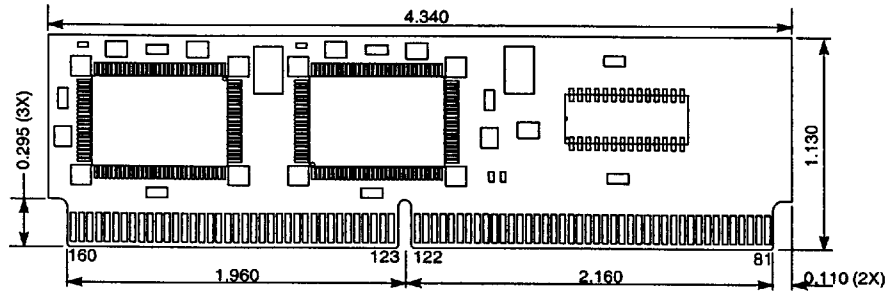
Write Cycle 2 ($\overline{OE}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	
Address Setup Time	t_{AVEL}	0		ns	
Address Valid to End of Write	t_{AVEH}	10		ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	9		ns	3, 4
Data Valid to End of Write	t_{DVEH}	6		ns	
Data Hold Time	t_{EHDX}	0		ns	
Write Recovery Time	t_{EHAX}	0		ns	

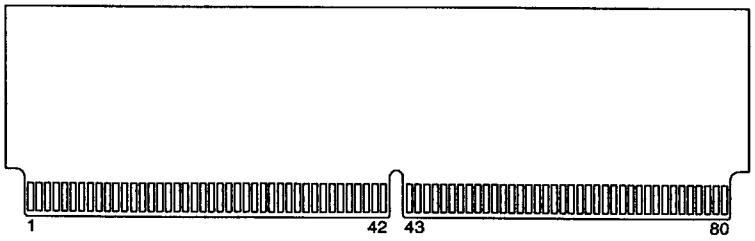
1. A write occurs during the overlap of $\overline{COE}$ low and $\overline{CWE}$ low
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{COE}$ goes low coincident with or after $\overline{CWE}$ goes low, the output will remain in a high impedance state.
4. If $\overline{COE}$ goes high coincident with or before $\overline{CWE}$ goes high, the output will remain in a high impedance state.

Layout Drawing - 256KB (32K x 64), 160-pin Synchronous module

Front View:



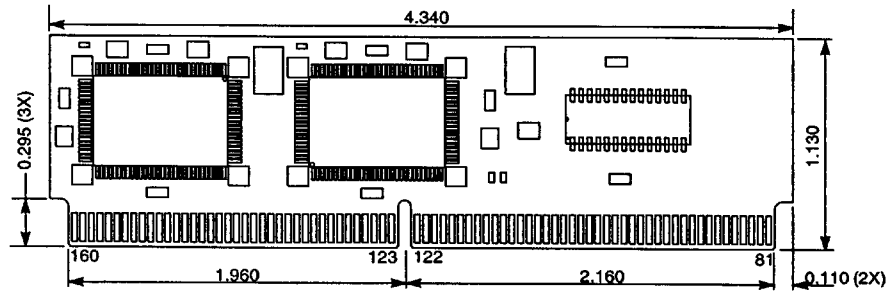
Back View:



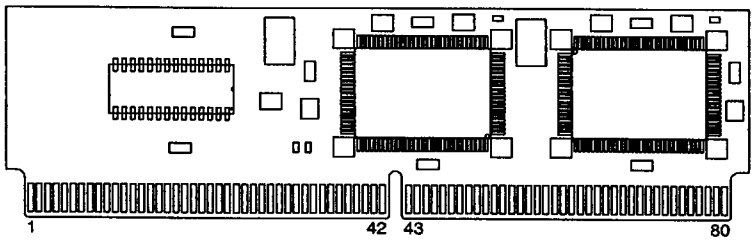
Uses Burndy connector partnumber CELP2X80SC-3Z48

Layout Drawing - 128KB (64K x 64), 160-pin Synchronous module

Front View:

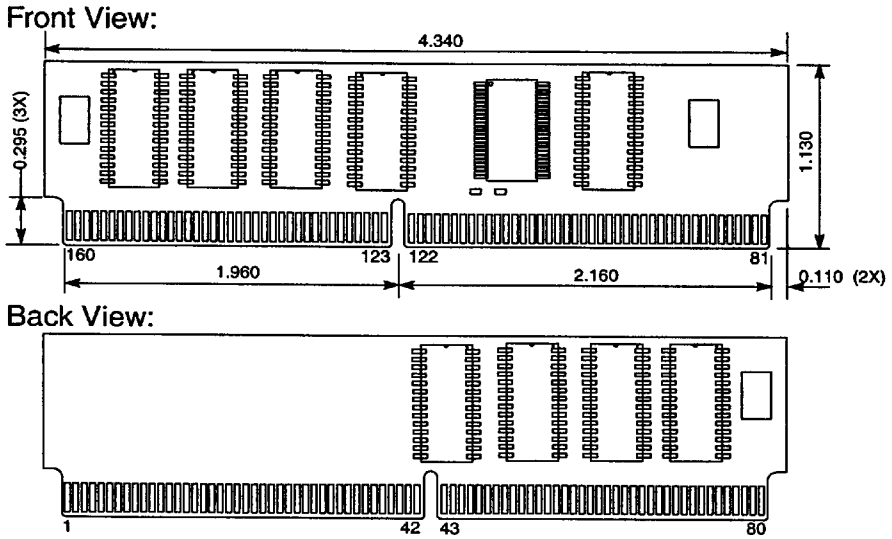


Back View:



Uses Burndy connector partnumber CELP2X80SC-3Z48

Layout Drawing - 256KB (32K x 64), 160-pin Asynchronous module



Uses Burndy connector partnumber CELP2X80SC-3Z48

Revision Log

Rev	Contents of Modification
10/95	Preliminary Release
12/95	Latest Release; EC # E21061; Dt 12/05/95
03/96	P/N correction; Dt 03/07/96