High-Performance SRAM Modules

Features

- 256K, 512K, and 1MB secondary cache module family using Synchronous and Asynchronous SRAMs.
- Organized as a 32K, 64K, or 128K x 72 package on a 4.3" x 1.1", 160-lead, Dual Read-out DIMM for SSRAM and 64K x 72 package for ASRAM
- Available in both interleaved (i486/Pentium™) and linear (PowerPC™) burst modes
- Operation for 50MHz to 66MHz supported
- Fast access times: 9 and 11ns using SSRAM; 12ns using ASRAM
- Byte Parity
- Individual Byte Write control
- Low capacitive address, control, clock, and data bus loading
- Single +3.3V or 5V, +/- 5% power supply
- 5V-tolerant common data I/O

Description

The IBM family of 256KB, 512KB, and 1MB synchronous SRAM modules uses IBM's burstable, high-performance 0.5-micron CMOS Static RAMs that are versatile and can achieve up to 9ns access. The 512KB modules integrate four 64K x 18 burst SRAMs. The burst-mode operation of these modules supports PowerPC-based systems and is available for either +3.3V or +5V applications. The 512KB ASRAM module offers a cost/performance optimization for +5V applications.

This IBM family of Cache modules supports operation up to 66MHZ. Outputs are 5V tolerant and LVTTL compatible. The Cache family is presently designed to support either Pentium or PowerPC-based controllers.

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Connector Pin Assignment

GND	81	1	GND
D63	82	2	D62
VCC5	83	3	VCC3.3
D61	84	4	D60
VCC5	85	5	VCC3.3
D59	86	6	D58
D57	87	7	D56
GND	88	8	GND
DP7	89	9	DP6
D55	90	10	D54
D53	91	11	D52
D51	92	12	D50
GND	93	13	GND
D49	94	14	D48
D47	95	15	D46
D45	96	16	D44
D43	97	17	D42
GND	98	18	GND
D41	99	19	D40
DP5	100	20	DP4
D39	101	21	D38
D37	102	22	D36
D35	103	23	D34
GND	104	24	GND
D33	105	25	D32
D31	106	26	D30
D29	107	27	D28
D27	108	28	D26
D25	109	29	D24
GND	110	30	GND
DP3	111	31	DP2
D23	112	32	D22
D21	113	33	D20
VCC5	114	34	VCC3.3
D19	115	35	D18
GND	116	36	GND
D17	117	37	D16
VCC5	118	38	VCC3.3
D15	119	39	D14
D13	120	40	D12
GND	121	41	GND
D11	122	42	D10
VCC5	123	43	VCC3.3
D9	124	44	D8
DP1	125	45	DP0
VCC5	126	46	VCC3.3
D7	127	47	D6
D5	128	48	D4
D3	129	49	D2
D1	130	50	D0
GND	131	51	GND
A0B	132	52	A0A
A1B	133	53	A1A
A2B	134	54	A2A
A3B	135	55	A3A
A4	136	56	A5
GND	137	57	GND
A6	138	58	A7
A8	139	59	A9
A10	140	60	A11
A12	141	61	A13
A14	142	62	A15
GND	143	63	GND
A16	144	64	PD0
PD1	145	65	PD2
CLK0	146	66	CLK1
CLK2	147	67	CLK3
GND	148	68	GND
$\overline{\text{WE7}}$	149	69	$\overline{\text{WE6}}$
$\overline{\text{WE5}}$	150	70	$\overline{\text{WE4}}$
$\overline{\text{WE3}}$	151	71	$\overline{\text{WE2}}$
$\overline{\text{WE1}}$	152	72	$\overline{\text{WE0}}$
GND	153	73	GND
$\overline{\text{ADSC1}}$	154	74	$\overline{\text{ADSC0}}$
$\overline{\text{CE1}}$	155	75	$\overline{\text{CE0}}$
$\overline{\text{ADV1}}$	156	76	$\overline{\text{ADV0}}$
$\overline{\text{OE1}}$	157	77	$\overline{\text{OE0}}$
VCC5	158	78	VCC3.3
$\overline{\text{ADSP1}}$	159	79	$\overline{\text{ADSP0}}$
GND	160	80	GND

Pins 146, 147, 154, 156, 159, 66, 67, 74, 76, 79 are no connect for the asynchronous module version.

Pin Definition

A0 - A15	Address
D0 - D63	Data I/O
DP0 -DP7	Parity I/O
$\overline{CE0}$ - $\overline{CE1}$	Chip Enable
$\overline{WE0}$ - $\overline{WE7}$	Byte Write Enable
$\overline{OE0}$ - $\overline{OE1}$	Output Enable
$\overline{ADSP0}$ - $\overline{ADSP1}$	Address Status Processor
$\overline{ADSC0}$ - $\overline{ADSC1}$	Address Status Controller
$\overline{ADV0}$ - $\overline{ADV1}$	Address Advance
CLK0 - CLK3	Clock
PD0 - PD2	Presence Detect
GND	Ground
VCC	Power Supply

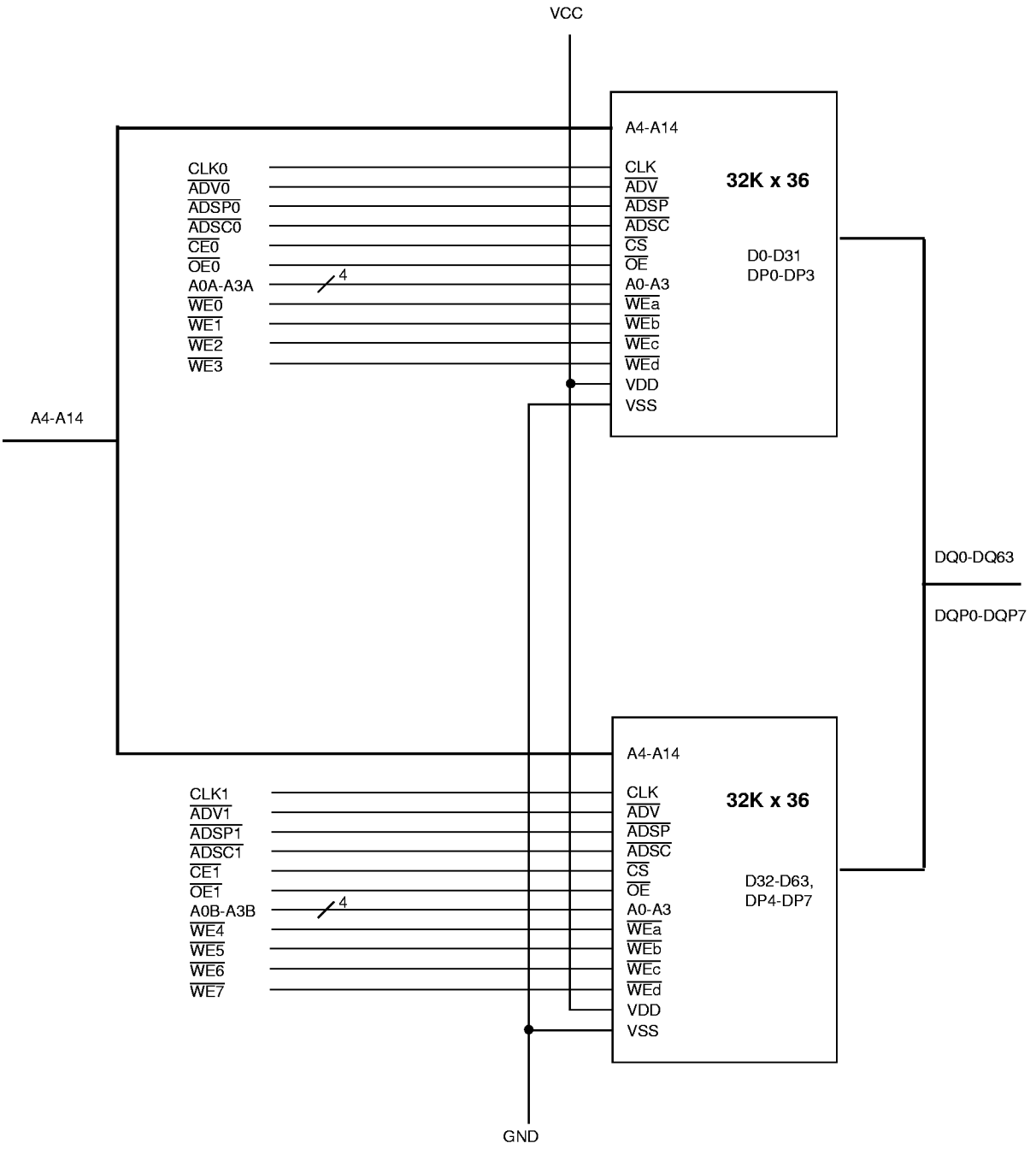
Pin Description

Signal	I/O	Level	Description
A0-A15	I	N/A	Address inputs. These inputs are registered at the rising edge of CLK if $\overline{ADSP}$ or $\overline{ADSC}$ is LOW.
D0-D15	I/O	N/A	Data I/O. The 64 bit data bus is divided into 8 bytes: D(0:7), D(8:15), D(16:23), D(24:31), D(32:39), D(40:47), D(48:55), D(56:63). D(0:7) is the least significant byte and D(56:63) is the most significant byte. The direction of the data pins is controlled by $\overline{OE}$.
DP0-DP7	I/O	N/A	Data Parity I/O. These are the data parity bits for the data bus. DQP0 applies to D(0:7) and DQP7 applies to D(56:63).
$\overline{CE0}$-$\overline{CE1}$	I	LOW	Chip enable. These lines are used to enable or disable the module. They can also be used to block $\overline{ADSP}$.
$\overline{WE0}$-$\overline{WE7}$	I	LOW	Byte write enables. These lines allow individual bytes to be written to the module. $\overline{WE0}$ controls DQ0-DQ7 and DQP0, $\overline{WE1}$ controls DQ8-DQ15 and DQP1, etc.
$\overline{OE0}$-$\overline{OE1}$	I	LOW	Output enable. These are asynchronous inputs which enable the data I/O drivers when active.
$\overline{ADSP0}$-$\overline{ADSP1}$	I	LOW	Address Status Processor. When this input and/or $\overline{ADSC}$ is active, a new external address will be latched thus interrupting any ongoing burst. If both $\overline{ADSP}$ and $\overline{ADSC}$ are active at the same time (at the rising edge of CLK), only $\overline{ADSP}$ will be recognized. $\overline{ADSP}$ is ignored when $\overline{CE}$ is HIGH.
$\overline{ADSC0}$-$\overline{ADSC1}$	I	LOW	Address Status Controller. When this input and/or $\overline{ADSP}$ is active, a new external address will be latched thus interrupting any ongoing burst. A read or write is performed using the new address if all chip enables are active.
$\overline{ADV0}$-$\overline{ADV1}$	I	LOW	Address Advance. The input is used to automatically increment the internal burst address counter. Depending on the module type, the burst sequence can be either linear (Power-PC based) or interleaved (Pentium/486) based.
CLK(0:3)	I	N/A	Clock. This signal is used to latch the address, data (store), $\overline{ADSP}$, $\overline{ADSC}$, $\overline{CE}$, $\overline{WE}$, and $\overline{ADV}$. All synchronous inputs must meet setup and hold times around the clock's rising edge.
GND	I	N/A	Ground.
VCC3.3 or VCC5	I	N/A	Power Supply: +3.3V (Synchronous modules) or +5.0V (Asynchronous module)

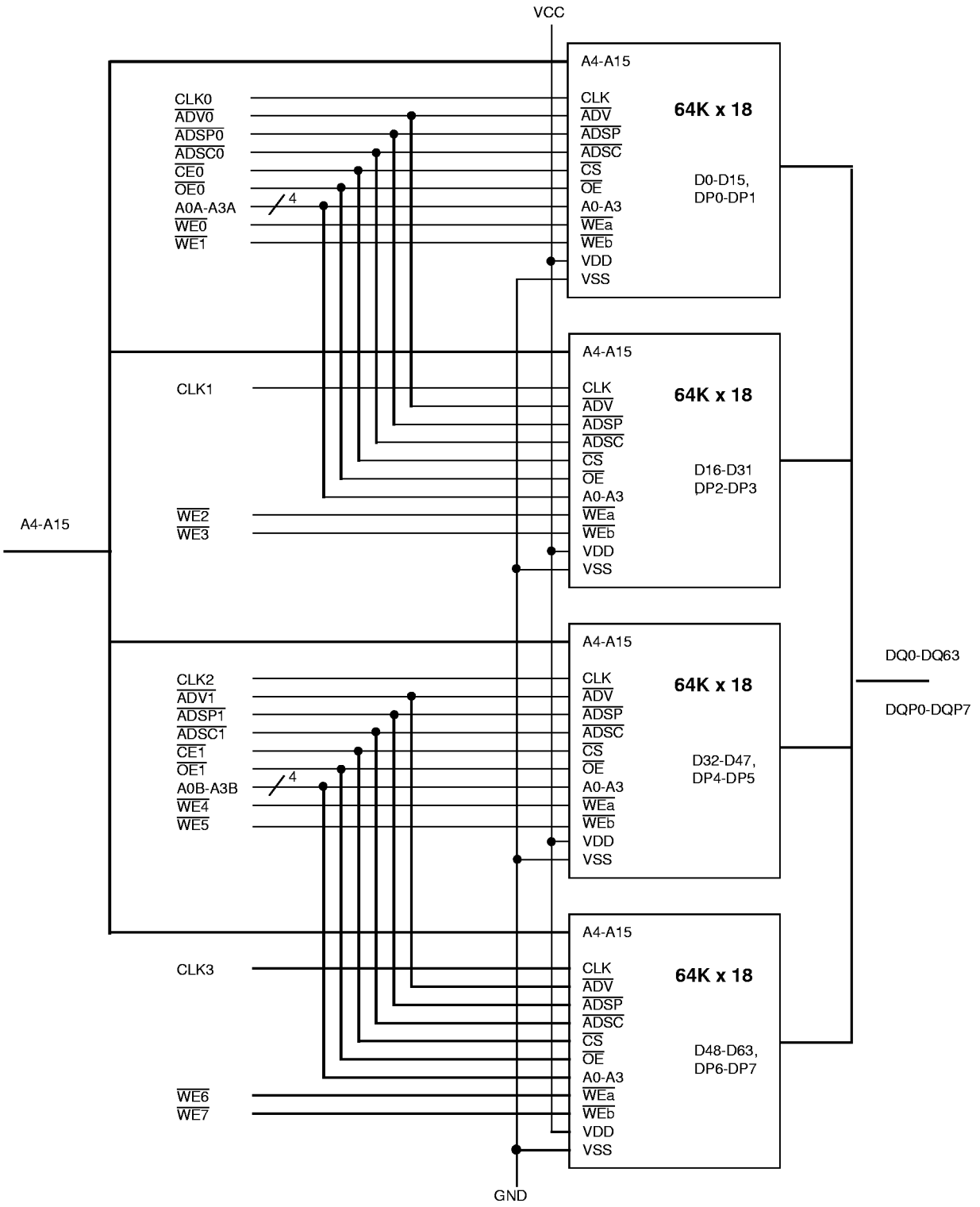
Ordering Information

Part Number	Organization	Speed	Availability	Type
IBM14N32722FPA-9	32K x 72	9 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N32722FPA-11	32K x 72	11 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N64722DPA-9	64K x 72	9 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N64722DPA-11	64K x 72	11 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N13722DPA-9	128K x 72	9 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N13722DPA-11	128K x 72	11 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N32724FPA-9	32K x 72	9 ns Access / 15 ns Cycle	On Request	PowerPC
IBM14N32724FPA-11	32K x 72	11 ns Access / 15 ns Cycle	On Request	PowerPC
IBM14N64724DPA-9	64K x 72	9 ns Access / 15 ns Cycle	Now	PowerPC
IBM14N64724DPA-11	64K x 72	11 ns Access / 15 ns Cycle	Now	PowerPC
IBM14N13724DPA-9	128K x 72	9 ns Access / 15 ns Cycle	Now	PowerPC
IBM14N13724DPA-11	128K x 72	11 ns Access / 15 ns Cycle	Now	PowerPC
IBM14N13722DPB-9	128K X 72	9 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N13722DPB-11	128K X 72	11 ns Access / 15 ns Cycle	On Request	Pentium
IBM14N13724DPB-9	128K X 72	9 ns Access / 15 ns Cycle	On Request	PowerPC
IBM14N13724DPB-11	128K X 72	11 ns Access / 15 ns Cycle	On Request	PowerPC
IBM14N64726GAA-12	64K x 72	12 ns Access / 15 ns Cycle	On Request	Asynch.

Block Diagram: Synchronous module 32K x 72

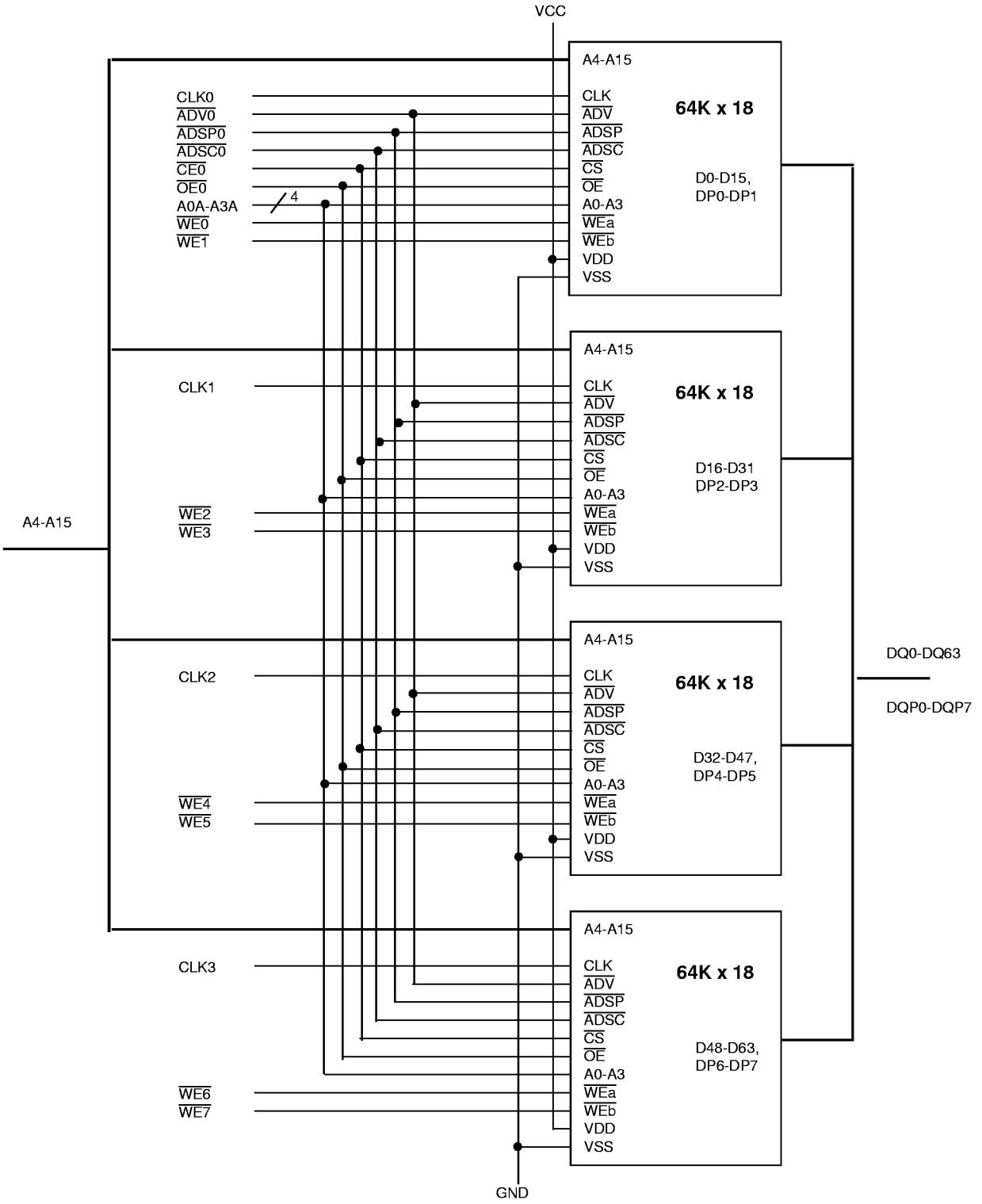


Block Diagram: Synchronous module 64K x 72



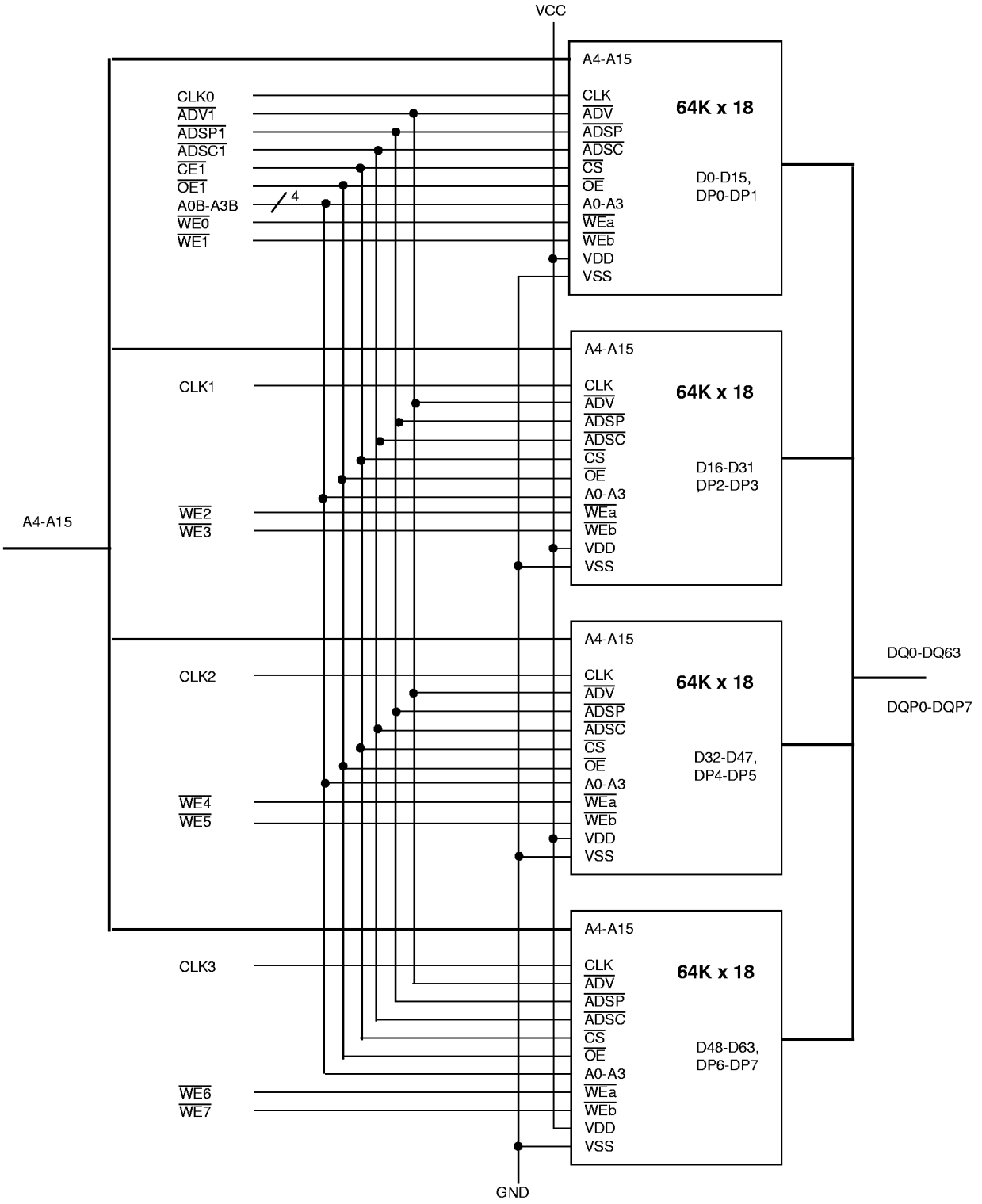
Block Diagram: Synchronous module 128K x 72 - Front Side

Note: The following nets are dotted front to back: WE0 through WE7, CLK0 through CLK3, DQ0 through DQ63, DQP0 through DQP7



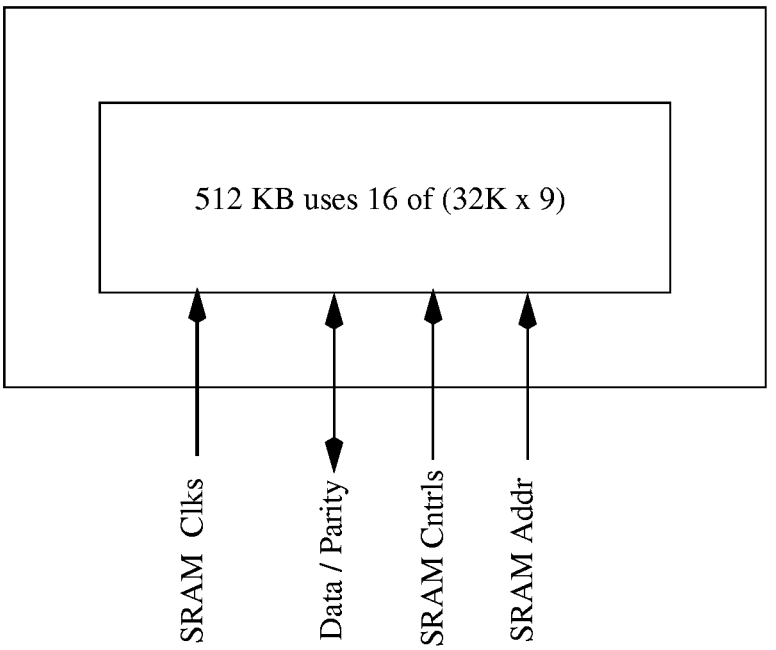
Block Diagram: Synchronous module 128K x 72 - Back Side

Note: The following nets are dotted front to back: WE0 through WE7, CLK0 through CLK3, DQ0 through DQ63, DQP0 through DQP7



Block Diagram: Asynchronous module 64K x 72

Asynchronous module (512KB)



Burst Sequence Truth Table Synchronous modules, interleave burst

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(0,0)	(1,1)	(1,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(1,0)	(0,1)	(0,0)

Burst Sequence Truth Table Synchronous modules, linear burst

External Address	A15-A2	(A1,A0)			
		(0,0)	(0,1)	(1,0)	(1,1)
1st Access	A15-A2	(0,0)	(0,1)	(1,0)	(1,1)
2nd Access	A15-A2	(0,1)	(1,0)	(1,1)	(0,0)
3rd Access	A15-A2	(1,0)	(1,1)	(0,0)	(0,1)
4th Access	A15-A2	(1,1)	(0,0)	(0,1)	(1,0)

Presence Detect Table

Part Number	Module Burst Type	Module Size	PD0	PD1	PD2
IBM14N32722FPA	Interleaved	256KB	N.C.	GND	GND
IBM14N64722DPA	Interleaved	512KB	GND	GND	GND
IBM14N13722DPA	Interleaved	1MB	GND	N.C.	GND
IBM14N32724FPA	Linear	256KB	N.C.	GND	N.C.
IBM14N64724DPA	Linear	512KB	GND	GND	N.C.
IBM14N13724DPA	Linear	1MB	GND	N.C.	N.C.
IBM14N64726GAA	Asynch	512KB	GND	GND	NC

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units	Notes
Power Supply Voltage (3.3V)	V_{CC3}	-0.5 to 4.6	V	1, 2
Power Supply Voltage (5.0V)	V_{CC5}	-0.5 to 7	V	1, 3
Input Voltage	V_{IN}	-0.5 to 6.0	V	1
Output Voltage	V_{OUT}	-0.5 to V_{CC3}+0.5	V	1
Operating Temperature	T_{OPR}	0 to +70	°C	1
Storage Temperature	T_{STG}	-55 to +125	°C	1
Power Dissipation	P_D	6.0	W	1, 2
Power Dissipation	P_D	8.0	W	1, 3
Short Circuit Output Current	I_{OUT}	50	mA	1

1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. For synchronous modules only.
3. For asynchronous module only.

Recommended DC Operating Conditions (TA=0 to 70 C) : Synchronous modules

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage	$V_{CC3.3}$	3.135	3.3	3.465	V	1, 4
Input High Voltage	V_{IH}	2.2	—	5.5	V	1, 2, 4
Input Low Voltage	V_{IL}	-0.3	—	0.8	V	1, 3, 4
Output Current	I_{OUT}	—	5	8	mA	4

1. All voltages referenced to V_{SS}. All V_{DD} and V_{SS} pins must be connected.
2. V_{IH}(Max)DC = 5.5 V, V_{IH}(Max)AC = 6.0 V (pulse width ≤ 4.0ns)
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -1.5 V (pulse width ≤ 4.0ns)
4. Input Voltage levels are tested to the following DC conditions: 1 microsecond cycle and 200 nanosecond set-up and hold times.

Capacitance (TA=0 to +70 C, VDD=3.3V 5%, f=1MHz) Maximum values: Synchronous modules

Parameter	Symbol	Test Condition	256KB	512KB	1MB	Units
Input Capacitance (Address)	C_{IN1}	V_{IN} = 0V	15	25	45	pF
Input Capacitance (Control, $\overline{CE}$, $\overline{OE}$)	C_{IN2}	V_{IN} = 0V	10	15	25	pF
Input Capacitance ($\overline{WE}$, CLK)	C_{IN3}	V_{IN} = 0V	10	10	15	pF
Data I/O Capacitance (DQ0-DQ71)	C_{OUT}	V_{OUT} = 0V	10	10	15	pF

DC Electrical Characteristics (TA= 0 to +70 C, VDD=3.3V 5%): Synchronous modules

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current Average Power Supply Operating Current ($\overline{OE}$ = V_{IH}, I_{OUT} = 0)	I_{DD10} I_{DD12}	---	900	mA	1
Standby Current Power Supply Standby Current ($\overline{CS2}$ = V_{IH}, CS2 = V_{IL}All other inputs = V_{IH} or V_{IL}, $I_{OUT.}$ = 0, CLK at 100MHz)	I_{SB}	---	100	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{DD})	I_{LI}	---	8	µA	
Output Leakage Current (V_{OUT} =0 &V_{DD}, $\overline{OE}$ = V_{IH})	I_{LO}	---	8	µA	
Output High Level Output “H” Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4	---	V	
Output Low Level Output “L” Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}	---	0.4	V	

1. I_{OUT} = Chip Output Current

Recommended DC Operating Conditions (TA=0 to 70 C): Asynchronous Module

Parameter	Symbol	Min.	Typ.	Max.	Units	Notes
Supply Voltage (5.0V)	V_{CC}	4.75	5.0	5.25	V	1
Input High Voltage	V_{IH}	2.2	—	Vcc+0.3	V	1, 2
Input Low Voltage	V_{IL}	-0.5	—	0.8	V	1, 3
Output Current	I_{OUT}	—	-5	5	mA	

1. All voltages referenced to GND. All V_{CC} and GND pins must be connected.
2. V_{IH}(Max)= Vcc + 0.5
3. V_{IL}(Min)DC = - 0.3 V, V_{IL}(Min)AC= -2.0V (pulse width ≤ 20.0 ns.)

Capacitance (TA=0 to 70 C, VCC5=5V 5%, f=1MHz) Maximum values: Asynchronous Module

Parameter		Symbol	Test Condition	512KB	Units
Input Capacitance (Address)	A0... A3	C_{IN1}	V_{IN} = 0V	50	pF
	All others			100	
Input Capacitance ($\overline{CE}$, $\overline{OE}$)		C_{IN2}	V_{IN} = 0V	65	pF
Input Capacitance ($\overline{WE}$)		C_{IN3}	V_{IN} = 0V	18	pF
Data I/O Capacitance (DQ0-DQ71)		C_{OUT}	V_{OUT} = 0V	10	pF

DC Electrical Characteristics TA= 0 to +70 C, VCC5=5V 5%) : Asynchronous Module

Parameter	Symbol	Min.	Max.	Units	Notes
Operating Current @ 5.0V Maximum Power Supply Operating Current (Maximum V_{CC5}, I_{out} = 0)	I_{CC12}		1140	mA	1
Standby Current @ 5.0V Power Supply Standby Current (Maximum V_{CC5}, $V_{IH} \leq \overline{CS}$; All other inputs = V_{IH} or V_{IL}; I_{out}= 0)	I_{SB}		640	mA	1
Input Leakage Current Input Leakage Current, any input (V_{IN} = 0 &V_{cc})	I_{LI}		40	µA	
Output Leakage Current (V_{OUT} =0 &V_{cc}, $\overline{OE}$ = V_{IH})	I_{LO}		40	µA	
Output High Level Output "H" Level Voltage (I_{OH}=-8mA @ 2.4V)	V_{OH}	2.4		V	
Output Low Level Output "L" Level Voltage (I_{OL}=+8mA @ 0.4V)	V_{OL}		0.4	V	

1. I_{OUT} = Chip Output Current

AC Characteristics (TA=0 to +70 C, VDD=3.3V 5%, Units in nsec) Synchronous modules

Parameter	Symbol	-9		-11		Notes
		Min.	Max.	Min.	Max.	
Cycle Time	t_{CYCLE}	15.0	—	15.0	—	
Clock Pulse High	t_{CH}	3.0	—	3.0	—	
Clock Pulse Low	t_{CL}	3.0	—	3.0	—	
Clock to Output Valid	t_{CQ}	—	9.0	—	11.0	1
Address Status Controller Setup Time	t_{ADSCS}	2.5	—	2.5	—	
Address Status Controller Hold Time	t_{ADSCH}	0.5	—	0.5	—	
Address Status Processor Setup Time	t_{ADSPS}	2.5	—	2.5	—	
Address Status Processor Hold Time	t_{ADSPH}	0.5	—	0.5	—	
Advance Setup Time	t_{ADVS}	2.5	—	2.5	—	
Advance Hold Time	t_{ADVH}	0.5	—	0.5	—	
Address Setup Time	t_{AS}	2.5	—	2.5	—	
Address Hold Time	t_{AH}	0.5	—	0.5	—	
Chip Selects Setup Time	t_{CSS}	2.5	—	2.5	—	
Chip Selects Hold Time	t_{CSH}	0.5	—	0.5	—	
Write Enables Setup Time	t_{WES}	2.5	—	2.5	—	
Write Enables Hold Time	t_{WEH}	0.5	—	0.5	—	
Data In Setup Time	t_{DS}	2.5	—	2.5	—	
Data In Hold Time	t_{DH}	0.5	—	0.5	—	
Data Out Hold Time	t_{CQX}	3.0	—	3.0	—	1
Clock High to Output High Z	t_{CHZ}	—	5.0	—	5.5	1, 2, 3
Clock High to Output Active	t_{CLZ}	2.5	—	2.5	—	1, 2, 3
Output Enable to High Z	t_{OHZ}	2.0	5.5	2.0	6.5	1, 2
Output Enable to Low Z	t_{OLZ}	0.25	—	0.25	—	1, 2
Output Enable to Output Valid	t_{OQ}	—	5.0	—	6.0	1

1. See AC Test Loading figure on the next page.
2. Transitions are measured ± 200 mV from steady state voltage.
3. At any given voltage and temperature, T_{CHZ} max is always less than T_{CLZ} min for a given device and from device to device. For any read cycle preceded by a write or deselect cycle, the data bus will transition glitch-free from HIZ to new RAM data.

AC Test Loading

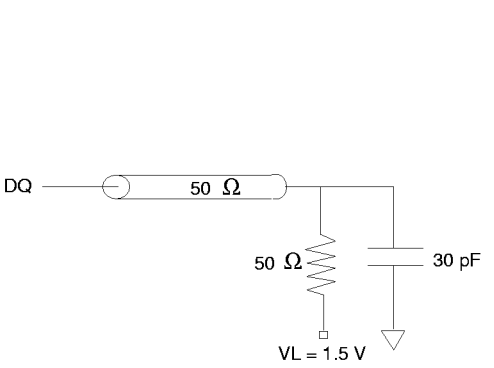


Fig. 1 Test Equivalent Load

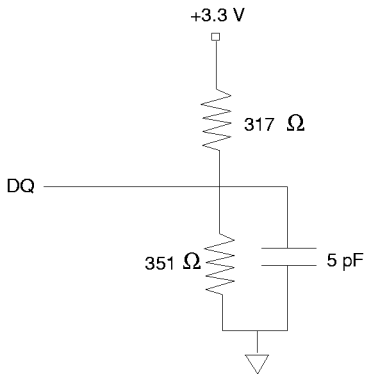
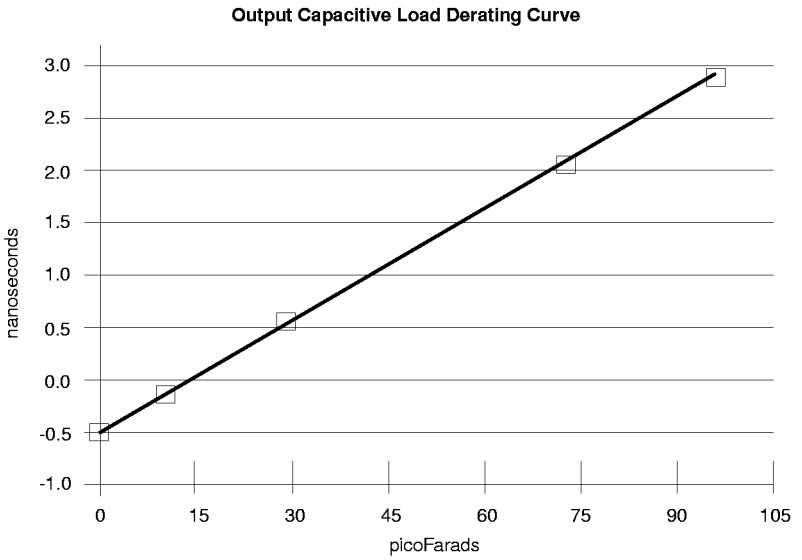
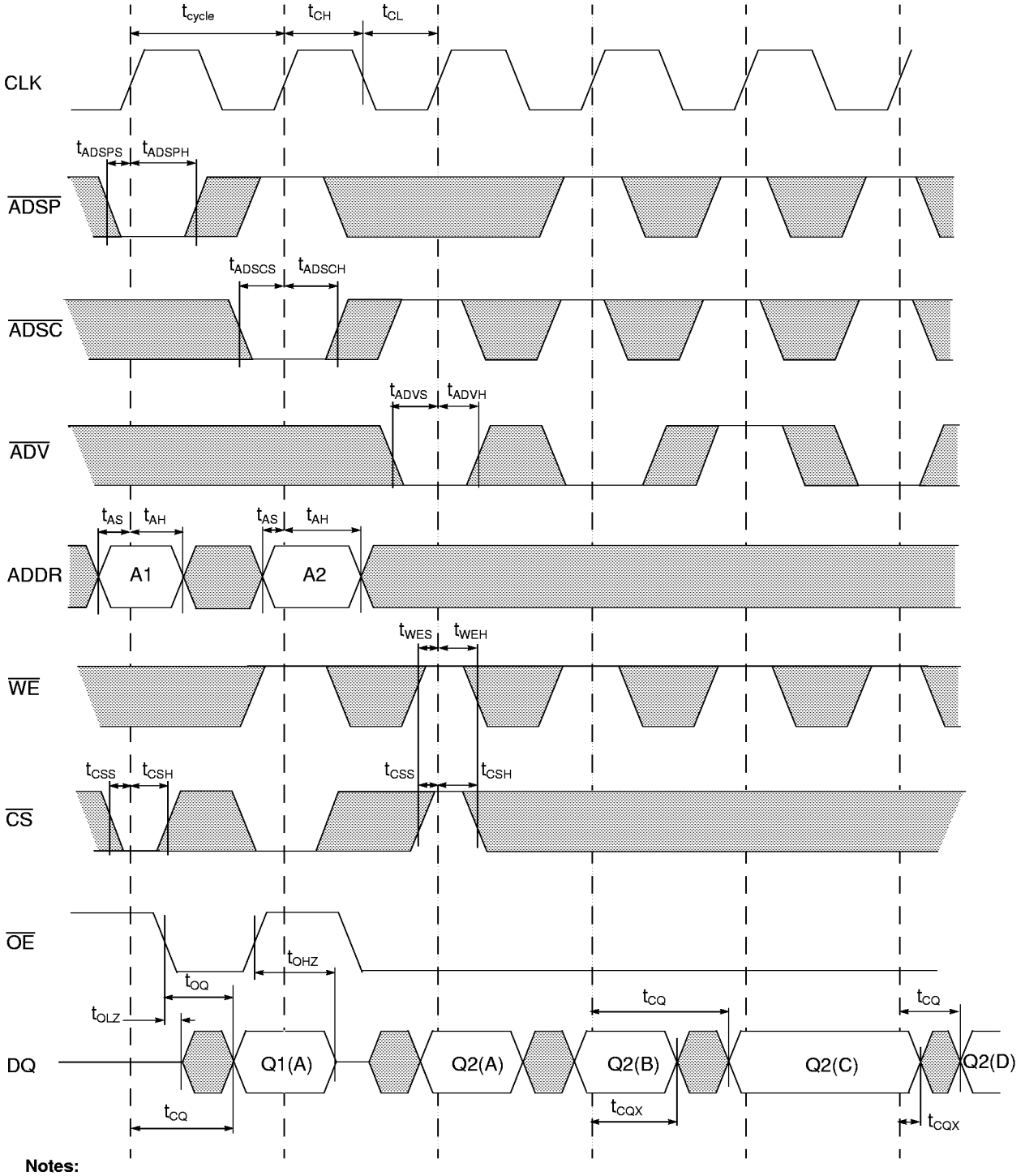


Fig. 2 Test Equivalent Load



The derating curve above is for a purely capacitive load on the output driver. For example, a part specified at 8ns access time will behave as though it has an 8.5 ns access time if a 30 pF load with no DC component was attached to the output driver. The access time guaranteed in the datasheets are based on a 50 ohm terminated test load. For unterminated loads the derating curve should be used. This curve is based on nominal process conditions with worst case parameters V_{CC} = 3.14 V, T_a = 70 °C.

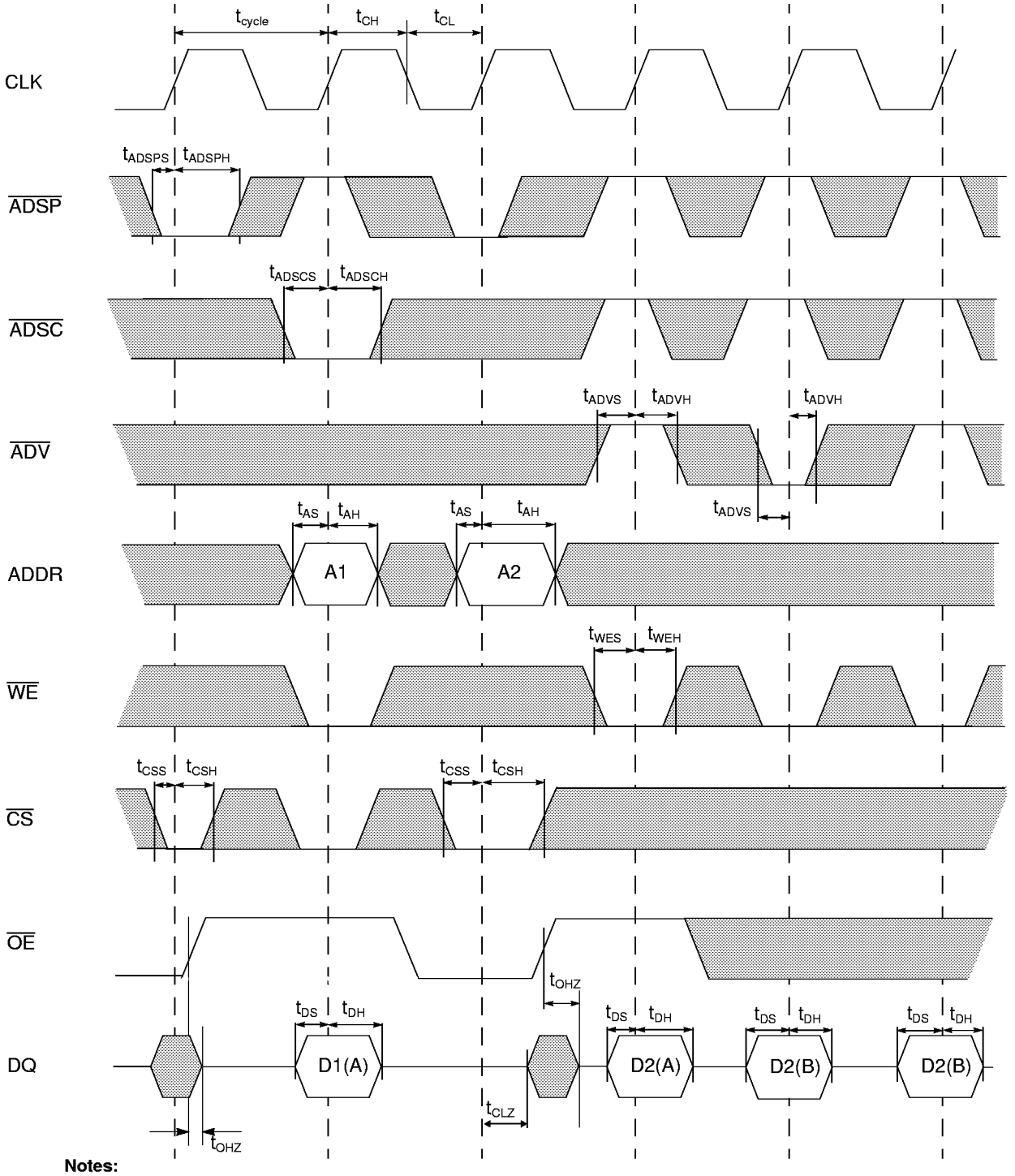
Synchronous SRAM Timing Diagram (Burst Read)



Notes:

1. Q1(A) and Q2(A) refer to output for Address A1 and A2 respectively.
2. Q2(B),Q2(C) and Q2(D) refer to output from subsequent internal burst counter addresses.

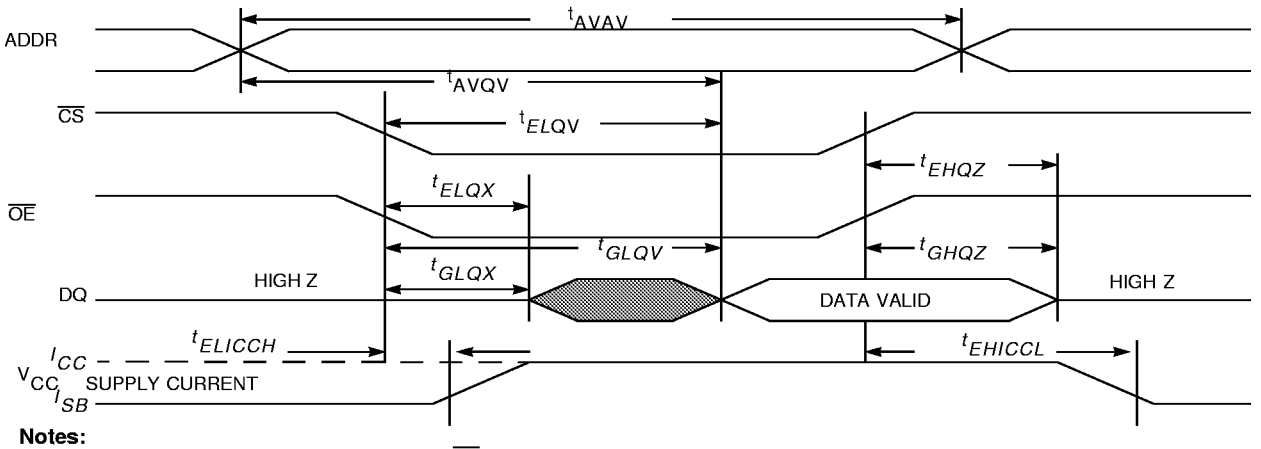
Synchronous SRAM Timing Diagram (Burst Write)



Notes:

1. D1(A) and D2(A) refer to data written to addresses A1 and A2.
2. D2(B) refers to data written to a subsequent internal burst counter address.
3. $\overline{WE}$ is a Don't Care when $\overline{ADSP}$ is sampled LOW.

Asynchronous SRAM Timing Diagram (Read)



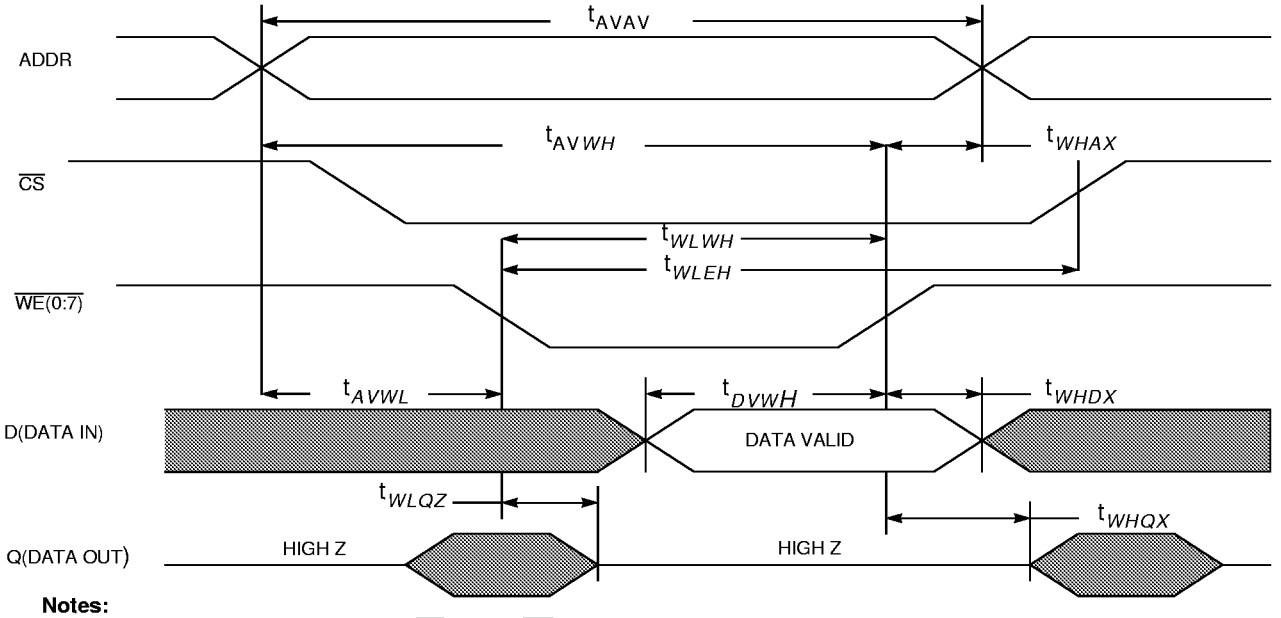
Notes:
1. Addresses valid prior to or coincident with $\overline{CE}$ going low.

Read Cycle

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Read Cycle Time	t_{AVAV}	12		ns	2
Address Cycle Time	t_{AVQV}		12	ns	
Enable Access Time	t_{ELQV}		12	ns	3
Output Enable Access Time	t_{GLQV}		6	ns	
Output Hold from Address Change	t_{AXQX}	3		ns	4, 5, 6
Enable Low to Output Active	t_{ELQX}	4		ns	4, 5, 6
Enable High to Output High-Z	t_{EHQZ}	0	7	ns	4, 5, 6
Output Enable Low to Output Active	t_{GLQX}	0		ns	4, 5, 6
Output Enable High to Output High-Z	t_{GHQZ}	0	6	ns	4, 5, 6
Power Up Time	t_{ELICCH}	0		ns	
Power Down Time	t_{EHICCL}		12	ns	

1. $\overline{WE(0:7)}$ is high for read cycle.
2. All timings are referenced from the last valid address to the first transitioning address.
3. Addresses valid prior to or coincident with $\overline{CE}$ going low
4. At any given voltage and temperature, t_{EHQZ} (max) < t_{ELQX} (min), and t_{GHQZ} (max) < t_{GLQX} (min), both for a given device and from device to device.
5. Transition is measured ±500 mv from steady-state voltage.
6. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 1)



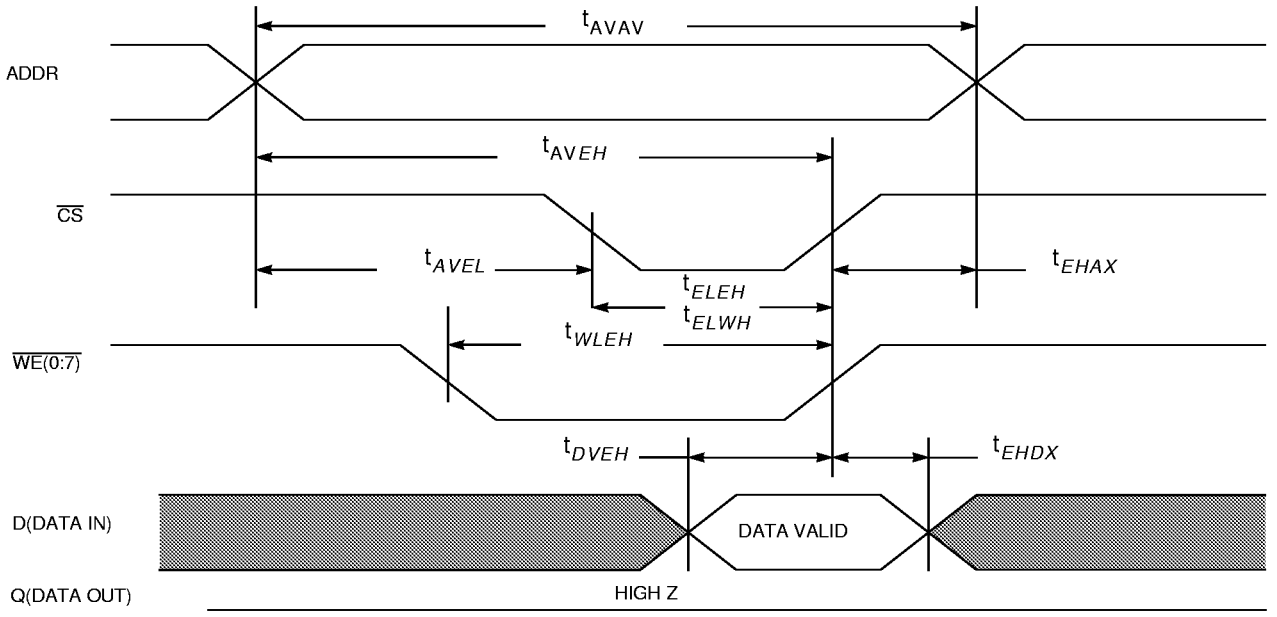
Notes:
1. A write occurs during the overlap of $\overline{OE}$ low and $\overline{WE}$ low..
2. If $\overline{OE}$ goes low coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.

Write Cycle 1 ($\overline{WE}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	1
Address Setup Time	t_{AVWL}	0		ns	
Address Valid to End of Write	t_{AVWH}	10		ns	
Write Pulse Width	t_{WLWH} t_{WLEH}	10		ns	
Write Pulse Width $\overline{G}$ High	t_{WLWH} t_{WLEH}	9		ns	2
Data Valid to End of Write	t_{DVWH}	6		ns	
Data Hold Time	t_{WHDX}	0		ns	
Write Low to Output High-Z	t_{WLQZ}	0	6	ns	3, 4, 5
Write High to Output Active	t_{WHQX}	2		ns	3, 4, 5
Write Recovery Time	t_{WHAX}	0		ns	

1. All timings are referenced from the last valid address to the first transitioning address.
2. If $V_{IH} \leq \overline{OE}$, the output will remain in a high impedance state
3. At any given voltage and temperature , t_{WLQZ} (max) < t_{WHQX} (min), both for a given device and from device to device.
4. Transition is measured ±500 mv from steady state voltage.
5. This parameter is sampled and not 100% tested.

Asynchronous SRAM Timing Diagram (Write Cycle 2)



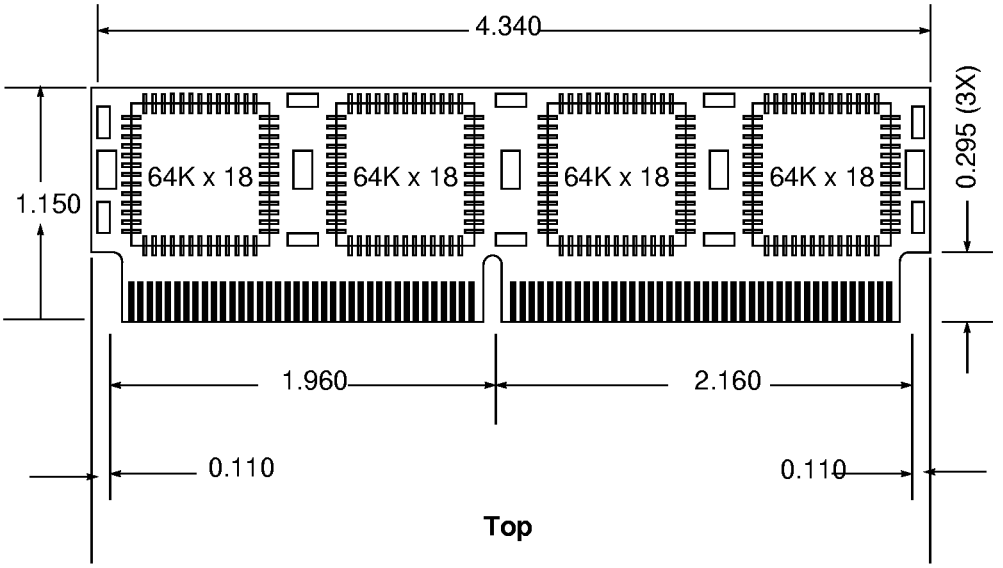
Notes:
1. A write occurs during the overlap of $\overline{OE}$ low and $\overline{WE}$ low.

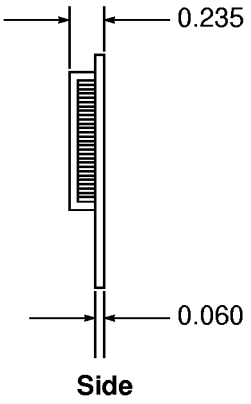
Write Cycle 2 ($\overline{OE}$ Controlled)

Parameter	Symbol	DATA		Unit	Notes
		Min.	Max.		
Write Cycle Time	t_{AVAV}	12		ns	
Address Setup Time	t_{AVEL}	0		ns	
Address Valid to End of Write	t_{AVEH}	10		ns	
Enable to End of Write	t_{ELEH} t_{ELWH}	9		ns	3, 4
Data Valid to End of Write	t_{DVEH}	6		ns	
Data Hold Time	t_{EHDX}	0		ns	
Write Recovery Time	t_{EHAX}	0		ns	

1. A write occurs during the overlap of $\overline{OE}$ low and $\overline{WE}$ low
2. All timings are referenced from the last valid address to the first transitioning address.
3. If $\overline{OE}$ goes low coincident with or after $\overline{WE}$ goes low, the output will remain in a high impedance state.
4. If $\overline{OE}$ goes high coincident with or before $\overline{WE}$ goes high, the output will remain in a high impedance state.

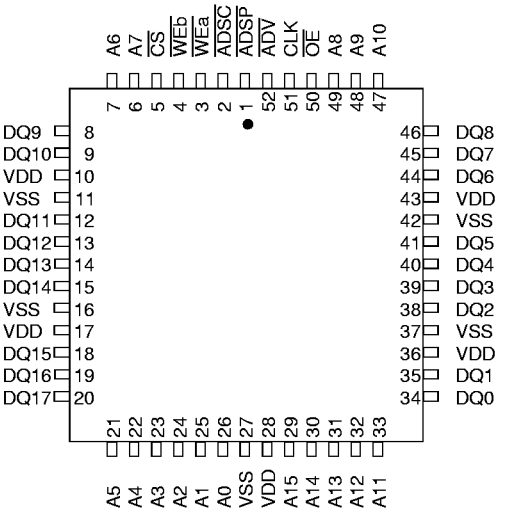
Layout Drawing: 512KB (64K x 72), 160-pin, Synchronous module



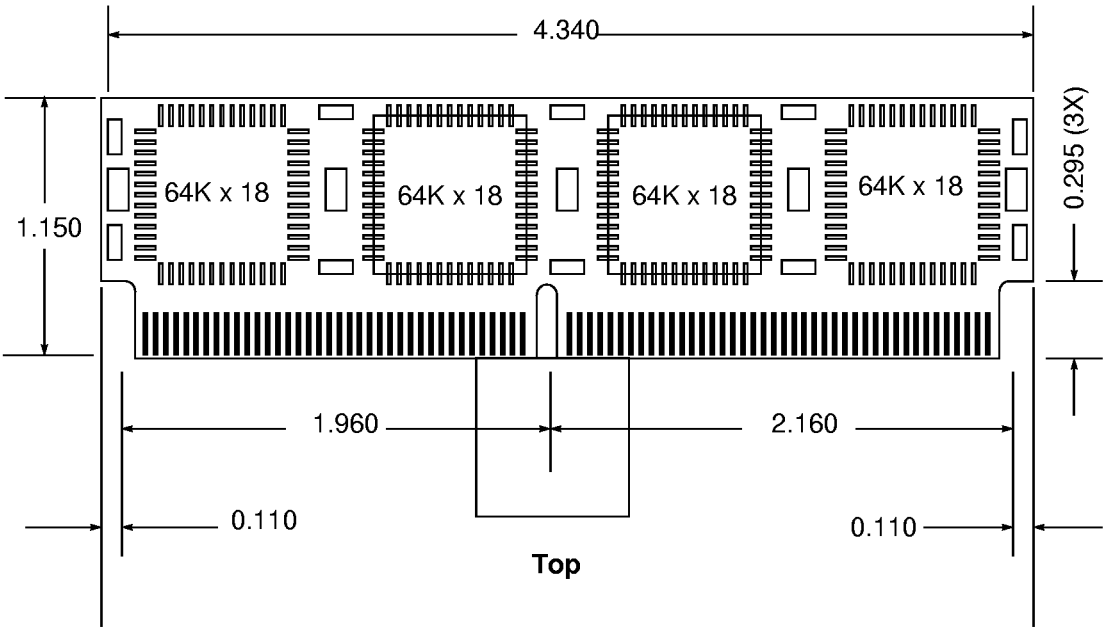


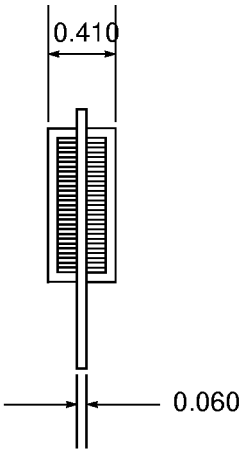
Pinout

64K x 18 PLCC Burst SRAM
(IBM041812PPL)



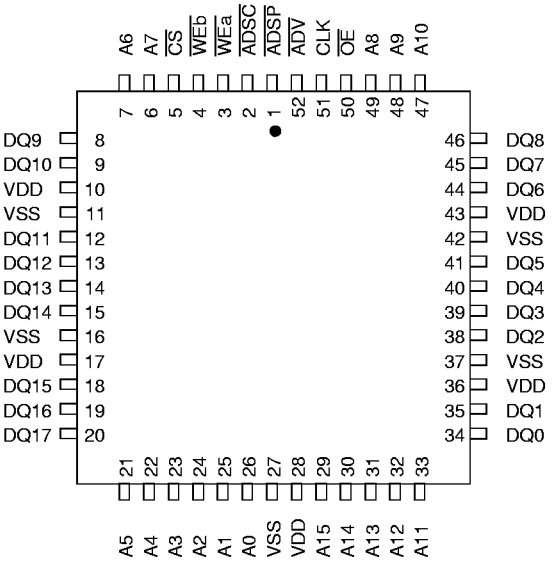
Layout Drawing: 1MB (128K x 72), 160-pin, Synchronous module



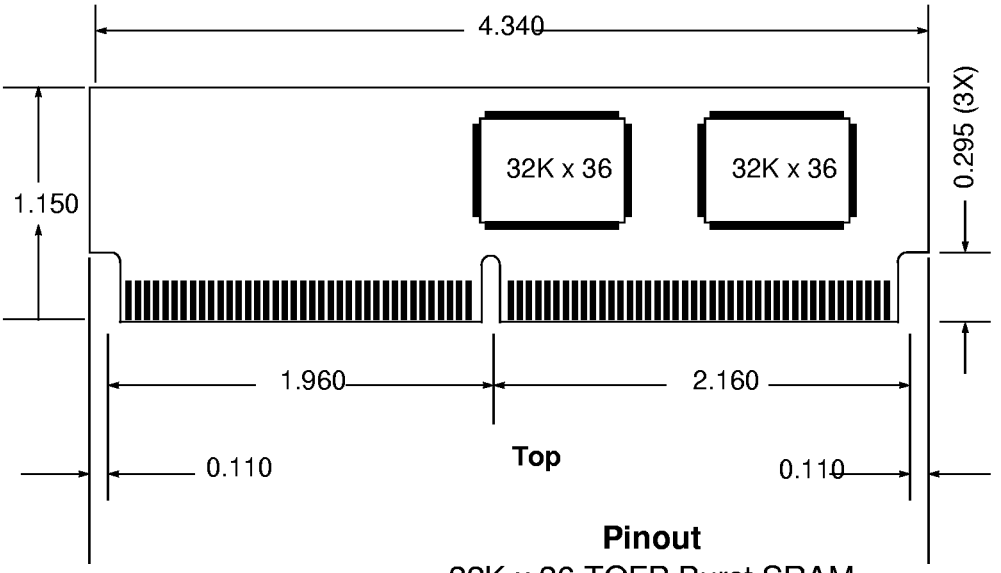


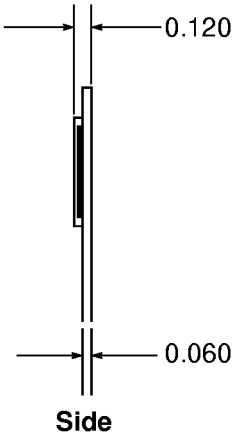
Pinout

64K x 18 PLCC Burst SRAM
(IBM041812PPL)



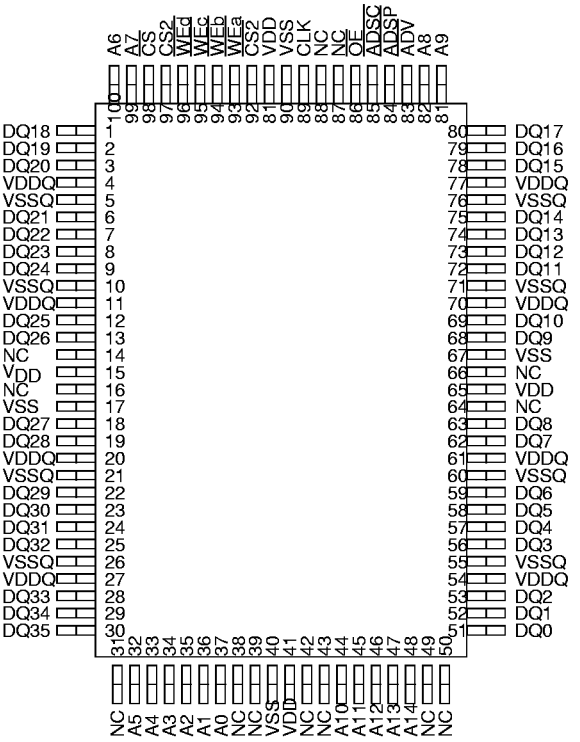
Layout Drawing: 256KB (32K x 72), 160-pin, Synchronous module





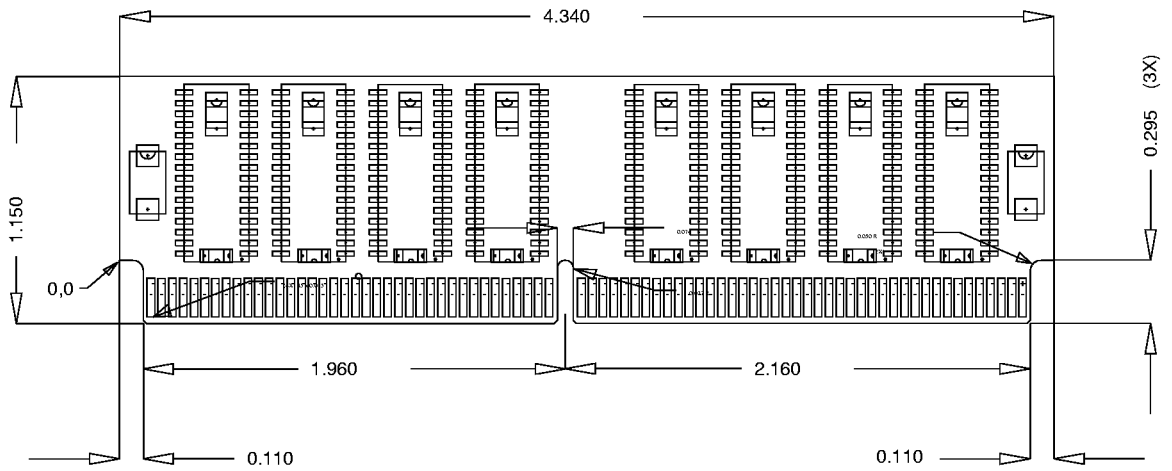
Pinout

32K x 36 TQFP Burst SRAM
(IBM043612PQK)

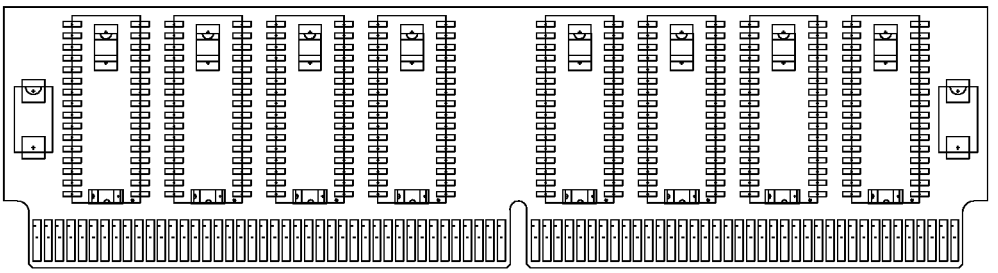


Layout Drawing 512KB (64K x 72), 160-pin, Asynchronous module

Front View:



Back View:



Revision Log

Rev	Contents of Modification
10/94	Initial Release
2/95	Added x36 module info., updated text and added part numbers..
5/95	Added pin capacitance values and defined PD bits.
11/95	Updated DIMM speed offerings and other pertinent information.
12/95	Official release.
2/96	Update part numbers (added 1MB SE design).
4/98	re-release of document.