PowerPC™

Preliminary Data

PowerPC 620 RISC Microprocessor

Highlights

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64-bit Advanced Superscaler Processor:
- Fetch and dispatch up to 4 instructions per cycle
- Speculative execution past 4 unresolved branches
- Register renaming for integer, floating-point registers

Six Execution Units:
- Branch unit with 4 reservation stations
- 3 integer units with 2 reservation stations each
- Floating-point unit supporting IEEE-754 single and double precision with 2 reservation stations
- Load/store unit with 3 reservation stations

Static/Dynamic Branch Prediction:
- Branch prediction in fetch and dispatch stages
- 256-entry branch target address cache
- 2048-entry branch history table

Caches:
- 32KB, 8-way set associative instruction cache
- 32KB, 8-way set associative non-blocking data cache
- Write-thru or write-back data cache modes
- Parity protection on both caches

Memory Management and MP Support:
- 80-bit virtual, 64-bit effective addressing
- 128-entry, 2-way set associative shared TLB
- 20-entry, fully associative segment lookaside buffer
- 16 segment registers for 32-bit mode support
- Separate 64-entry, fully associative effective to real address translators for instruction and data
- 4 instruction, 4 data block address translation registers
- Coherent data cache (4-state MESI protocol)

L2 Cache Interface:
- 128-bit CMOS/GTL data interface
- Unified instruction and data secondary cache
- Direct mapped, physically indexed, physically tagged
- Cache capacity configurable from 1MB to 128MB
- Interface clocked at 1, 1/2 or 1/3 the processor clock
- ECC protected

Bus Interface:
- 40-bit address bus, 128-bit data bus with byte parity
- Supports 64-bit data bus mode
- Split transaction, pipelined snoop bus protocol
- Interface clocked at 1/2, 1/3 or 1/4 the processor clock
- On-chip phase-lock-loop

Software/System Support:
- Performance monitor functions
- Power management
- IEEE 1149.1 (JTAG) interface and on-chip LSSD
- Array built-in self test and on-chip debug support

Product Description

The PowerPC 620* RISC microprocessor is the first chip in a new product line of servers and high-end workstations within the PowerPC microprocessor family. It features high bandwidth memory subsystem ideal for symmetric multiprocessing, transaction processing and numerically intensive computing. It's the first 64-bit implementation of the PowerPC Architecture* supporting both 32/64-bit applications.

The PowerPC 620 microprocessor has a center frequency of 133 MHz and uses a 5-stage pipeline: fetch, dispatch, execute, complete and writeback. It uses a superscaler design to control six independent execution units: branch, three integer, floating-point and load/store. Branch prediction, instruction prefetching and speculative execution are used to take advantage of multiple execution units. Instructions are dispatched to the execution units in program order, executed out-of-order, and completed in-order to support precise exceptions.

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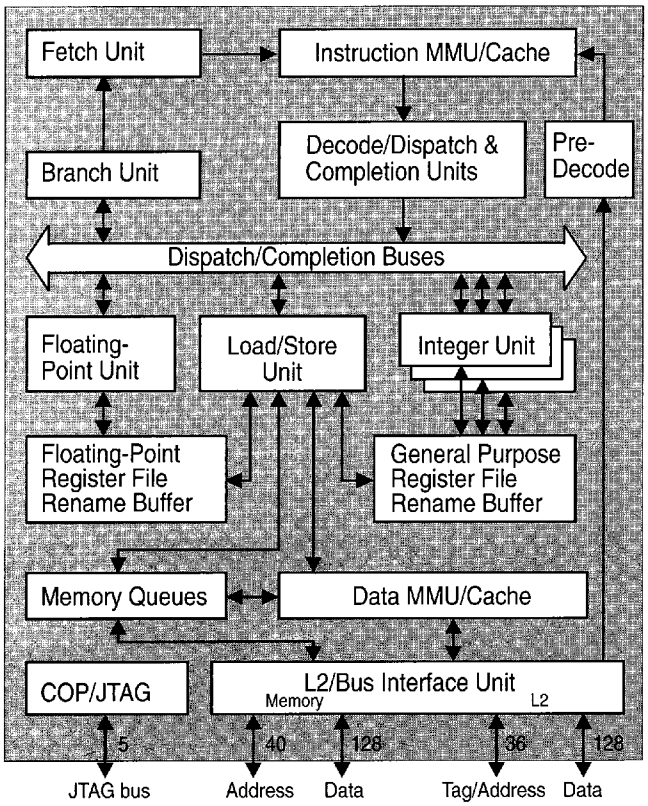
Specifications

Technology	0.5 µm CMOS, four levels of metal
Die Size	311mm², 17.1 mm x 18.2 mm
Number of Transistors	~7 million
Performance	225 SPECint92**, 300 SPECfp92** @ 133MHz (estimated)
Supply Voltage	3.3V ± 0.3V
Power Dissipation	30W @ 133MHz
Signal I/O	482
Packaging	25 x 25 Ball Grid Array (BGA)



[1] In this document, the terms "PowerPC 620 microprocessor" and "620" are used to denote the fourth microprocessor of the PowerPC Architecture family.

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