Introduction

General Description

This PMD Module is designed to be a direct replacement for the previous IBM Token Ring PMD module, as well as to provide further board component cost reduction when used in new applications.

The PMD Module provides the network interface required for the IEEE 802.5 Token-Ring protocol. It is designed to be used with an IBM internally designed protocol MAC (Media Access Control) chip, such as the Token Ring MAC for ISA/PCMCIA or Token Ring MAC for PCI.

The token-ring serial data are received, equalized, and phase-aligned by the PMD Module. Recovered clock and data are brought to chip I/O. This module also has a dual Phase Lock Loop (PLL) design, which enables both 4-Mbps and 16-Mbps data to be received simultaneously, allowing the MAC chip to implement the Ring Speed Detect function.

On the Transmit side, the PMD Module converts the Manchester encoded Transmit data and clock to a differential signal for transmission onto the media (shielded twisted pair [STP] or unshielded twisted pair [UTP]). A phantom drive circuit is provided for inserting a station onto the ring.

The PMD Module is rated for operation between 0°C and 70°C ambient temperature and has a Nominal power dissipation of 480 mW (600 mW maximum), with a stand-by power dissipation of only 103 mW.

Fabricated in the state-of-the-art Bi-CMOS process, the PMD Module is available in two different packaging options: a 44-pin plastic leaded chip carrier (PLCC) direct replacement for the previous IBM Token RIng PMD module and a 64-pin thin quad flat pack (TQFP), which provides the additional function.

Key Features

- Supports 4-Mbps and 16-Mbps token-ring speeds
- Clock recovery with pseudo constant phase detector
- Integrated Receive equalizers (4-Mbps and 16-Mbps are independent)
- Supports simultaneous 4-Mbps and 16-Mbps Receive/Clock recovery (allows for Ring Speed Detect implementation)
- Support for UTP and STP cable media
- Wire fault detection
- Auto-FRAQ function for media repeater applications without a MAC chip
- Reduced Power mode (Standby)
- Wrap mode for self-test
- Single +5-V +/- 10% power supply
- Single STP/UTP Interface Magnetics Module (16-Pin) available
- **Synthesizer and Oscillator circuit provides 32-MHz clock generation from 4-MHz crystal**
- **DC control circuit for 3.3-V power supply conversion**
- **Transmit/Receive Swap function**

Note: Features in **bold** require the 64-pin TQFP Module.

Module Part Numbers

The following are the module P/Ns:

- 44-pin PLCC — P/N IBM30CMTA5P0PLAAAT
- 64-pin TQFP — P/N IBM30CMTA5PRLQAAAT

Additional Functions

These functions require the 64-pin TQFP package.

- DC Control circuit to assist in 5-V to 3.3-V power supply conversion.
- Synthesizer/Oscillator circuit, which allows the PMD Module to use the original 32-MHz oscillator or a 4-MHz crystal.
- Swap circuitry has been added, which allows the Media Transmit and Receive outputs of the PMD Module to be switched.
- A second Wrap feature has been added for hub applications, which performs a media wrap.
- MAC-less media repeater, or *Dumb Repeat mode*, has been enhanced.
  - The second Wrap feature eliminates the external wiring previously required.
  - Start-up Frequency Acquisition (FRAQ) requirement has been eliminated by adding a VCO Missing circuit.
  - Ring Speed Detect circuit has been added to determine if ring speed is 4-Mbps or 16-Mbps.

Minor Changes

The following changes have been made to the PMD Module. These changes, for the most part, do not impact typical adapter applications.

- Threshold detect level has been increased from 10 mV to 75 mV (peak to peak).
- In Dumb Repeat mode, idles are generated on the Receive clock and data outputs during FRAQ condition.
- When in Reset/Standby mode, the 32-MHz oscillator/synthesizer clock circuit, including the buffer output and the regulator circuit, still functions. Formerly, Reset/Standby disabled all circuits and I/Os.
- New layout guidelines are provided for applications which cannot provide an isolated Receive analog section.

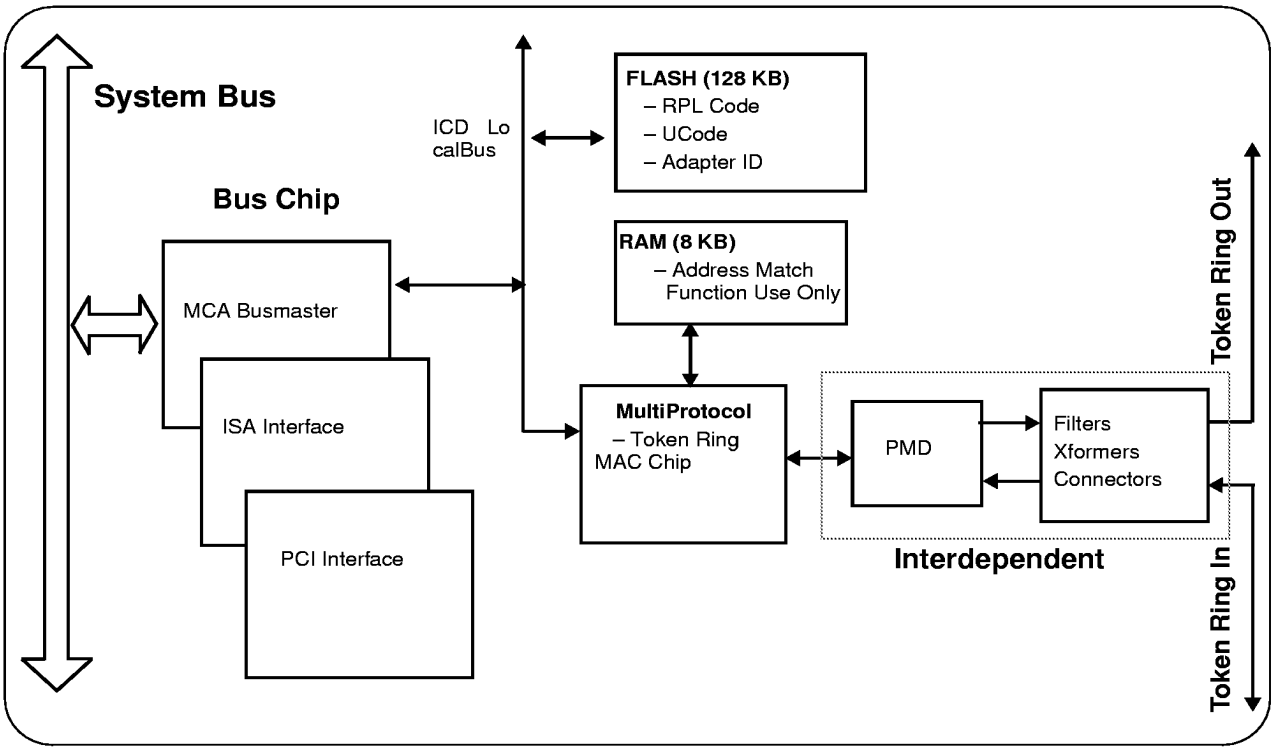
Typical PMD System Application

Figure 2 shows a system application example of the PMD Module in a media-speed token-ring adapter card. The PMD Module is used in combination with the MultiProtocol Controller MAC chip and a bus interface chip (PCI, ISA, Microchannel). In addition to the PMD Module, discrete transformer and filtering components are required to interface to the cable media.

The PMD Module can also be used with the Token Ring MAC for ISA/PCMCIA chip in a classic Store and Forward-type adapter design. This MAC provides both the MAC and the Bus Interface Chip function.

For certain applications, the PMD Module can be used without a MAC chip as a media-level repeater (often called *Dumb Repeat mode*).

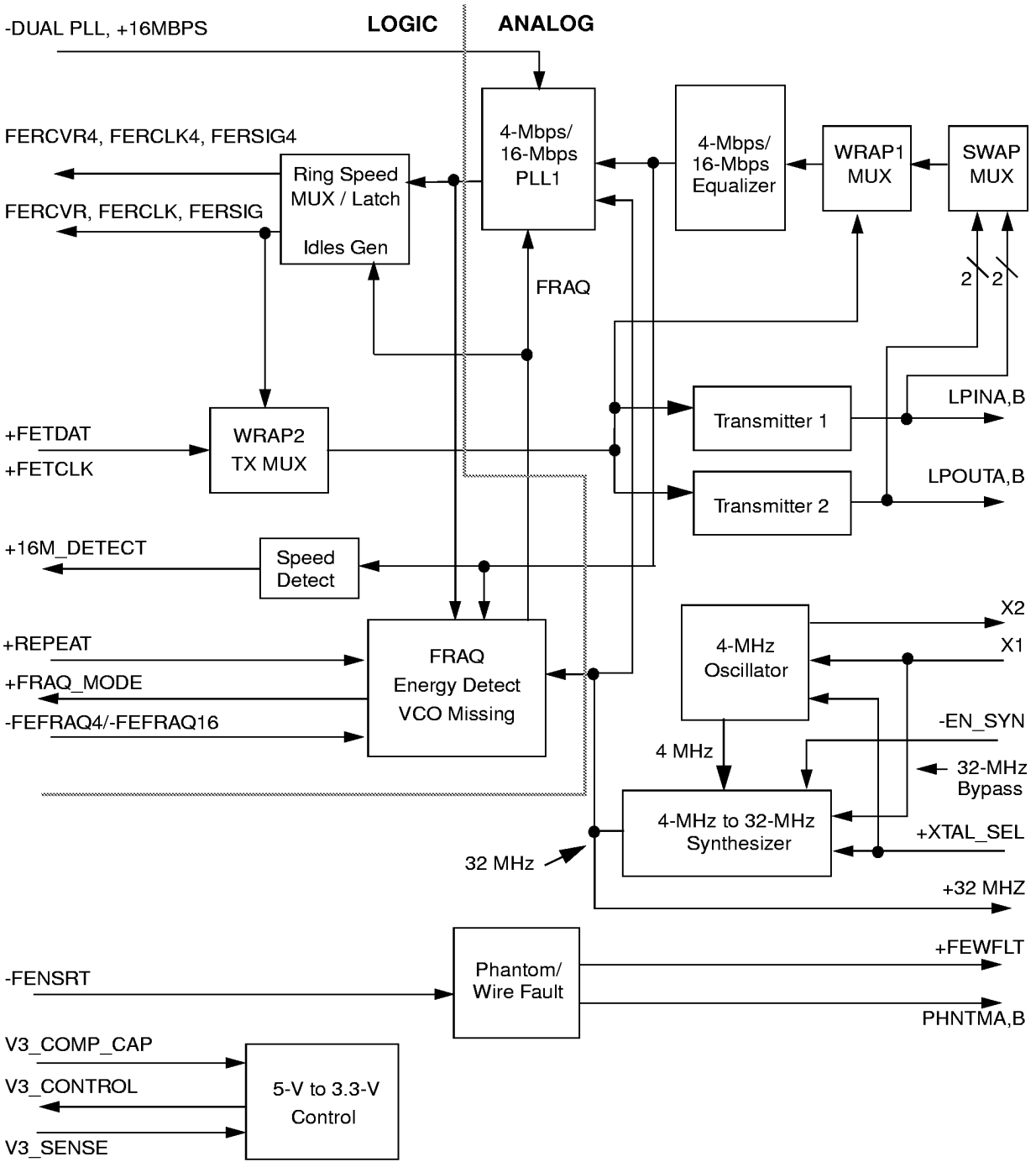
Figure 1. PMD Usage in a Media-Speed Token-Ring Adapter Application



PMD MODULE Functional Block Diagram

Figure 2 illustrates the major functions of PMD. Each of these major functions is subsequently described.

Figure 2. PMD MODULE Functional Block Diagram with Signal Names



Transmitter

The Transmitter section of the chip takes the clock (FETCLK) and data (FEDRVR) signals from the MAC chip, latches the data signal with the rising edge of the clock signal, and transmits the signal from the PMD Module through the isolation transformer and onto the media.

The Transmitter section also includes the Wrap function, which allows the normally transmitted data to be wrapped back to the Receive portion for test purposes.

Receiver and Equalizer (4 Mbps and 16 Mbps)

This section of the PMD chip takes the transformer coupled signal from the media and receives, equalizes, preamplifies, and converts it to digital levels. The receiver also detects the signal amplitude and disables the receiver if the signal amplitude is too small.

The integrated equalizer eliminates the need for external active equalization circuits.

Phase Locked Loop (4 Mbps and 16 Mbps)

This section of the PMD chip derives the data clock from the input data stream. A pseudo Constant Gain PLL is used in the design. The PLL has two modes of operation: Phase Locked mode (normal operation) and Frequency Acquisition (FRAQ) mode.

The FRAQ mode sets the frequency of the Voltage Controlled Oscillator (VCO) by locking the VCO to a 32-MHz signal from the local crystal oscillator. During Phase Locked mode, the PLL is phase locked to the rising edge of the input data and provides a clock aligned to the center of the bit time. The pseudo constant gain circuit ignores every other edge of zeros data in order to provide the same PLL response for both Manchester ones and zeros input.

The PMD Module also supports Dual PLL operation in which both PLLs operate simultaneously. This feature, when combined with functions on the MAC chip and microcode, permits the implementation of Ring Speed Detect, a function which allows an adapter to be plugged into a ring of unknown speed; the adapter itself determines if it is configured to run at the proper speed. Please note that this MAC-level implementation of Ring Speed Detect should not be confused with Speed Detect Circuit internal to the PMD Module. They are two different techniques.

Ring Speed Latch and MUX

The Latch circuit is used to sample the received input data stream with the clock derived from the input data stream. The data signal (FERCVR) is sampled on the falling edge of the clock (FERCLK). The unsampled data (FERSIG) is also provided for test and control purposes.

The MUX circuit is used to multiplex the 4-Mbps Receive data/clock and the 16-Mbps Receive data/clock onto the standard clock and data signals out of the PMD Module.

The Idles Generation circuit is also located in this block. This circuit generates idle data patterns in Dumb Repeat mode when the FRAQ condition occurs.

Phantom Drive and Wire Fault Detect

This section of the PMD chip contains the phantom driver (which provides the current to trip the relay needed to insert a station into the ring), the wire fault detect circuit, and the undervoltage detect circuit. The Wire Fault Detect circuit asserts output +FEWFLT when the resistance on either PHNTMA or PHNTMB is above a high limit or below a low limit. The high limit has a range of 5.5 to 12.0 Kohms and the low limit has a range of 0.05 to 2.4 Kohms. Noise (or unbalanced signal typical of a true broken wire), along with a value near the limit, may cause this circuit to oscillate. Further filtering is done by the MAC chip so that only a solid fault (no glitches) will be reported by the adapter as a fault condition. As a reference, the 802.5 Standard for the adapter fault condition is >50 Kohms or <0.05 Kohms; for a no fault condition, the standard is >2.9 Kohms and <5.4 Kohms.

The +FEWFLT signal will also assert when the undervoltage detect circuit determines that the voltage has dropped 78% to 82% of nominal. This corresponds to a absolute voltage limit of 3.5 V to 4.5 V, assuming a 10% supply.

Speed Detect

The Speed Detect Circuit monitors the incoming data and determines if the frequency is above or below 4.5 MHz (+/- 0.1 MHz). The output, +16M_DETECT, when asserted, indicates that 16-Mbps data is being received.

Wrap1 and Wrap2

The Wrap1 function provides the standard diagnostic Wrapback function implemented. The WRAP2 function provides a Media Wrap function, where data is received from the network, retimed, and then re-transmitted to the network. In Wrap2 mode, the clock and data are also provided on the FERCVR, FERCLK, and FERSIG outputs.

Swap

The Transmitter Swap function allows the PMD Module to transmit or receive on either pair of wires. When Swap mode is disabled, data is transmitted on the LPOUTA/B pins and received on the LPINA/B pins, as is normally done in the PMD Module

. When Swap mode is enabled, data is transmitted on the LPINA/B pins and received on the LPOUTA/B pins.

5-V to 3.3-V Conversion Control Circuit

The 5-V to 3.3-V Control circuit, when combined with external components, provides a regulated 3.3-V (+/-10%) supply voltage from the 5-V (+/- 10%) power supply. The maximum output current which can be supplied with this circuit is 300 mA.

Synthesizer/Oscillator Circuit

The synthesizer/oscillator circuit enables the PMD Module to use a 32-MHz oscillator or a 4-MHz crystal as the clock source.

FRAQ / VCO Missing / Energy Detect

The primary function of this section is to provide energy detection and frequency error detection for the PMD Module when it is used as a MAC-less media repeater, which is often called Dumb Repeat mode. The MAC chip normally provides these functions and puts the PLL circuits in FRAQ mode via the external signals, -FEFRAQ4 and -FEFRAQ16.

The FRAQ logic monitors the Receive clock frequency and puts the PLL circuits in FRAQ mode if the Receive clock frequency deviates from the local crystal frequency. When a Frequency Error is detected, the PLLs are put in FRAQ mode for 128 µs. While in FRAQ mode, the Energy Detect circuit monitors the received data to ensure there are sufficient data transitions to maintain lock. The PLLs will be kept in FRAQ mode until there are enough data transitions to clear the Energy Detect error. The VCO Missing logic monitors the VCO frequency and puts the PLLs in FRAQ mode if the VCO frequency is in error. The limits for each of the three error conditions are shown in Table 1.

Table 1: FRAQ Limits

Sub-Block	4-MB Limits	16-MB Limits
Frequency Error	(0.7–1.2)% of 8 MHz	(3.0–4.0)% of 32 MHz
Energy Detect	<27 +/- 2 rising edges in 16 µs	<27 +/- 2 rising edges in 4 µs
VCO Missing	VCO < 8 MHz	VCO < 8 MHz

Compatibility/Compliance

The PMD Module is designed to be compliant with the IEEE 802.5 Specification; however, full compliance with the IEEE 802.5 Specification also depends on the components used with the PMD Module, the layout of the token-ring front end, and the card manufacturing test.

The Front-End Interface has been tested to be compatible with previous IBM Token-Ring front-end designs on chips such as the original PMD module.

I/O Specifications

PMD Module Pin Descriptions

The following table lists the I/O pins and their definitions grouped by function. The pin number is provided for the 64-pin TQFP package.

Table 2: PMD 64-pin TQFP Module Pin Descriptions

Pin	Pin Name	Type	Description
			CLOCK AND DATA INTERFACE PINS
47	+FERCLK	O, Z	**Received Clock:** This is the clock derived from the Manchester data input. • For 16-Mbps operation, it is 32 MHz • For 4-Mbps operation, it is 8 MHz • In Dual PLL mode operation, it is 32 MHz
51	+FERCLK4	O, Z	**Received Clock:** This is the clock derived from the Manchester data input. • For 16-Mbps operation, it is held at ground • For 4-Mbps operation, it is the same as FERCLK (8 MHz) • In Dual PLL mode operation, it is 8 MHz
53	+FERCVR	O, Z	**Received Data:** This is the retimed Manchester data as it is received from the ring. This signal has been sampled on the falling edge of the FERCLK signal. • For 16-Mbps operation, it is 16-Mbps data • For 4-Mbps operation, it is 4-Mbps data • In Dual PLL mode operation, it is 16-Mbps data
55	+FERCVR4	O, Z	**Received Data:** This is the retimed Manchester data as it is received from the ring. This signal has been sampled on the falling edge of the FERCLK4 signal. • For 16-Mbps operation, it is held at ground • For 4-Mbps operation, it is the same as FERCVR • In Dual PLL mode operation, it is 4-Mbps data
61	+FERSIG	O, Z	**Raw Received Data:** This is the raw, non-retimed Manchester data as it is received from the ring. • For 16-Mbps operation, it is 16-Mbps data • For 4-Mbps operation, it is 4-Mbps data • In Dual PLL mode operation, it is 16-Mbps data
63	+FERSIG4	O, Z	**Raw Received Data:** This is the raw, non-retimed Manchester data as it is received from the ring. • For 16-Mbps operation, it is held at ground • For 4-Mbps operation, it is the same as FERSIG (4-Mbps data) • In Dual PLL mode operation, it is 4-Mbps data
3	+FETCLK	IPU	**Transmit Clock:** This signal is used to sample the FEDRVR signal; it is sensitive to jitter, since any jitter on this signal will be propagated onto the ring.

I/O Type Definitions:

O = TTL output	IPD = TTL Input with 15-KΩ Pull-Down Resistor
Z = Tri-state	IPU = TTL Input with 15-KΩ Pull-Up Resistor
A = Analog	I = TTL Input

Table 2: PMD 64-pin TQFP Module Pin Descriptions

Pin	Pin Name	Type	Description
4	+FEDRVR	IPU	**Transmit Data:** This is the serial Manchester encoded data to be transmitted onto the ring. This signal is latched on the rising edge of FETCLK in order to maintain symmetry.
			CONFIGURATION AND CONTROL PINS
5, 13	-FEFRAQ4, -FEFRAQ16	IPU	**Frequency Acquisition:** Puts the PLL into Frequency Acquisition (FRAQ) mode. This mode sets the center frequency of the VCO by locking the VCO to the local crystal oscillator. • Lo=FRAQ mode • Hi=Normal operation
26	+16MBPS	IPU	**Ring Speed:** Determines which speed (4 or 16 Mbps) is active. • Lo = 4 Mbps • Hi = 16 Mbps
29	-DUALPLL	IPU	**Dual PLL:** Puts the front-end module in dual PLL mode. • Lo = Dual PLL (Both PLLs active) • Hi = Normal operation (PLLs controlled by +16 Mbps)
34	+FENSRT	IPD	**Insert:** Controls the phantom driver (ring insertion). • Lo = Do not insert • Hi = Insert
50	+STANDBY	I	**Standby:** Puts the PMD Module into a Reduced Power Standby mode. • Lo = Normal operation • Hi = Power-Down Standby mode This pin does not perform a POR function; and it does not have an on-chip pull-up or pull-down resistor. It must be externally biased.
23	-FEWRAP	IPU	**Wrap:** Wraps the FEDRVR signal to the receiver inputs. During this mode, the Transmit outputs (LPOUTs) and Receiver inputs (LPINs) are disabled. • Lo = Wrap • Hi = Normal
62	+REPEAT	IPD	**Repeater Select:** Selects mode. • Lo = Operation requires a MAC • Hi = Dumb Repeat mode (MAC-less repeater)
60	-MEDIA_WRAP	IPU	**Media Wrap Mode:** Enables Media Wrap mode.
24	+SWAP	IPD	**Swap Mode:** Enables Swap mode of operation. Transmitter and Receiver pin function are swapped.
			STATUS PINS
1	+16_DETECT	O, Z	**16-Mbps Data Detected:** Output of Ring Speed Detect circuitry indicating that the received data is 16 Mbps as opposed to 4 Mbps.

I/O Type Definitions:

O = TTL output	IPD = TTL Input with 15-KΩ Pull-Down Resistor
Z = Tri-state	IPU = TTL Input with 15-KΩ Pull-Up Resistor
A = Analog	I = TTL Input

Table 2: PMD 64-pin TQFP Module Pin Descriptions

Pin	Pin Name	Type	Description
56	+FRAQ_MODE	O, Z	**FRAQ Mode:** Indicates that the PLL is in FRAQ mode. This signal is valid only when you are in Dumb Repeat mode (+REPEAT asserted).
			OSCILLATOR/CRYSTAL INPUT AND REDRIVE PINS
12	X1	A, I	**Crystal or Oscillator Input:** First input of the 4-MHz crystal circuit analog input or 32-MHz oscillator TTL input.
16	X2	A	**Crystal:** Second input of 4-MHz crystal analog input circuit.
37	SYN_FLT_CAP	A	**Synthesizer Filter Capacitor:** Connection for external capacitor component for synthesizer circuit. Component is only required when synthesizer is used (+EN_SYN asserted).
64	+XTAL_SEL	IPD	**Crystal Select:** Selects 32-MHz Oscillator or 4-MHz Crystal as the clock source. • Lo = Selects 32-MHz Oscillator operation • Hi = Selects 4-MHz Crystal operation
38	+EN_SYN	IPD	**Enable Synthesizer:** Enables Synthesizer operation. Required when 4-MHz Crystal is used. It is optional when the 32-MHz Oscillator is used.
11	32MHZ	O, Z	**32 MHz:** A 32-MHz Clock signal derived from the 4-MHz Crystal or the 32-MHz Oscillator signal.
			PHANTOM DRIVER
14,15	PHNTMA, PHNTMB	O	**Phantom Driver:** Provides the Phantom Drive current necessary to insert a station on the ring.
46	+FEWFLT	O, Z	**Wire Fault:** Indicates the condition of the Phantom Drive lines. • Lo = No Wire Fault • Hi = Wire Fault
			FRONT END TRANSMITTER AND RECEIVER
18, 19	LPOUTA, LPOUTB	A	**Transmit Outputs:** These differential, high-current drive outputs drive the isolation transformer.
30, 31	LPINA, LPINB	A	**Receiver Inputs:** These are differential inputs from the isolation transformer. They feed a differential equalizer/amplifier to provide valid data to the PLL.
			TOKEN-RING FRONT-END DISCRETE COMPONENT CONNECTION PINS
25	RBIAS	A	**Current Bias Resistor:** Used in conjunction with internal bandgap reference voltage to generate an accurate current reference.
27, 28	EQ4A, EQ4B	A	**4-Mbps Equalizer:** Components for the 4-Mbps equalizer.
35, 36	EQ16A, EQ16B	A	**16-Mbps Equalizer:** Components for the 16-Mbps equalizer.
42	FLT16	A	**16-Mbps PLL Filter:** This is where the components for the 16-Mbps PLL filter are connected. *THIS PIN IS EXTREMELY SENSITIVE TO NOISE.*
43	FLTG	A	**PLL Filter Current Return:** This is dedicated current return for the PLL. *THIS PIN IS EXTREMELY SENSITIVE TO NOISE AND SHOULD NOT BE CONNECTED TO GROUND.*
I/O Type Definitions: O = TTL output Z = Tri-state A = Analog			IPD = TTL Input with 15-KΩ Pull-Down Resistor IPU = TTL Input with 15-KΩ Pull-Up Resistor I = TTL Input

Table 2: PMD 64-pin TQFP Module Pin Descriptions

Pin	Pin Name	Type	Description
44	FLT4	A	**4-Mbps PLL Filter:** This is where the components for the 4-Mbps PLL filter are connected. *THIS PIN IS EXTREMELY SENSITIVE TO NOISE.*
			5-V TO 3.3-V CONVERSION PINS
49	V3_SENSE	A	**3.3-V Sense Signal:** Sense input from 3.3-V supply to PMD regulator circuit.
48	V3_CONTROL	A	3.3-V Control Signal: Output from PMD regulator circuit to external PNP transistor circuit.
45	V3_COMP_CAP	A	**Compensation Capacitor:** Connects to off-chip compensation capacitor.
			POWER AND GROUND
–	VDD		**Positive (+5 V) Supply Pins:** Digital • .Pins 2, 9, 21, 58
–	GND		**Negative (Ground) Supply Pins:** Digital. • Pins 7, 10, 17, 20, 22, 54, 57, 59
39	AVDD		**Positive (+5 V) Supply Pins:** Analog
32, 40	AGND		**Negative (Ground) Supply Pins:** Analog
			NO CONNECTS
–	NC		Signal is not connected. • 6, 8, 33, 41, 52

I/O Type Definitions:

O = TTL output	IPD = TTL Input with 15-KΩ Pull-Down Resistor
Z = Tri-state	IPU = TTL Input with 15-KΩ Pull-Up Resistor
A = Analog	I = TTL Input

DC Specifications

Table 3 gives the electrical specifications for the PMD Digital I/O.

Table 3: DC Specifications for PMD I/O

Symbol	Parameter	Conditions	Min	Max	Units
VOH	Minimum High-Level Output Voltage	IOH = - 1 mA	3.0		V
VOL	Minimum Low-Level Output Voltage	IOL = 1 mA		0.4	V
VIH	Minimum High-Level Input Voltage		2.0		V
VIL	Maximum Low-Level Input Voltage			0.8	V
IOZ	Maximum Output Leakage Current in TRI_STATE	VOUT = Vdd or GND	-10	+10	uA
IN1	Input Current w/o Integrated Resistor	VI = Vdd or GND	-1	+1	uA
IN1	Input Current w/ Integrated Resistor	VI = Vdd or GND	-500	+500	uA

The analog I/Os have unique properties and characteristics, and must be wired with the components exactly as shown in the “PMD 64-Pin TQFP Token-Ring Connection Diagram” on page 17.

The Transmitter (LPOUTA, LPOUTB) output signal levels are not standard logic levels. The levels are designed to meet the IEEE 802.5 specification. The typical values are 3.7 volts peak to peak for STP cable and 3 volts peak to peak for UTP cables.

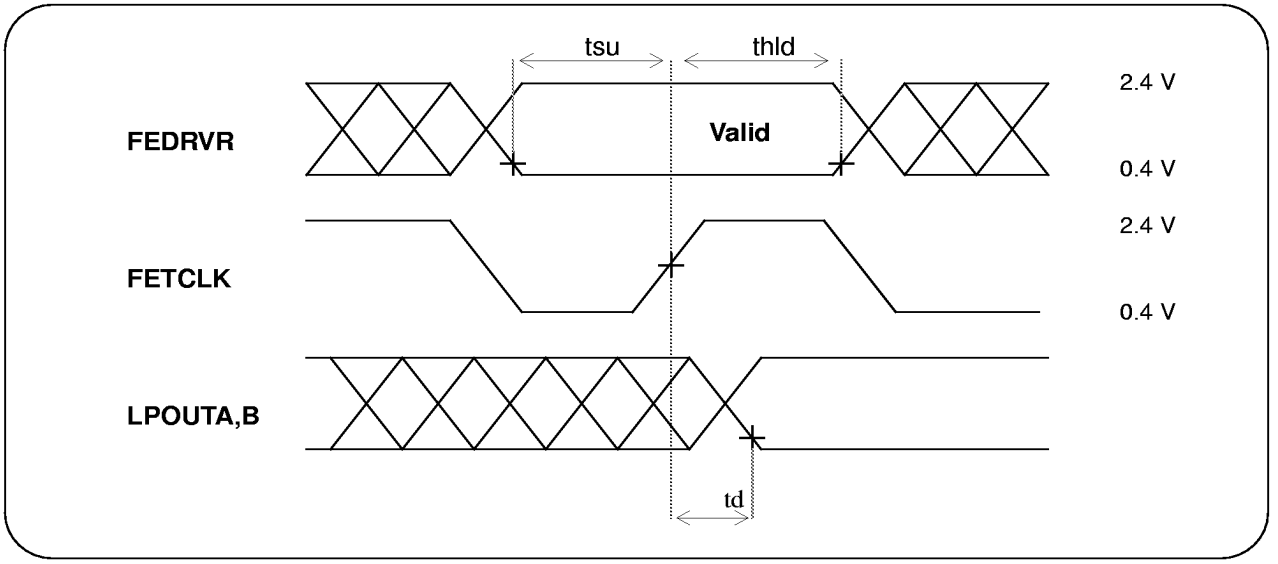
AC Specifications

Transmit Timing Information

Table 4: Transmit Timings—AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tsu	Set-up time	16 Mbps	4			ns
tsu	Set-up time	4 Mbps	4			ns
thld	Hold time	16 Mbps	4			ns
thld	Hold Time	4 Mbps	4			ns
td	Delay from FETCLK transition to LPOUTx transition	16 Mbps		10		ns
td	Delay from FETCLK transition to LPOUTx transition	4 Mbps		10		ns

Figure 3. Transmit Timing Diagrams

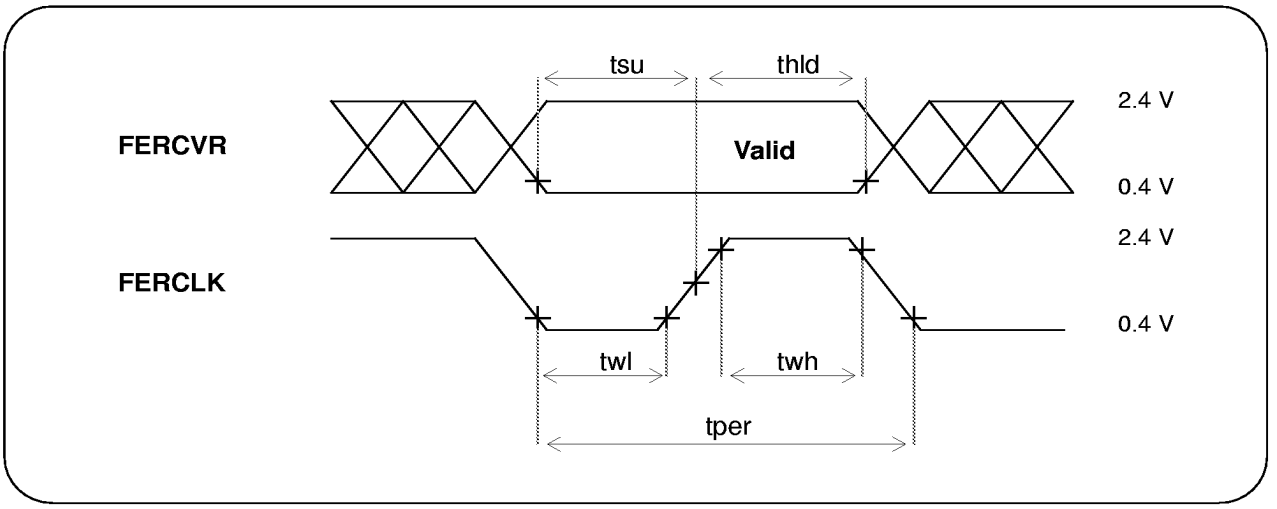


Receive Timing Information

Table 5: Receive Timings—AC Specifications

Symbol	Parameter	Conditions	Min	Typ	Max	Units
tsu	Set-up time	16 Mbps	8			ns
tsu	Set-up time	4 Mbps	50			ns
thld	Hold time	16 Mbps	8			ns
thld	Hold time	4 Mbps	50			ns
twh	Pulse duration, FERCLK high	16 Mbps	12			ns
twh	Pulse duration, FERCLK high	4 Mbps	54			ns
twl	Pulse duration, FERCLK low	16 Mbps	12			ns
twl	Pulse duration, FERCLK low	4 Mbps	54			ns
tper	Period of FERCLK	16 Mbps		31.25		ns
tper	Period of FERCLK	4 Mbps		125		ns

Figure 4. Receive Timing Diagram



Physical Specifications

Power Dissipation

Table 6 provides the power supply dissipation for the PMD Module.

Table 6: PMD Power Dissipation

	IEVdd Nominal	Card Power	Chip Power
Total (nom)	123 mA	625 mW	480 mW
Total (max)	147 mA	750 mW	600 mW
Total (reset)	19 mA	93 mW	103 mW

Power Dissipation Notes:

1. The Power dissipation specifications assume normal PMD operation. Dumb Repeat mode (AutoFRAQ enabled) adds an additional 32 mW nominal (38 mW max) of chip power.
2. The difference between the card power and the chip power is that the card power includes power dissipated by the passive external components connected to the PMD Module (resistors, and so on); however, it does not include the power dissipation of the external transistor circuit for the regulator.
3. The Reset power of 103 mW is nominal.

Electrical Characteristics—Absolute Ratings

Table 7 gives the absolute ratings for various electrical characteristics.

Table 7: Absolute electrical ratings for the PMD Module

Supply Voltage (Vdd)	+4.5 V to +5.5 V
DC Input Voltage (VIN)	-0.5 V to (Vdd + 0.5 V)
DC Output Voltage (VOUT)	-0.5 V to (Vdd + 0.5 V)
Storage Temperature Range (Tstg)	-56°C to +150°C
Operating Temperature Range	TBD
Power Dissipation (PD)	750 mW
ESD Rating	-2000 V to +2000 V

Thermal Characteristics

Table 8: Thermal Characteristics

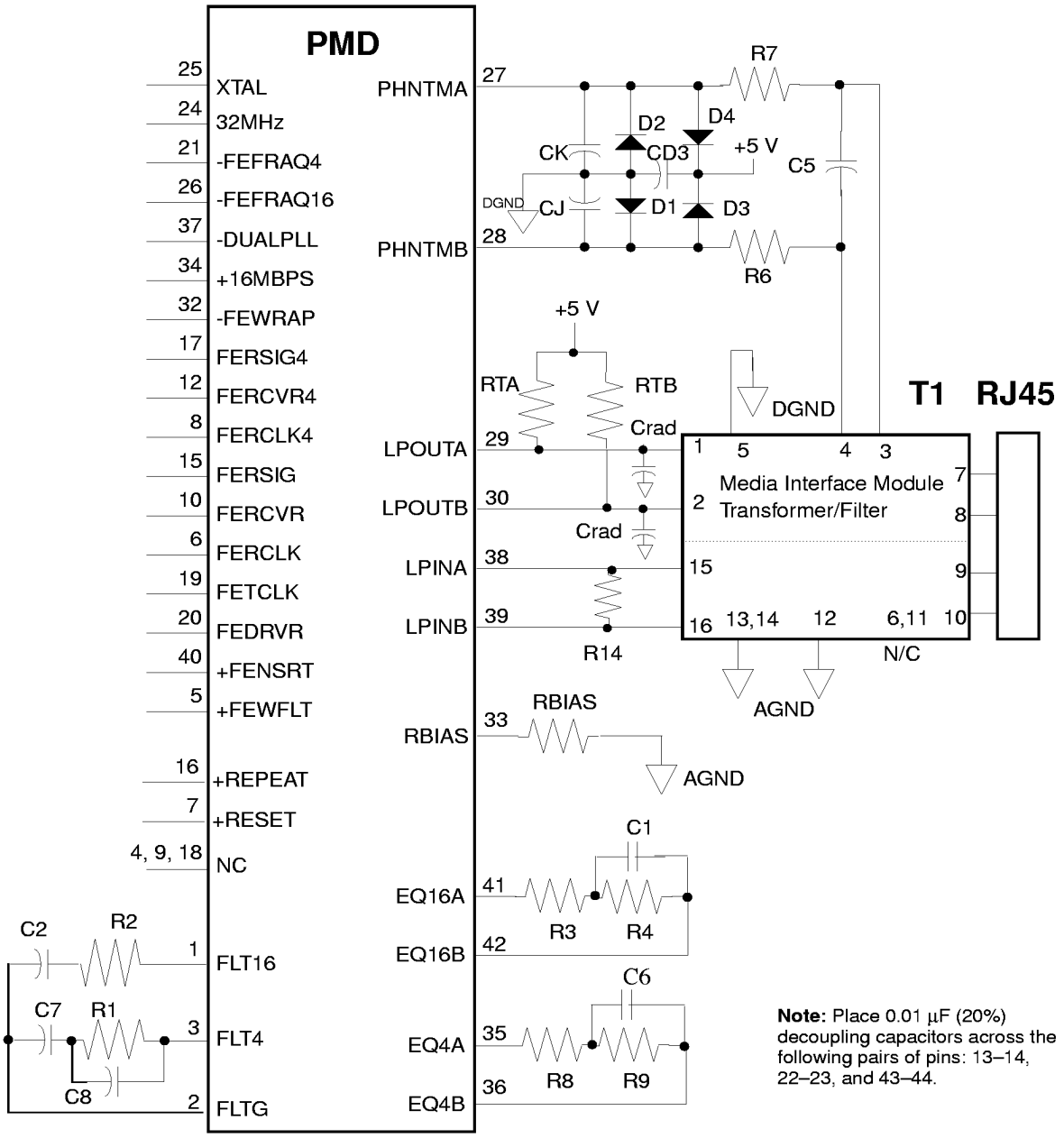
Parameter	Min	Typ	Max	Unit	Test Conditions
Thermal Resistance: Junction to Ambient		45		C/W	0 ft/min airflow

Mechanical Drawing

A complete mechanical drawing of the PMD module is available upon request.

PMD 44-Pin PLCC Token-Ring Connection Diagram

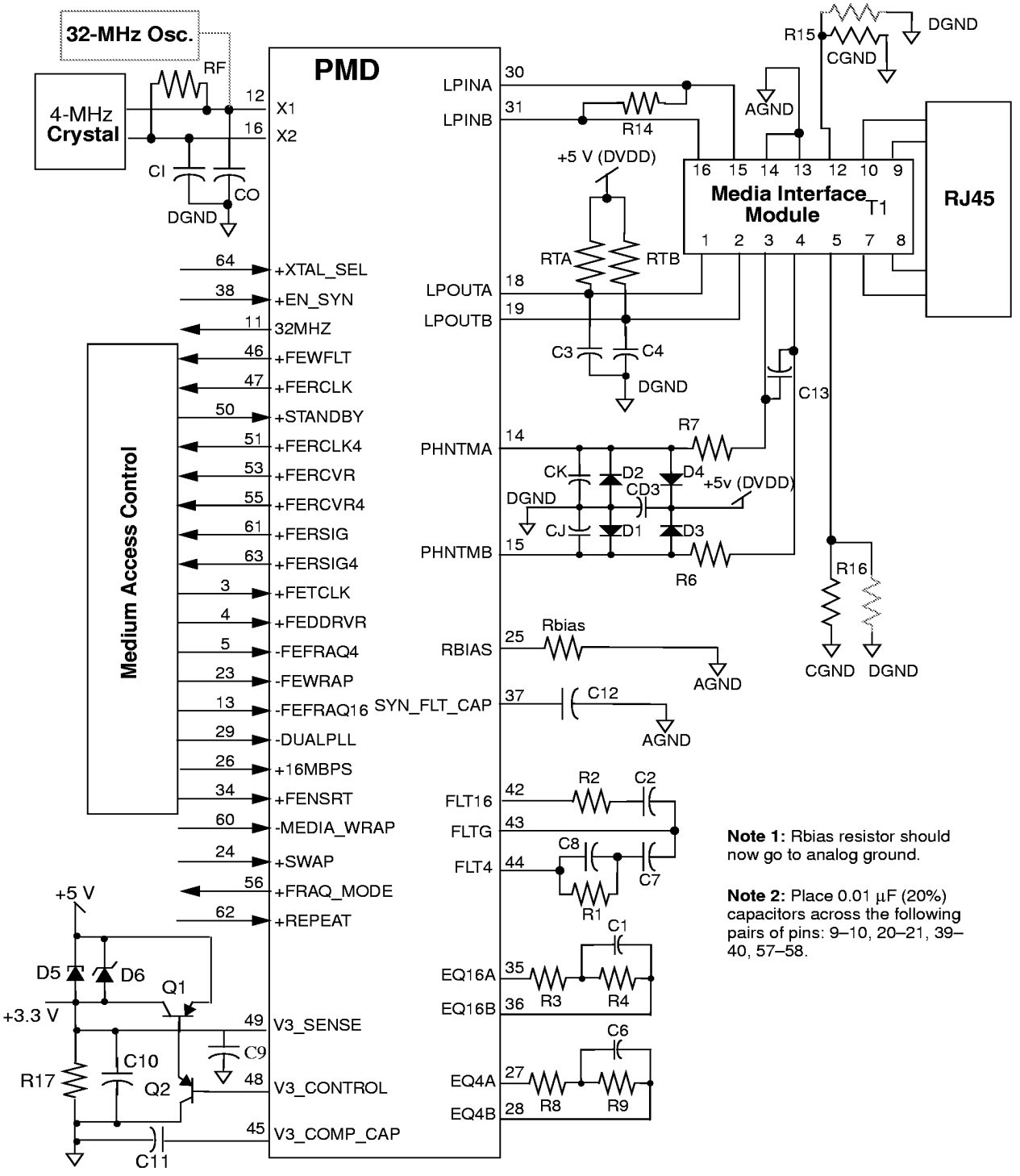
Figure 5. Connection Diagram — 44L PLCC



Note: Place 0.01 µF (20%) decoupling capacitors across the following pairs of pins: 13–14, 22–23, and 43–44.

PMD 64-Pin TQFP Token-Ring Connection Diagram

Figure 6. TQFP Token-Ring Connection Diagram—64 Pin

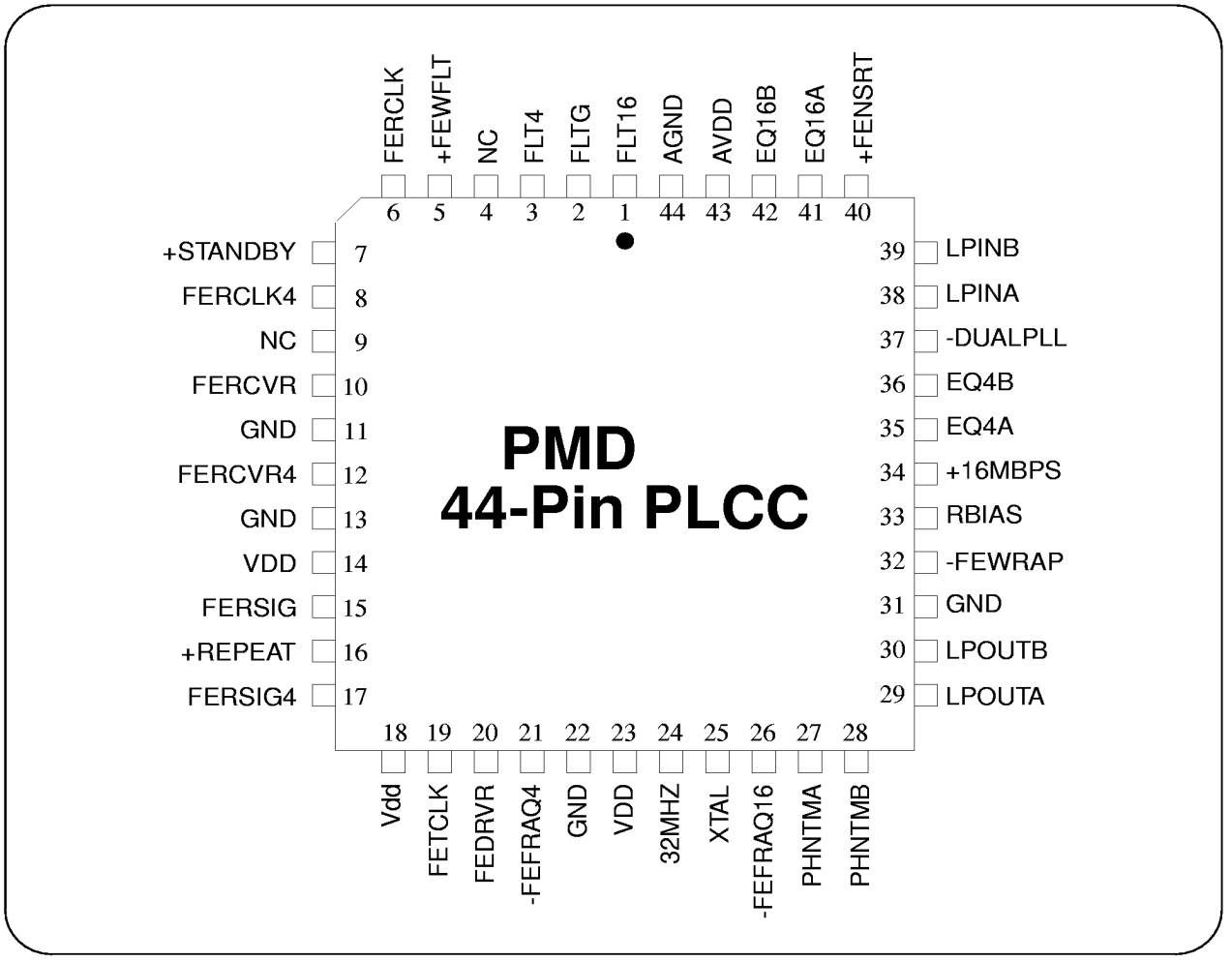


Note 1: Rbias resistor should now go to analog ground.

Note 2: Place 0.01 µF (20%) capacitors across the following pairs of pins: 9–10, 20–21, 39–40, 57–58.

Pin Diagram (44-Pin PLCC Package)

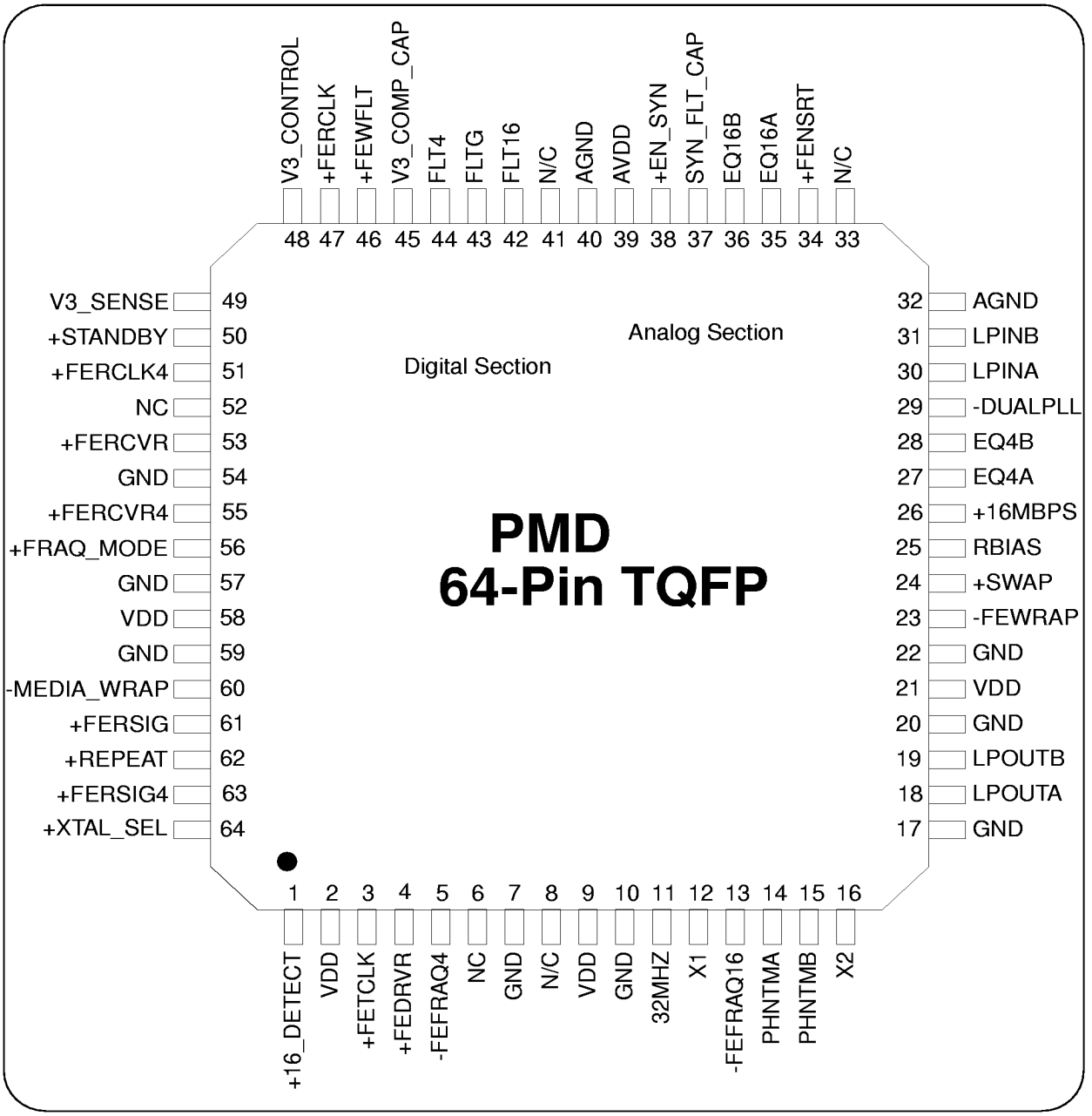
Figure 7. PMD PLCC 44-Pin Connection Diagram As Viewed from the Top of the Module.



Note: In TRAC, Pin 9 was +PLLSEL; Pin 18 was +ALTTX; and Pin 4 was +TEST.

Pin Diagram (64-Pin TQFP Package)

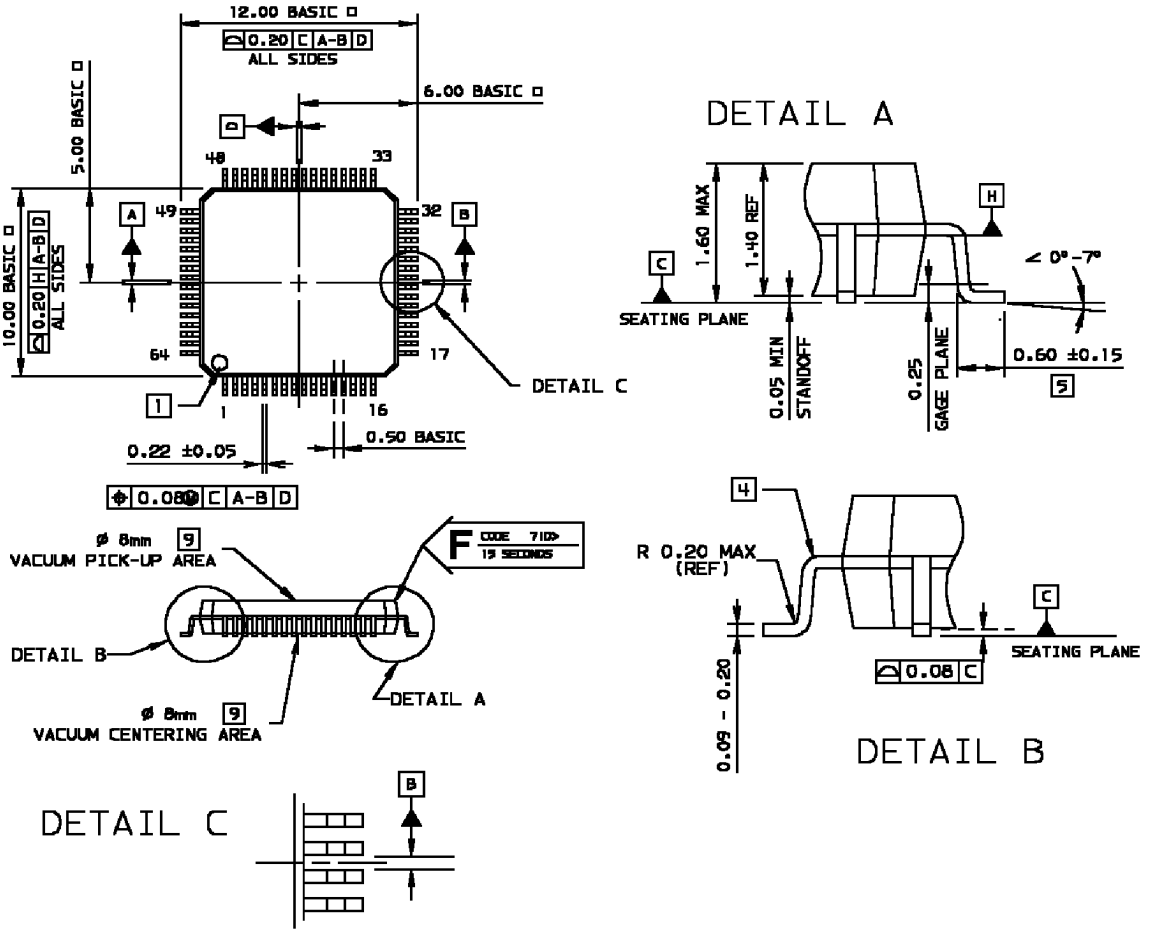
Figure 8. PMD 64-Pin TQFP Connection Diagram As Viewed from the Top of the Module



Note: In the original PMD, Pin 1 was NC; Pin 2 was +ALTTX; Pin 6 was Vdd; Pin 16 was NC; Pin 24 was NC; Pin 37 was EQOA6; Pin 38 was EQOB6; Pin 45 was +TEST; Pin 48 was NC; Pin 49 was Ground; Pin 52 was +PLLSEL; Pin 56 was NC; Pin 60 was Vdd; and Pin 64 was Ground.

Figure 9. Package Diagrams

64 Lead Thin PQFP



1. PIN 1 VISUAL INDICATOR MUST BE EASILY DISTINGUISHABLE FROM ANY MOLD EJECTOR PIN MARKS.
2. LEAD FINISH TO BE Sn/Pb ALLOY. MAXIMUM Sn TO BE 90%. THICKNESS TO BE 5.0 - 20.0 MICROMETERS.
3. MARKING: IBM OR SUPPLIER P/N. DATE CODE, AND MFG'S LOGO.
4. FLASH MAY EXTEND TO INNER VERTICAL SECTION OF LEAD.
5. FOOT LENGTH IS DETERMINED USING GAGE PLANE METHOD PER JEDEC 5PP-008
6. DATUMS A, B, AND D ARE LOCATED AT THE CENTER OF THE SPACE BETWEEN THE CENTER LEADS AND IS MEASURED AT DATUM PLANE H. DATUM D IS ⊥ TO DATUM A-B.
7. APPLICABLE SPECIFICATIONS FOR FINISHED COMPONENTS:
   - A- 68X5655 - MOISTURE SENSITIVE
   - B- 6231587 - GENERAL MECHANICAL
   - C- 23F0325 - PACKAGE FOR SHIPMENT
   - D 2413138 - FLAME APPLICATION PT. FOR FLAMMABILITY SPEC
8. DIMENSIONALLY, THIS PHYSICAL OUTLINE IS EQUIVALENT TO JEDEC REGISTRATION MO-136, VARIATION "BJ".
9. NO MOLD PROTRUSIONS OR INDENTATIONS ALLOWED. LASER MARKING IN THE VACUUM PICK-UP AREA IS ALLOWED

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Glossary

BER. Bit error rate.

CMOS. Complementary metal oxide semiconductor.

CRC. Cyclic redundancy check.

Differential Manchester. A data encoding scheme that is used on a token ring. The bit state is determined from the presence or absence of a transition at the leading bit boundary. A transition is always present at the mid-bit position in a properly encoded bit.

EMC. Electromagnetic compatibility.

EMI. Electromagnetic interference.

FE. Front end.

High-Z (High Impedance). When applied to logic circuitry, this term indicates that the output or input can be in any one of three states. Two of the states are the normal logical 1 and 0 states. The third state is a high impedance state.

IEEE. Institute of Electrical Electronics Engineers.

LAN. Local area network.

LPUL. Least-positive up level.

LPDL Least-positive down level.

LSSD. Level sensitive scan design—a design method which allows IBM to test logic at the chip, module, and/or card levels.

mA. Milliampere.

MAC. Media access control.

Mbps. Megabits per second.

MPUL. Most-positive up level.

MPDL. Most-positive down level.

MPC. Multiprotocol chip. A custom designed VLSI chip which implements the token-ring MAC layer.

PHY. Physical Layer.

PLL. Phase locked loop. A feedback system which synchronizes a received signal stream with a resident oscillator.

PMD. Physical Medium Dependent

POR. Power-on Reset.

ppm. Parts per million.

PWC. Passive wiring concentrator. A ring wiring concentration unit that provides insertion and detachment functions for ring lobes.

RAM. Random access memory.

RAS. Reliability, availability, and serviceability.

R/O. Read only.

ROM. Read only memory.

SPQL. Ship product quality level.

TBD. To be determined.

TEMPL. Twisted-pair Ethernet module for physical layer. National Semiconductor Ethernet Front-End chip.

TRAC. Token-Ring Analog Chip.

TTL. Transistor-transistor logic.

µA. Microampere.

VCO. Voltage Controlled Oscillator. A component of a phase locked loop.

VLSI. Very large scale integration.