IBM Microelectronics
IBM31T1602 Infrared Communications Controller Data Sheet and Application Notes

Note:

Before using this information and the product it supports, be sure to read the general information under "Notices" on page 7

Release 2.0 (February, 1998)

The following paragraph does not apply to the United Kingdom or any country where such provisions are inconsistent with local law:

INTERNATIONAL BUSINESS MACHINES CORPORATION PROVIDES THIS PUBLICATION "AS IS" WITHOUT WARRANTY OF ANY KIND, EITHER EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. Some states do not allow disclaimer of express or implied warranties in certain transactions, therefore, this statement may not apply to you.

Requests for technical information about IBM products should be made to your IBM Authorized Dealer or your IBM Marketing Representative.

TABLE OF CONTENTS

1 IBM31T1602 Infrared Communications Controller 8
1.1. Highlights 8
1.2. General Description 8
1.3. Architecture Description 8
1.4. System Configuration 9
1.4.1. Plug and Play Configuration Register Access 9
1.4.2. Indirect Configuration Register Access 10
1.4.3. Direct Configuration Register Access 10
1.5. UART Subsystem Configuration 10
1.6. FIR Subsystem Configuration 11
1.6.1. FIR Transmit Operation 11
1.6.2. FIR Receive Operation 12
1.7. Interrupt Handling 14
1.8. External Transceiver Interface 14
1.9. Power Management Feature 14
1.10. Pin Descriptions 15
1.10.1. IBM31T1602 Pin Descriptions 16
1.11. Register Summary 20
1.11.1. Plug and Play Register Summary 20
1.11.2. 21
1.11.3. Indirect Configuration Register Summary 21
1.11.4. Direct Configuration Register Summary 21
1.11.5. UART Control Register Summary 21
1.11.6. FIR Control Register Summary 22
2 IBM31T1602 Operational Modes 24
2.1. Overview 24
2.2. Plug and Play Configuration 24
2.3. Indirect Configuration - Host DMA 24
2.3.1. Indirect Configuration Characteristics 26
2.3.2. Configuration Register Power-up Defaults - Indirect Configuration, Host DMA Mode 26
2.4. Indirect Configuration - Shared Memory 28
2.4.1. Configuration Register Power-up Defaults - Indirect Configuration, Shared Memory Mode 29
2.4.1.1 IBM31T1602 Configuration 30
2.4.1.2 IBM31T1602 Configuration 30
2.5. Direct Configuration - Host DMA 30
2.5.1. Direct Configuration Characteristics 31
2.6. Host DMA Approach vs. Shared Memory Approach for Fast IR 32
3 Interfacing Optical Transceivers to the IBM31T1602 33
3.1. Overview 33
3.2. Interfacing to Transceivers from IBM, Temic, Sharp, and Hewlett-Packard 34
3.3. Interface to the IBM31T1101 Transceiver 34
3.4. Interface to the IBM31T1100 and TFDS6000 Transceivers 35
3.4.1. Bandwidth Switching with the IBM31T1101, IBM31T1100 and TFDS6000 Transceivers. 35
3.4.2. Switching from SIR Mode to FIR Mode 36
3.4.3. Switching from FIR Mode to SIR Mode 36
3.5. Interface to the RY5DD01A (Sharp) 37
3.6. Interface to the HSDL-1100 (Hewlett-Packard) 38
3.6.1. Using the IBM31T1602 PDK with an HP Transceiver 38
3.7. Sharp Carrier Detect 39
3.8. RTS Auto Reset Function 39
3.9. Programmed I/O Receive for the FIR Subsystem 39

4 Register Description 40
4.1. Plug and Play Mode 40
4.1.1. Configuration Register Access 40
4.1.2. Plug and Play Configuration 40
4.1.3. Set Read Data Port Address Register (Configuration Location=0x00) 41
4.1.4. Serial Isolation Register (Configuration Location=0x01) 42
4.1.5. Configuration Control Register (Configuration Location=0x02) 42
4.1.6. Wake Command Register (Configuration Location=0x03) 42
4.1.7. Resource Data Register (Configuration Location=0x04) 43
4.1.8. Status Register (Configuration Location=0x05) 43
4.1.9. Card Select Number (CSN) Register (Configuration Location=0x06) 43
4.1.10. Logical Device Number (LDN) Register (Configuration Location=0x07) 43
4.1.11. Activate Register (Configuration Location=0x30) 44
4.1.12. I/O Range Check Register (Configuration Location=0x31) 44
4.1.13. Power Management Register (Configuration Location=0x38) 44
4.1.14. Shared Memory Base Address Bits 23:16 Register (Configuration Location=0x40) 45
4.1.15. Shared Memory Base Address Bits 15:8 Register (Configuration Location=0x41) 45
4.1.16. Shared Memory Control Register (Configuration Location=0x42) 45
4.1.17. Shared Memory Range/Limit Bits 23:16 Register (Configuration Location=0x43) 45
4.1.18. Shared Memory Range/Limit Bits 15:8 Register (Configuration Location=0x44) 46
4.1.19. UART Base Address Upper Byte Register (Configuration Location=0x60 46
4.1.20. UART Base Address Lower Byte Register (Configuration Location=0x61) 46
4.1.21. FIR Subsystem Base Address Upper Byte Register (Configuration Location=0x62) 46
4.1.22. FIR Subsystem Base Address Lower Byte Register (Configuration Location=0x63) 47
4.1.23. UART IRQ Select Configuration Register (Configuration Location=0x70) 47
4.1.24. UART IRQ Type Configuration Register (Configuration Location=0x71) 47
4.1.25. FIR Subsystem IRQ Select Configuration Register (Configuration Location=0x72) 48
4.1.26. FIR Subsystem IRQ Type Configuration Register (Configuration Location=0x73) 48
4.1.27. First DMA Channel Configuration Register (Configuration Location=0x74) 48
4.1.28. Second DMA Channel Configuration Register (Configuration Location=0x75) 49
4.2. Indirect Configuration Registers 49
4.2.1. Power Down Register (PDR, Index=0x02) 49
4.2.2. Identification Register (IDR, Index=0x08) 50
4.2.3. DMA Line Select Register (DLS, Index=0xA2) 51
4.2.4. Shared Memory Base Address Register (SMBA, Index=0xA2) 51
4.2.5. Infrared Control Register (IRC, Index=0xA3) 51
4.2.6. UART High Address Register (UARTH, Index=0xA4) 52
4.2.7. UART Low Address Register (UARTL, Index=0xA5) 52
4.2.8. FIR High Address Register (FIRH, Index=0xA6) 53
4.2.9. FIR Low Address Register (FIRL, Index=0xA7) 53
4.3. Direct Configuration Registers 53
4.3.1. Identification 0 Register (ID0, Index=0x0) 53
4.3.2. Identification Register 1 (ID1, Index=0x1) 53
4.3.3. Setup Register (SET, Index=0x2) 54
4.3.4. UART Low Index Register (UARTL, Index=0x3) 55
4.3.5. UART High Address Register (UARTH, Index=0x4) 55
4.3.6. FIR Low Address Register (FIRL, Index=0x5) 55
4.3.7. FIR High Address Register (FIRH, Index=0x6) 55
4.3.8. Local DMA Control Register (LDMAC, Index=0x7) 55
4.3.9. Shared Memory Base Address Register (SMBA, Index=0x7) 56
4.4. UART Control Registers 56
4.4.1. Receive Buffer Register (RBR, Index=0x0, DLAB=0) 56
4.4.2. Transmit Holding Register (THR, Index=0x0, DLAB=0) 56
4.4.3. Interrupt Enable Register (IER, Index=0x1) 56
4.4.4. Interrupt Identification Register (IIR, Index=0x2) 57
4.4.5. FIFO Control Register (FCR, Index=0x2) 57

4.4.6. Line Control Register (LCR, Index=0x3) 58
4.4.7. Modem Control Register (MCR, Index=0x4) 59
4.4.8. Line Status Register (LSR, Index=0x5) 59
4.4.9. Modem Status Register (MSR, Index=0x6) 61
4.4.10. Scratchpad Register (SCR, Index=0x7) 62
4.4.11. Divisor Latch LSB Register (DLL, Index=0x0, DLAB=1) 62
4.4.12. Divisor Latch MSB Register (DLM, Index=0x1, DLAB=1) 62
4.5. FIR Control Registers 63
4.5.1. Master Control Register (All Banks, Index=0x0) 63
4.5.2. Master Status Register (Bank=0, Index=0x1) 63
4.5.3. Miscellaneous Control Register (Bank=0, Index=0x1) 64
4.5.4. RxFIFO Register (Bank=0, Index=0x2) 65
4.5.5. TxFIFO Register (Bank=0, Index=0x2) 65
4.5.6. TxControl 1 Register (Bank=0, Index=0x3) 65
4.5.7. TxControl 2 Register (Bank=0, Index=0x4) 68
4.5.8. TxStatus Register (Bank=0, Index=0x5) 69
4.5.9. RxControl Register (Bank=0, Index=0x6) 70
4.5.10. RxStatus Register (Bank=0, Index=0x7) 70
4.5.11. Reset Command Register (Bank=0, Index=0x7) 72
4.5.12. Frame Address Register (Bank=1, Index=0x1) 72
4.5.13. Rx Byte Count Low Register (Bank=1, Index=0x2) 72
4.5.14. Rx Byte Count High Register (Bank=1, Index=0x3) 73
4.5.15. Rx Ring Frame Pointer Low Register (Bank=1, Index=0x4) 73
4.5.16. Rx Ring Frame Pointer High Register (Bank=1, Index=0x5) 73
4.5.17. Tx Byte Count Low Register (Bank=1, Index=0x6) 73
4.5.18. Tx Byte Count High Register (Bank=1, Index=0x7) 74
4.5.19. Infrared Configuration 1 Register (Bank=2, Index=0x1) 74
4.5.20. Infrared Transceiver Control Register 1 (Bank=2, Index=0x2) 75
4.5.21. Infrared Transceiver Control Register 2 (Bank=2, Index=0x3) 76
4.5.22. General Purpose Timer Register (Bank=2, Index=0x4) 76
4.5.23. Infrared Configuration 3 Register (Bank=2, Index=0x5) 77
4.5.24. Modem Tuning Register (Bank=2, Index=6) 78
4.5.24.1 Pre-demodulation Pulse Shaping 78
4.5.24.2 Basic Pulse Shaping Operation 78
4.5.24.3 Adaptive Operation 79
4.5.24.4 4 Mbits/s Tuning Options 80
4.5.24.5 1.152 Mbits/s and SIR Tuning Options 83
4.5.25. Shared Memory Page Register (Bank=3, Index=0x1) 83
4.5.26. TxDMA Start Address Low Register (Bank=3, Index=0x2) 84
4.5.27. TxDMA Start Address High Register (Bank=3, Index=0x3) 84
4.5.28. Revision ID Register (Bank=3, Index=0x7) 85
5 Electrical Specifications 86
5.1. Recommended Operating Conditions 86
5.2. Power Requirements 86
5.3. DC Specifications 86
5.3.1. Driver DC Voltage Specifications (in Volts) 86
5.3.2. Driver DC Currents at Rated Voltages 86
5.3.3. Receiver DC Voltage Specifications (in Volts) 86
5.3.4. Receiver DC Current Specifications 87
6 Timing Diagrams 88
6.1. IBM31T1602 in Host DMA Mode, ISA I/O Write Cycle 88
6.2. IBM31T1602 in Host DMA Mode, ISA I/O Read Cycle 89
6.3. IBM31T1602 in Host DMA Mode, ISA DMA Read Cycle (I/O Write) 90
6.3.1. ISA DMA Read (I/O Write) Timing Specification 90
6.4. IBM31T1602 in Host DMA Mode, ISA DMA Write Cycle (I/O Read) 91
6.4.1. ISA DMA Write (I/O Read) Timing Specification 91

6.5. IBM31T1602 in Shared Memory Mode, ISA I/O or Memory Write Cycle with Wait State 92
6.6. IBM31T1602 in Shared Memory Mode, ISA I/O or Memory Read Cycle with Wait State 93
6.7. IBM31T1602 in Shared Memory Mode, Local Memory Write Cycle 94
6.8. IBM31T1602 in Shared Memory Mode, Local Memory Read Cycle 95
Appendix A : Application Notes 96
A.1 : Metastability in FIR subsystem 96
A.2 : Premature reset of EOM with Auto Reset RTS on 96
A.3 : Interrupt Status Bits Stability 97
A.4 : Sharp Carrier Detection when in IrDA-FIR mode 97
A.5 : Sharp Carrier Detection when in IrDA-SIR mode 97
A.6 : Hard vs. Soft Powerdown for Plug and Play Shared Memory Mode 97
A.7 : RTS bit is write-only 98
Appendix B : IR Modulation Schemes 99
HP-SIR Modulation 99
B.2 : Sharp Modulation 99
B.3 : 1.152 Mbits/s Modulation 99
B.4 : 4 Mbits/s 4PPM Modulation 100
B.4.1 : 4 Mbits/s 4 PPM Format 100
B.4.2 : 4 PPM Baud Rate 101
Appendix C : Indirect Configuration Register Default Settings 102
Appendix D : UART Information 104
D.1 : UART Reset Control 104
D.2 : UART Interrupt Priority Settings Of the Interrupt Identification Register 104
D.3 : Programmable Baud Rate Generator 105
Appendix E : Bandwidth Switching with the IBM31T1101, IBM31T1100 and TFDS6000 Transceivers 106
E.1 : Switching from SIR Mode to FIR Mode 106
E.2 : Switching from FIR Mode to SIR Mode 107
Appendix F : Internal Resource Data Structure 108
F.1 : Internal Resource Data Structure - Host DMA 108
F.2 : Internal Resource Data Structure - Local DMA 109
7 Appendix G : Pinout Cross Reference 112
Appendix H : Packaging Information 116
H.1 : IBM31T1602 Footprint 116
Appendix I : Ordering Information 117

NOTICES

References in this publication to IBM products, programs or services do not imply that IBM tends to make these available in all countries in which IBM operates. Any reference to an IBM licensed program in this publication is not intended to state or imply that only IBM's licensed program may be used. Any functionally equivalent product, program or service that does not infringe any of IBM's intellectual property rights may be used instead of the IBM product, program or service. Evaluation and verification of operation in conjunction with other products, except those expressly designated by IBM, are the user's responsibility.

IBM may have patents or pending patent applications covering subject matter in this document. The furnishing of this document does not give you any license to these patents. You can send license inquiries in writing, to the IBM Director of Commercial Relations, IBM Corporation, Purchase, NY 10577.

The information provided is believed to be accurate and reliable. IBM reserves the right to make changes to the product described without notice. No liability is assumed as a result of its use nor for any infringement of the rights of others.

This document may contain preliminary information and is subject to change by IBM without notice. IBM assumes no responsibility of liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. Products described in this document are not intended for use in implementation or other direct life support applications where malfunction may result in direct physical harm or injury to persons.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction, NY
12533-6531

Fast Fax Service: 415-855-4121

Trademarks and Service Marks

The following terms, denoted by an asterisk (*), used in this publication, are trademarks or service marks of IBM Corporation in the United States or other countries:

IBM	IBM Microelectronics

The following terms, denoted by an asterisk (*), used in this publication, are trademarks of other companies, as follows:

IrDA	Infrared Data Association
TFDS6000	Temic Semiconductors
RY5DD01A	Sharp Electronics Corporation
HSDL-1100	Hewlett Packard Company

1 IBM31T1602 Infrared Communications Controller

1.1. Highlights

IrDA 1.1**, HP-SIR and Sharp ASK compatible
Supports IrDA data rates up to 4 Mbits/s
16450 and 16550 standard UART compatibility
Interfaces with the IBM31T1100 and IBM31T1101 infrared transceiver modules, and easily connects to other IrDA transceivers
General purpose bidirectional I/O pins for external transceiver control
ISA bus interface
Full ISA Plug and Play support
On-chip or external Plug and Play resource data structure
Plug and Play, Indirect and Direct configuration
Two programmable Rx lines
Host DMA and Shared Memory modes
Supports single or dual DMA channel operation
Back-to-back packet transmission and reception
Advanced interrupt configuration
Low power consumption
Power-down modes
48 MHz external clock input
3.3V supply voltage
Small 100-pin Low Quad Flat Pack (LQFP) package

1.2. General Description

The IBM31T1602 is a low-cost, low-power highly integrated Infrared Communications Controller capable of supporting both low-speed and high-speed infrared modulation schemes. The low-speed communication mode supports data rates up to 115.2 kbits/s. The high-speed mode supports both 1.152 Mbits/s and 4 Mbits/s data rates. Implemented in IBM Microelectronic's 0.8 micron CMOS technology, the IBM31T1602 offers high performance, and many on-chip functions to meet today's and tomorrow's requirements for infrared communications applications.

The IBM31T1602's internal architecture is designed to easily interface to an ISA system, as well as provide multiple configuration modes to satisfy a wide variety of programming needs.

Typical applications for the IBM31T1602 include: data communications, serial data transfer between notebook computers, desktops and printers, and digital camera technology.

1.3. Architecture Description

The IBM31T1602 Infrared Communications Controller consists of an Infrared Core module and a Host Interface module (see Figure 1-1 on page 1-2). The Infrared Core module controls all infrared communications functions and is divided into two subsystems: UART and Fast Infrared (FIR). Each subsystem consists of a controller and a modem.

The UART is fully compatible with the industry standard 16550 UART. The UART subsystem modem is capable of HP-SIR and Sharp ASK modulation. The FIR subsystem consists of a serial-to-parallel, parallel-to-serial converter and supports both 1.152 Mbits/s and 4 Mbits/s IrDA speeds.

The Host Interface module connects to an ISA bus. It contains the bus interface logic, system configuration registers, power management circuitry, and local DMA control functions. The IBM31T1602 supports two modes of block data transfers: Host DMA and Shared Memory Buffer. In Host DMA mode, data is transferred using the host system's DMA controller. In Shared Memory mode, data is first buffered in local RAM, then read by the host for receive or shifted out to the infrared link in transmit.

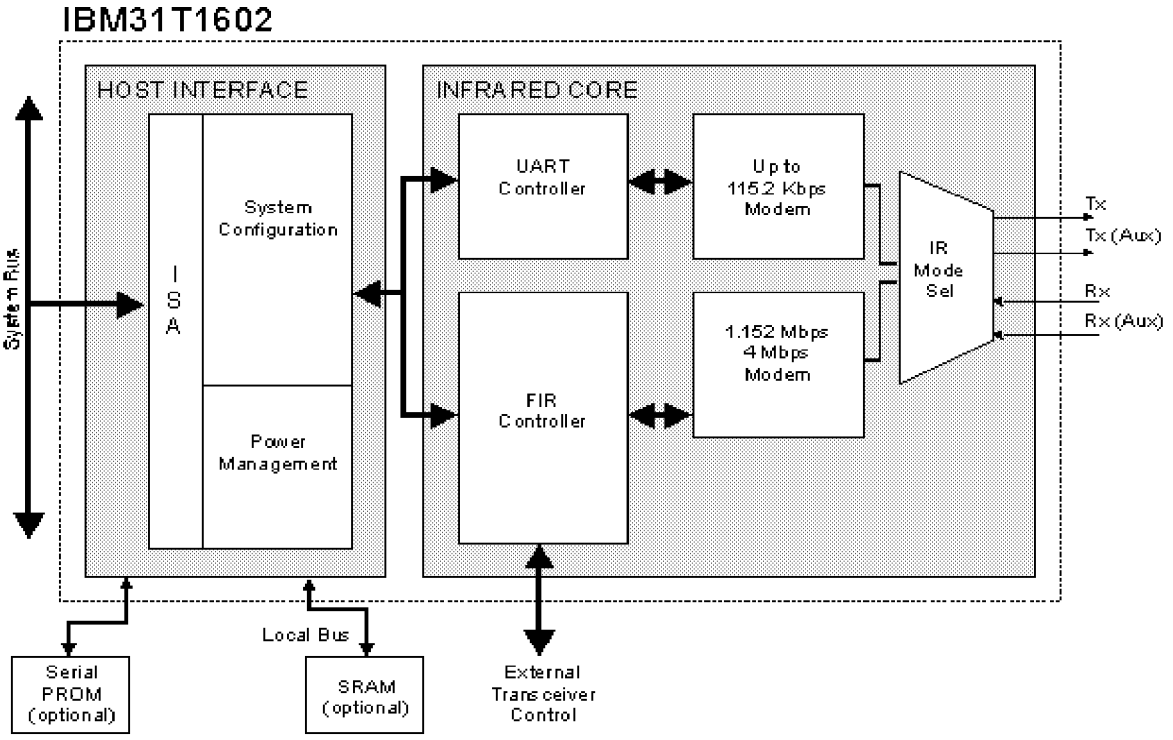


Figure 1-1. IBM31T1602 Functional Block Diagram

1.4. System Configuration

The IBM31T1602 can be configured using one of three methods: plug and play, indirect, or direct configuration. The configuration method is determined by three mode pins: MODE2, MODE1, and MODE0. (See 1.10, "Pin Configuration" on page 1-7)

1.4.1. Plug and Play Configuration Register Access

Plug and Play (PnP) configuration has been implemented in the IBM31T1602 according to the Plug and Play ISA Specification Version 1.0a.

Configuration activity is achieved through three I/O ports:
PnP Configuration Address Port, at I/O address 0279h, write-only
PnP Configuration Write Data Port, at I/O address 0A79h, write-only
PnP Configuration Read Data Port, at a variable address

Note that the Configuration Address Port and Configuration Write Data Port are located at fixed I/O addresses. The Configuration Read Data Port is assigned an address by configuration software, anywhere in the range 0203h to 03FFh as long as the address has 11b (binary) in the bits A1:0. Therefore, valid addresses are 0203h, 0207h, 020Bh, 020F, 0213h, 0217h, 021Bh, 021Fh, etc. The configuration program must ensure that the address does not conflict with a register on a non-PnP ISA device.

To access a PnP configuration register, the address of the target configuration register must first be written to the Configuration Address Port (at location 0279h). Note that a read from location 0279h actually reads the LPT1 printer status port. This is why the PnP Configuration Address Port, also at location 0279h, is a write-only register. To write data into the target configuration register, write the data into the Configuration Write Data Port at location 0A79h. To read data from the target configuration register, read the Configuration Read Data Port.

1.4.2. Indirect Configuration Register Access

Two 8-bit I/O ports are used to access the configuration registers: the index port and data port.

The index port is used to address a specified configuration register. The data port is used to read or write to and from the configuration register that is being pointed to by the index port. The destination and source of the data is determined by the last setting of the index port.

To write to a configuration register, the programmer writes the index value of the configuration register to the index port (see Table 5 for index assignments). Next, the programmer loads the 8-bit data value destined for the configuration register in two consecutive write accesses to the data port. To read from a configuration register, the programmer writes the index value of the configuration register to the index port, then reads from the data port.

Note: Only two consecutive write operations to the data port can modify an indirect configuration register. This protection mechanism prevents accidental erasure of any previously set configuration data. A single read from the index and data port may be done at any time.

The table below shows four possible address locations of the index and data ports. The addresses are set by the BADDR0 and BADDR1 pins.

Index and Data Port Locations

Table 1-1 Index and Data Port Locations

BADDR1	BADDR0	Index	Data
0	0	0x398	0x399
0	1	0x26E	0x26F
1	0	0x15C	0x15D
1	1	0x02E	0x02F

The programmer must determine the index port location after power-on-reset. This is done by reading all four index port addresses twice. After a hardware reset, the correct location is determined by an 0x88 value being returned on the first read, and a 0xDF value being returned on the second read. This signifies that the index port has been located successfully.

The IBM31T1602 can be set to a default configuration on power-up. This is accomplished by setting the CFG2-CFG0 pins. This feature is not available if Plug and Play or Direct Configuration mode is selected. Appendix C, "Indirect Configuration Register Default Settings" on page C-1 describes the different default configurations.

1.4.3. Direct Configuration Register Access

This type of register access is similar to the one used in PS/2 Micro Channel* systems where configuration (POS) registers are accessed by driving the SETUP line low during I/O cycles, and address lines (A2-A0) select one of eight direct configuration registers.

Note: Direct configuration register bits map directly into corresponding indirect configuration register bits.

1.5. UART Subsystem Configuration

The UART subsystem is a fully compatible version of the NS16550 UART. It has full EIA interface capability, however the EIA interface lines do not go out to the module pins, therefore this UART cannot be used as a fully functional COM port. It is mainly used for the low-speed infrared functions. Addressing

to the UART is programmable. The UART address registers must be properly set up during system configuration.

The low-speed infrared modulation in the IBM31T1602 is fully IrDA 1.0 compatible. The UART is used to serialize the packet data to the infrared link one character at a time. Each character has eight data bits, one start bit and one stop bit. Start character, stop character, transparency character insertion or removal and CRC generation or checking as specified in IrDA 1.0 are all done by software.

Two modulation schemes, HP-SIR or Sharp-ASK are supported. In receive, the HP-SIR pulse width can be 1.6 µs or 3/16ths of a single bit time. In transmit, the pulse width is fixed at 1.6 µs regardless of the data rate to conserve power.

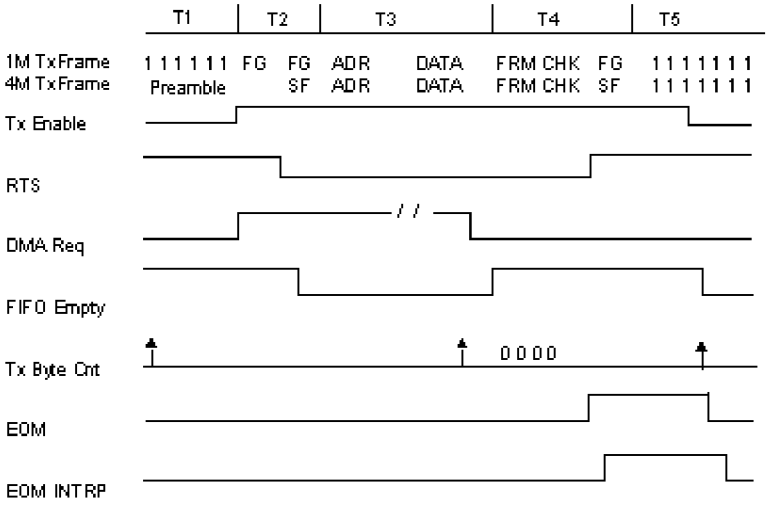
1.6. FIR Subsystem Configuration

The FIR subsystem is fully IrDA 1.1 compatible. It supports the serial infrared link at 576 kbits/s, 1.152 Mbits/s and 4 Mbits/s. The lower speeds are a Synchronous Data Link Control (SDLC) protocol, packet based with start/stop flags delimiting a data packet encoded by 'zero-insertion'. The 4 Mbits/s bit protocol uses an optical preamble and postamble to
delimit the 4 Pulse Position Modulated (4 PPM) packet data.

The FIR High/Low Address Registers must be set up during the system configuration. The Enable Infrared bit must also be set to 1 to grant access to all the FIR internal registers. The FIR Address Registers default to a preset address according to CFG pins settings.

1.6.1. FIR Transmit Operation

The FIR transmit operation is illustrated below:



T1 Set-up phase:

Set up Transmit Control Registers per desired options.
Load the byte count to the Transmit Byte Count Register.
Set up the host DMA controller and the Tx packet.
Set RTS and Transmit Enable bits.

T2 Start-up phase:

RTS is active. If no carrier is detected, the transmitter starts transmitting.
DMA Req is activated if DMA is enabled. The Tx FIFO is filled with transmit data. If DMA is not enabled, the Write Tx FIFO register can be used.
If the Num Start Flag/Preamble bit is 0, the transmitter starts sending flags (1M) or preambles (4M) until the Tx FIFO is half filled (8 bytes). If the Num Start Flag/Preamble bit is 1, the transmitter waits until the Tx FIFO is half filled, then sends two start flags (1M mode) or preambles and one start flag (4M mode).

T3 Send data phase:

The transmitter starts sending data stored in the FIFO.
DMA Req to the host is active when the FIFO is not full.

T4 End of transmission:

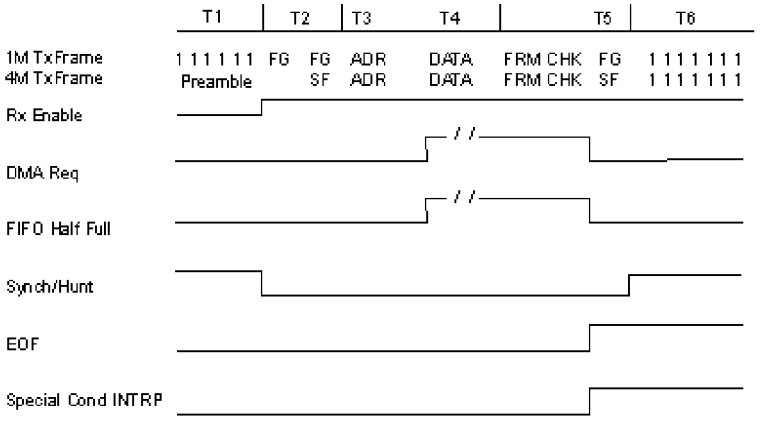
The Byte Counter counts down to 0.
DMA Req stops. The transmitter sends out the remaining data in the FIFO.
CRC generator inverts the CRC and sends it out.
Closing flag is sent. EOM latch is set. Interrupt is activated.

T5 Idle phase:

The transmitter continues sending 1s or flags (1M) or preambles (4M), depending on the Idle line setting option.
The host reads the TxStatus Register to check for transmission completion status.
Reset EOM, Transmit Enable and RTS bits.
End of transmission.

1.6.2. FIR Receive Operation

The FIR receive operation is illustrated below:



Receiving logic facilities:

Receive serialize-deserialize logic and its control circuitry.
Receive Byte Count Register (keeps track of received bytes).
Receive FIFO, 16 x 11 bits: 8-bit data, 3-bit status (Frame Error, Abort and End Of Frame).
Receive Ring Frame Counter (keeps track of the number of receive bytes in the host Rx buffer).
Receive Ring Frame Pointer (points to the last byte of the most recently received packet in the host Rx buffer).

T1 Start-up phase:

Set up Receive Control Registers per the receiving options.
Set Receive Enable bit.
FIR modem logic detects carrier, receive clock starts running. If continuous 1s are received, the receive clock may not be in sync with the incoming data.

T2 Flag(s)/Preambles detection:

When the start flag is detected, all counters in the receiver are initialized. Characters can be recognized from this point on.
0 deletion starts for 1Mbps mode only.

T3 Address matching: the first non-flag byte after the starting flag is the address. Depending on the address mode option, the frame can be rejected or receiving starts. If the frame is rejected, the receiver will look for the next starting flag and another address match.

T4 Receive data:

When a byte of data is received, the data and the three status bits are stored in the Rx FIFO.
If DMA is enabled, DMA Req is activated when the FIFO threshold level is reached. DMA continues until all data stored in the FIFO has been transferred to the host receive buffer. However, the three status bits in the FIFO are not transferred to the host.
If DMA is not used, the Read Rx FIFO I/O command can be used. Read the status bits first, then read the data byte. If EOF or Abort is set to 1, the data byte just read is the last byte of the packet. If the FIFO is still not empty, the next entry is the beginning of another packet. The Receive Byte counter and Receive Ring Frame counter are increased accordingly.

T5 Closing flag:

When the closing flag is detected, the End Of Frame bit will set.
CRC pattern is checked. Frame error is set if CRC is incorrect.

T6 Post-frame phase:

DMA continues until all the received data in the FIFO has been transferred. Two more bytes will be stored in Rx FIFO and transmitted to the host receive buffer. Their format is:

First byte: Bits 7-0 - byte count bits 7 to 0
Second byte: Bit 7 - Abort
Bit 6 - Frame Error
Bit 5 - Overrun
Bits 4 to 0 - Byte Count bits 12 to 8

DMA deactivates.
The Receive Ring Frame pointer is updated pointing to the second byte (see above) which has been stored successfully in the host Rx buffer.
If DMA is not used, the last two bytes will not be stored in the FIFO. Status bit EOF will be set at the last Frame Check byte received.
Steps T2 to T6 are repeated if continuous frame receiving is required.

1.7. Interrupt Handling

Two subsystems in IBM31T1602 can generate host interrupts: the UART (SIR operation) and FIR controller. In direct mode there are four interrupt pins on the module that can be connected to any four host interrupts on the system board. They are: UART Interrupt (UIRQ pin 82), FIR Interrupt (FIRQ pin 83), IRQ3 (pin 49) and IRQ4 (pin 50). In Indirect and Plug and Play modes there are seven interrupt pins on the module that can be connected to any seven host interrupts on the ISA bus. They are: UART Interrupt (UIRQ/IRQ10 pin 82), FIR Interrupt (FIRQ/IRQ15 pin 83), IRQ3 (pin 49), IRQ4 (pin 50), IRQ5 (pin 86), IRQ11 (pin 99) and IRQ13 (pin 85).

The IBM31T1602 provides great flexibility for interrupt merging and routing. Setting the Advanced Interrupt Configuration bit (b3 of the Infrared Control Register) to 1 allows the UART Interrupt and the FIR interrupt to be routed to any of the external interrupt pins (see Interrupt Select bits in the UARTL and FIRL registers). If the Advanced Interrupt Configuration bit is set to 0, both the UART interrupt and the FIR interrupt are merged and can then be routed to IRQ3 or IRQ4. Once the configuration registers have been locked, further interrupts merging can be done by programming the Infrared Configuration 2 Register, which is one of the general control registers.

1.8. External Transceiver Interface

The IBM31T1602 can interface to the IBM31T1100 or IBM31T1101 transceivers with minimal circuitry. Only the following interface lines are used:

TXD	Transmit data.
$\overline{\text{RXD}}$	Receive data.
XCVROFF	Transceiver off; powerdown and bandwidth switching control.

The IBM31T1100 and the IBM31T1101 transceivers require special control information when switching between low speed IrDA and high speed IrDA modes. A serial interface mechanism serves this purpose.

The IBM31T1602 is a 3.3 Volt part, whereas the IBM31T1100 and IBM31T1101 transceivers are 5 Volt parts. While the IBM31T1602 can receive the 5 Volt RXD signal, the TXD and XCVROFF signals to the transceivers must be buffered to 5 Volts.

If other transceivers are used, there are several other transceiver interface lines that can be used:

XCVRDET	Transceiver detect.
GPIO_A - GPIO_D	General Purpose Input/Output pins, controlled by internal registers.

Refer to *IBM31T1602 Infrared Controller Application Note* for information on connecting the IBM31T1602 to various transceivers.

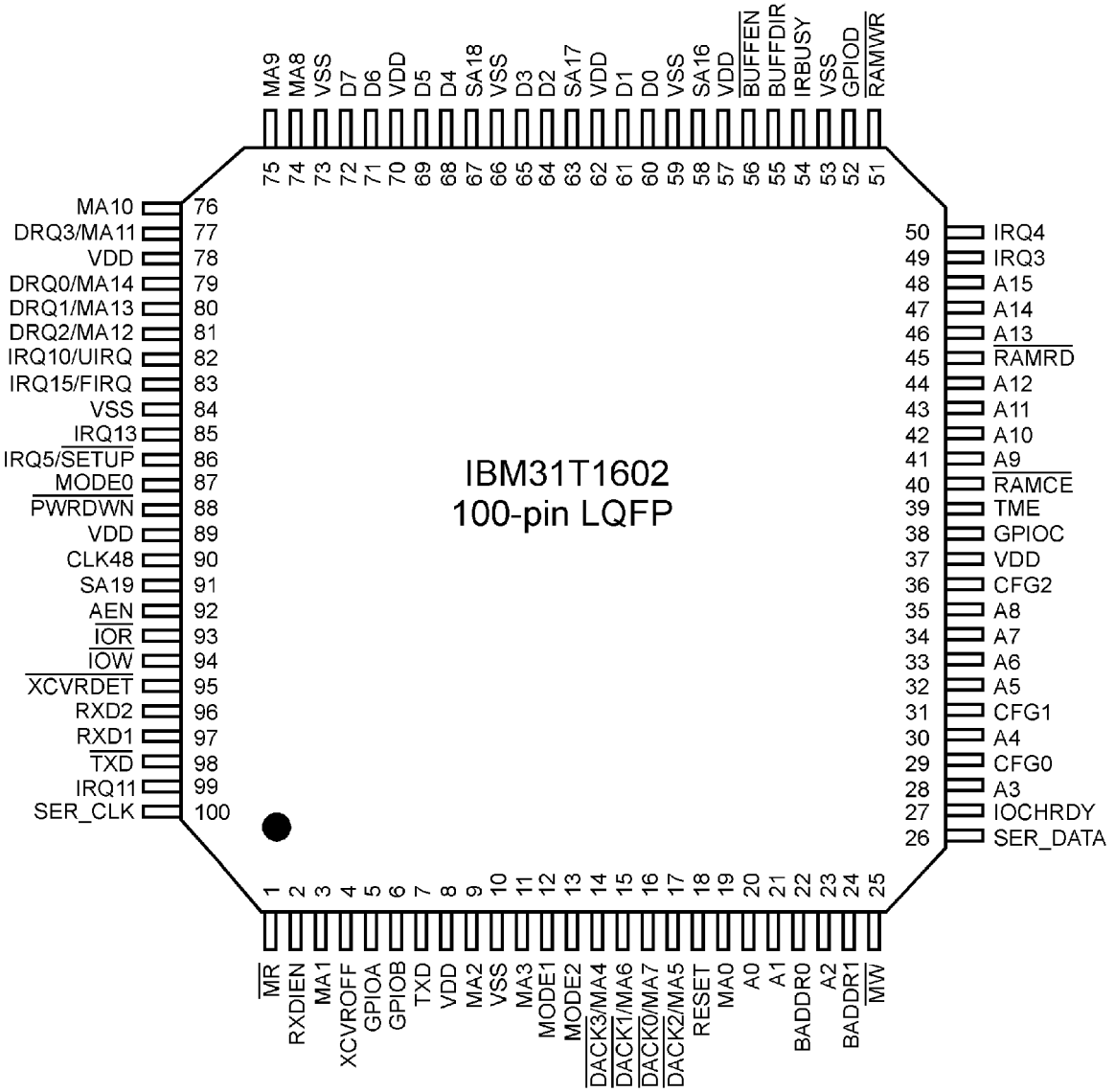
1.9. Power Management Feature

The IBM31T1602 powerdown operates two ways: complete shutdown or partial shutdown. In complete shutdown mode, clocks to all subsystems are disabled and minimum power dissipation is achieved. In partial shutdown mode, the subsystem that is not enabled or not in 'action' has its clocks disabled, leaving only the functional unit consuming required power.

To put the IBM31T1602 in complete powerdown mode, set En Power Down (b1 of the Power Down Register) to 1 and set Power Down (b0 of the Power Down Register) to 1, or activate (set low) the PWRDWN pin (this consumes the least amount of power); or, set En Infrared (b0 of the Infrared Configuration Register) to 0.

For partial powerdown mode, set En Power Down to 1, (the default value upon reset). Then, only the circuit that provides the function selected by the Infrared Configuration 1 Register will be active; the others will automatically shut down.

1.10. Pin Descriptions



1.10.1. IBM31T1602 Pin Descriptions

Table 1-2 (Page 1 of 6) Interface Configuration Signals

Signal	Pin	Type	Description
BADDR1 -BADDR0	24, 22	I	Base Address Select. Select one of four base addresses of the index and data ports which are used in accessing indirect configuration registers. BADDR1-BADDR0 inputs are used only in Indirect Configuration mode
CFG2 -CFG0	36, 31, 29	I	Default Register Configuration Select. Sampled during an active chip reset cycle and in conjunction with MODE inputs, select the default settings of the indirect configuration registers. CFG2-CFG0 inputs are used only in Indirect Configuration mode.
A15 - A0	48, 47, 46, 44, 43, 42, 41, 35, 34, 33, 32, 30, 28, 23, 21, 20	I	System Address. 16-bit address bus provides addressing of IBM31T1602 registers and shared memory.

Table 1-2 (Page 2 of 6) Interface Configuration Signals

Signal	Pin	Type	Description
D7 - D0	72, 71, 69, 68, 65, 64, 61, 60	B	System Data. 8-bit bidirectional system data bus transfers data between the IBM31T1602, host processor, and external SRAM device. The data lines are tristated when not being driven.
$\overline{\text{IOR}}$	93	I	I/O Read. This active-low input is asserted by the host processor during reads from the IBM31T1602
$\overline{\text{IOW}}$	94	I	I/O Write. This active-low input by the host processor during writes to the IBM31T1602.
AEN	92	I	Address Enable. When AEN is high, the host DMA controller has control of the ISA bus. AEN must be low before programmed I/O or shared memory accesses can be made to the IBM31T1602.
IOCHRDY	27	O	I/O Channel Ready. When driven low, this output extends I/O and memory bus cycles. It is only used in Shared Memory mode. In Host DMA mode, IOCHRDY is tristated.
IRQ3, IRQ4, IRQ11, IRQ13	49, 50, 99, 85	O	Interrupt Request. When active, either the UART or the FIR Controller is requesting service. These IRQs normally operate in pulse mode. Advanced interrupt configuration provides the capability to change these IRQs to active-low interrupts. Advanced interrupt configuration also provides independent routing of UART and FIR Controller internal IRQ lines. These IRQs are tristated when they are not being driven.
IRQ10/UIRQ	82	O	IRQ10/UART Subsystem Interrupt Request. In Indirect Configuration mode, UAIRQ is a pulse-mode interrupt. In Direct Configuration mode, UAIRQ is an active-high interrupt. By using advanced interrupt configuration, both the UART and FIR Controller can share the single UAIRQ line. Also, advanced interrupt configuration provides the capability to change UAIRQ to an active-low interrupt. UAIRQ is tristated when not being driven. In Plug and Play mode, this pin functions as IRQ10.
IRQ15/FIRQ	83	O	IRQ15/FIR Controller Interrupt Request. In Indirect

Table 1-2 (Page 2 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
			Configuration mode, FIRQ is a pulse-mode interrupt. In Direct Configuration mode, FIRQ is an active-high interrupt. By using advanced interrupt configuration, both the UART and FIR Controller can share the single FIRQ line. Also, advanced interrupt configuration provides the capability to change FIRQ to an active-low interrupt. FIRQ is tristated when not being driven. In Plug and Play mode, this pun functions as IRQ15.
DRQ3 - DRQ0	77, 81, 80, 79	O	DMA Request. Used to request a data transfer from the host DMA controller. Up to two DMA request lines, one for transmit and one for receive, may be used (selected during configuration). The remaining DMA request lines are tristated. DRQ3-DRQ0 are used only in Host DMA mode. In Shared Memory mode, these pins become MA14-MA11.
Table 1-2 (Page 3 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
$\overline{\text{DACK3}}$ $\overline{\text{DACK0}}$	14, 17, 15, 16	I	DMA Acknowledge. When active, indicate the host DMA controller is acknowledging a corresponding DMA request (DRQ3 – DRQ0). Up to two DMA acknowledge lines, one for transmit and one for receive, may be used (selected during configuration). $\overline{\text{DACK3}}$ - $\overline{\text{DACK0}}$ lines are used only in Host DMA mode. In Shared Memory mode, these pins act as output pins for MA4-MA7.
SA19 - SA16	91, 67, 63, 58	I	Extended System Address. Extension to System Address bus. Used to address shared memory. **Note:** The host memory window must be enabled. Also, the IBM31T1602 controller does not latch address bits 16 through 19 and so these pins must be connected to the appropriate SA address lines on the ISA and not the LA address lines. In Host DMA mode these pins are ignored.
$\overline{\text{RAMCE}}$	40	O	RAM Chip Enable. This active-low output is asserted by the IBM31T1602 when performing reads and writes to an external SRAM device. $\overline{\text{RAMCE}}$ is used only in Shared Memory mode. In Host DMA mode, $\overline{\text{RAMCE}}$ is tristated.
$\overline{\text{RAMRD}}$	45	O	RAM Read. This active-low output is asserted by the IBM31T1602 when reading from an external SRAM device. $\overline{\text{RAMRD}}$ is used only in Shared Memory mode. In Host DMA mode, $\overline{\text{RAMRD}}$ is tristated.
$\overline{\text{RAMWR}}$	51	O	RAM Write. This active-low output is asserted by the IBM31T1602 when writing to an external SRAM device. RAMWR is used only in Shared Memory mode. In Host DMA mode, RAMWR is tristated.
BUFFDIR	55	O	Buffer Direction. Controls the direction of data when

Table 1-2 (Page 2 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
			external bidirectional drivers are used for the data pins. BUFFDIR is active when: The host processor is reading from an internal IBM31T1602 register The host DMA controller is reading from the IBM31T1602 FIR controller (Host DMA mode) The host processor is reading from an external SRAM device (Shared Memory mode)

Table 1-2 (Page 4 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
$\overline{\text{BUFFEN}}$	56	O	Buffer Enable. This active-low output can be used to enable external bidirectional drivers for the IBM31T1602 data pins. $\overline{\text{BUFFEN}}$ is active when: The IBM31T1602 is being accessed by the host processor The IBM31T1602 is being accessed by the host DMA controller in Host DMA mode An external SRAM device is being accessed by the host processor in Shared Memory mode **Note:** An external bidirectional driver is required for Shared Memory mode.
MA14 - MA0	79, 80, 81, 77, 76, 75, 74, 16, 15, 17, 14, 11, 9, 3, 19	O	Shared Memory Address. When the &chip. is operating in Shared Memory mode, these address lines are used to address an external SRAM device. MA3-MA0 and MA10-MA8 pins are tristated in Host DMA mode.
$\overline{\text{MR}}$	1	I	Memory Read. This active-low input is asserted by the host processor when performing memory reads. $\overline{\text{MR}}$ is used only in Shared Memory mode.
$\overline{\text{MW}}$	25	I	Memory Write. This active-low input is asserted by the host processor when performing memory writes. $\overline{\text{MW}}$ is used only in Shared Memory mode.
IRQ5/$\overline{\text{SETUP}}$	86	B	IRQ5/Setup Register Access. This active-low input is used only when making I/O accesses to direct configuration registers. When $\overline{\text{SETUP}}$ is active, the lower three bits of the address bus are decoded to access one of eight direct configuration registers. $\overline{\text{SETUP}}$ must be inactive when performing all other I/O accesses. $\overline{\text{SETUP}}$ is used only in Direct Configuration mode. In Plug and Play mode, this pin is configured like all IRQs. It is selectable with advanced configuration in Indirect Configuration mode, and functions as the setup line in Direct Configuration mode.
$\overline{\text{PWRDWN}}$	88	I	External Power Down. This active-low input is used in

Table 1-2 (Page 4 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
			powering down the IBM31T1602 The power-down feature must be enabled before activating $\overline{\text{PWRDWN}}$
IRBUSY	54	O	IR Busy. When active, indicates that the IBM31T1602 is busy.
SER_DATA	26	B	Serial PROM Data. This bidirectional pin is used in transferring data between the IBM31T1602 and an external serial PROM device.
SER_CLK	100	O	Serial PROM Clock. This output is used to drive the serial clock of an external serial PROM device.
CLK48	90	I	Chip Clock. 48 MHz oscillator input.

Table 1-2 (Page 5 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
RESET	18	I	Chip Reset. Resets all internal registers and configuration settings. RESET must be held active for at least 500 ms to ensure proper reset of the controller
MODE2 - MODE0	13, 12, 87	I	Mode Select. These inputs select the bus and memory configuration. The following describes the mode pin settings for the bus configuration: MODE2 MODE1 MODE0 Configuration Mode --- 0 0 0 ISA Direct Configuration, Host DMA 0 0 1 ISA Direct Configuration, Shared Memory 0 1 0 ISA Indirect Configuration, Host DMA 0 1 1 ISA Indirect Configuration, Shared Memory 1 0 0 ISA Plug and Play, Host DMA 1 0 1 Reserved 1 1 0 ISA Plug and Play, Shared Memory 1 1 1 Reserved
TXD	7	O	Transmit Data. Transmits infrared serial data. Connects directly to the transmit data input of the infrared transceiver module.
$\overline{\text{TXD}}$	98	O	Transmit Data. This negative-going output may be used with the TXD pin to provide a transmit differential output pair.
RXD1	97	I	Receive Data 1. This input receives TTL-recovered serial data. Connects directly to the receive data output of the infrared transceiver module. It can be programmed to receive active-low or active-high pulses for receive data. This receive data channel or Receive Data Channel 2 can be selected as the active channel by software control.
RXD2	96	I	Receive Data 2. This input receives TTL-recovered serial data. Connects directly to the receive data output of the infrared transceiver module. It can be programmed to receive active-low or active-high pulses for receive data. This receive data channel or Receive Data Channel 1 can be selected as the active channel by software control. This second receive data channel is useful when interfacing to IR transceivers that have two receive channels, for instance one for low-speed IrDA data and one for high-speed IrDA data.
XCVROFF	4	O	Transceiver Off. Connects to the power-down control input of the external infrared transceiver. Alternatively, it may be used to control external circuitry which provides power

Table 1-2 (Page 5 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
			directly to the transceiver.
$\overline{\text{XCVRDET}}$	95	I	Transceiver Detect. Senses the presence of an external infrared transceiver. The programmer may use this to generate hardware interrupts to dynamically power the transceiver on and off. **Note:** If using XCVROFF and at the same time not requiring the $\overline{\text{XCVRDET}}$ function, then the $\overline{\text{XCVRDET}}$ pin must be tied low.
GPIO_A - GPIO_D	5, 6, 38, 52	B	General Purpose Inputs/Outputs. These pins may be used for external infrared transceiver module control. These pins are controlled through internal registers.

Table 1-2 (Page 6 of 6) Interface Configuration Signals			
Signal	**Pin**	**Type**	**Description**
RXDIEN	2	I	Receiver Driver Inhibit Enable. This input is for manufacturing test purposes only and must be tied to ground under normal operation.
TME	39	I	Test Mode Enable. This input is for manufacturing test purposes only and must be tied to ground under normal operation.
VDD	8, 37, 57, 62, 70, 78, 89	P	Digital Supply. Connect to +3.3V power supply.
VSS	10, 53, 59, 66, 73, 84	P	Digital Ground.
I = Input, O = Output, B = Bidirectional, P = Power			

1.11. Register Summary

The following tables provide a summary of the IBM31T1602 registers.

1.11.1. Plug and Play Register Summary

Table 1-3 Plug and Play Register Summary			
Configuration Location	**Register Name**	**R/W (in CONFIG STATE)**	**Power-on Value (CONFIG STATE)**
0x00	Set Read Data Port Address	W	N/A
0x01	Serial Isolation Register	R	variable
0x02	Configuration Control Register	W	N/A
0x03	Wake Command Register	W	N/A
0x04	Resource Data Register	R	variable
0x05	Status Register	R	variable
0x06	Card Select Number Register	R/W	N/A
0x07	Logical Device Number Register	R	00
0x30	Activate Register	R/W	00
0x31	I/O Range Check Register	R/W	00
0x38	Power Management Register	R/W	02
0x40	Shared Memory Base Address Bits 23:16 Register	R/W	00
0x041	Shared Memory Base Address Bits 15:8 Register	R/W	00
0x42	Shared Memory Control Register	R	00

Table 1-3 Plug and Play Register Summary			
Configuration Location	**Register Name**	**R/W (in CONFIG STATE)**	**Power-on Value (CONFIG STATE)**
0x043	Shared Memory Range/Limit Bits 23:16 Register	R	FF
0x44	Shared Memory Range/Limit Bits 15:8 Register	R	E0
0x60	UART Base Address Upper Byte Register	R/W	00
0x61	UART Base Address Lower Byte Register	R/W	00
0x62	FIR Subsystem Base Address Upper Byte Register	R/W	00
0x63	FIR Subsystem Base Address Lower Byte Register	R/W	00
0x70	UART IRQ Select Configuration Register	R/W	00
0x71	UART IRQ Type Configuration Register	R/W	02
0x72	FIR Subsystem IRQ Select Configuration Register	R/W	00
0x73	FIR Subsystem IRQ Type Configuration Register	R/W	02
0x74	First DMA Channel Configuration Register	R/W	04
0x75	Second DMA Channel Configuration Register	R/W	04

1.11.2.

1.11.3. Indirect Configuration Register Summary

Table 1-4 Indirect Configuration Register Summary			
Index	**Register**	**Register Name**	**R/W**
0x02	PDR	Power Down Register	R/W
0x08	IDR	Identification Register	R
0xA2	DLS SMBA	DMA Line Select Register (Host DMA mode) Shared Memory Base Address Register (Shared Memory mode)	R/W R/W
0xA3	IRC	Infrared Control Register	R/W
0xA4	UARTH	UART High Address Register	R/W
0xA5	UARTL	UART Low Address Register	R/W
0xA6	FIRH	FIR High Address Register	R/W
0xA7	FIRL	FIR Low Address Register	R/W

See Appendix C, “Indirect Configuration Register Default Settings” on page C-1 for the default settings of indirect configuration registers.

1.11.4. Direct Configuration Register Summary

Table 1-5 Direct Configuration Register Summary			
Address	**Register**	**Register Name**	**R/W**
0x0	ID0	Identification 0 Register	R
0x1	ID1	Identification 1 Register	R
0x2	SET	Setup Register	R/W
0x3	UARTL	UART Low Address Register	R/W
0x4	UARTH	UART High Address Register	R/W
0x5	FIRL	FIR Low Address Register	R/W
0x6	FIRH	FIR High Address Register	R/W
0x7	LDMAC	Local DMA Control Register	R/W

1.11.5. UART Control Register Summary

Table 1-6 UART Control Register Summary

DLAB	A2-A0	Register	Register Name	R/W
0	0x0	RBR	Receiver Buffer Register	R
0	0x0	THR	Transmitter Holding Register	W
0	0x1	IER	Interrupt Enable Register	R/W
X	0x2	IIR	Interrupt Identification Register	R
x	0x2	FCR	FIFO Control Register	W
x	0x3	LCR	Line Control Register	R/W
x	0x4	MCR	Modem Control Register	R/W
x	0x5	LSR	Line Status Register	R/W
x	0x6	MSR	Modem Status Register	R/W
x	0x7	SCR	Scratch Register	R/W
1	0x0	DLL	Divisor Latch LSB	R/W
1	0x1	DLM	Divisor Latch MSB	R/W

See Appendix D, "UART Information" on page D-1 for the default settings of the UART control registers.

1.11.6. FIR Control Register Summary

Table 1-7 (Page 1 of 2) FIR Control Register Summary

Bank	Address	Register Name	R/W
0	0x0	Master Control Register	R/W
0	0x1	Master Status Register	R
0	0x1	Miscellaneous Control Register	W

Table 1-7 (Page 2 of 2) FIR Control Register Summary

Bank	Address	Register Name	R/W
0	0x2	RxFIFO Register	R
0	0x2	TxFIFO Register	W
0	0x3	TxControl 1 Register	R/W
0	0x4	TxControl 2 Register	R/W
0	0x5	TxStatus Register	R
0	0x6	RxControl Register	R/W
0	0x7	RxStatus Register	R
0	0x7	Reset Command Register	W
1	0x0	Master Control Register	R/W
1	0x1	Frame Address Register	R/W
1	0x2	Rx Byte Count Low Register	R
1	0x3	Rx Byte Count High Register	R
1	0x4	Rx Ring Frame Pointer Low Register	R
1	0x5	Rx Ring Frame Pointer High Register	R
1	0x6	Tx Byte Count Low Register	R/W
1	0x7	Tx Byte Count High Register	R/W
2	0x0	Master Control Register	R/W
2	0x1	Infrared Configuration 1 Register	R/W
2	0x2	Infrared Transceiver Control Register 1	R/W
2	0x3	Infrared Transceiver Control Register 2	R/W
2	0x4	Timer Register	R/W
2	0x5	Infrared Configuration 3 Register	R/W
2	0x6	Modem Tuning Register	R/W
2	0x7	Reserved	
3	0x0	Master Control Register	R/W
3	0x1	Shared Memory Page Register	R/W
3	0x2	TxDMA Start Address Low Register	R/W
3	0x3	TxDMA Start Address High Register	R/W

Table 1-7 (Page 1 of 2) FIR Control Register Summary			
Bank	**Address**	**Register Name**	**R/W**
3	0x4	Reserved	
3	0x5	Reserved	
3	0x6	Reserved	
3	0x7	Revision ID Register	R

Note: Shared Memory Page Register and TxDMA Start Address Registers of Bank 3 are part of the DMA Control subsystem and therefore accessible only in Shared Memory mode.

2 IBM31T1602 Operational Modes

2.1. Overview

The IBM31T1602 can be configured to operate in six different modes. These modes determine the nature of the controller's configuration registers and how these registers are programmed as well as the way that infrared data is transferred between the host CPU and the infrared controller for the high-speed modes (1.152 Mbits/s and 4 Mbits/s).

Table 2-2 Operational Modes

MODE2 (Pin 13)	MODE1 (Pin 12)	MODE0 (Pin 87)	Configuration Mode	Fast IR Data Transfer Method
0	0	0	Direct Configuration	Host DMA
0	0	1	Direct Configuration	Shared Memory
0	1	0	Indirect Configuration	Host DMA
0	1	1	Indirect Configuration	Shared Memory
1	0	0	Plug and Play Configuration	Host DMA
1	1	0	Plug and Play Configuration	Shared Memory

Legend:

Direct Configuration

Configuration registers are directly accessible in I/O space using an external address decoder.

Indirect Configuration

Configuration registers are accessible using indexed addressing via two I/O ports, an index port and a data port.

Plug and Play Configuration

The configuration register set and access to these registers conform to the Plug and Play ISA Specification Version 1.0a.

Host DMA

Use DMA cycles to transfer data to and from the IBM31T1602's internal FIFO and the host system's memory. Operation may be set up to use two DMA channels or a single DMA channel.

Shared Memory

Use RAM local to the controller to transfer data. The RAM is mapped into the host system's memory space. Both the host and the IBM31T1602 controller may read from and write to this RAM.

Notes on the MODE Pins:

Combinations of the states of the mode pins not listed in

2.2. Plug and Play Configuration

See 4.1, "Plug and Play Mode" on page 4-1.

2.3. Indirect Configuration - Host DMA

This configuration is shown below in Figure 2-1 on page 2-2. There are eight configuration registers which must be programmed prior to access of any of the IBM31T1602 subsystems. Access to these configurations is handled indirectly via two 8-bit I/O ports, an index port and a data port.

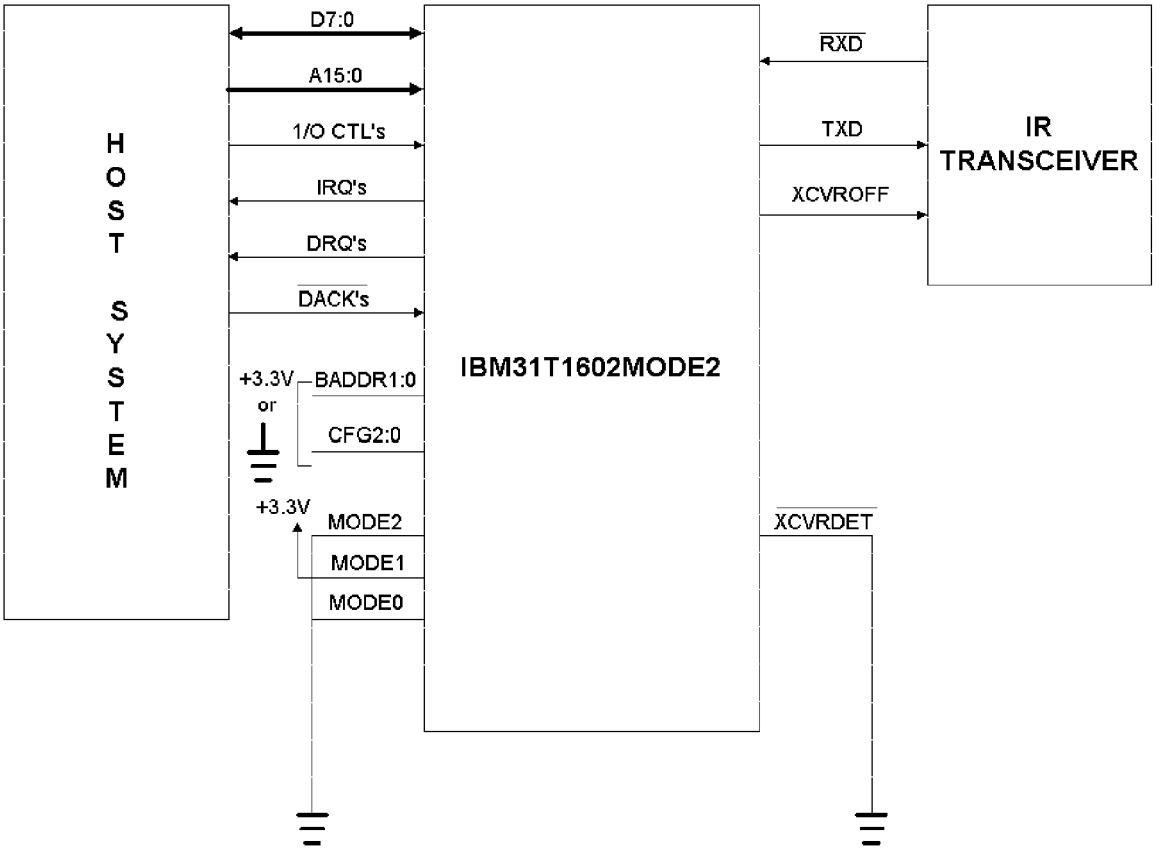


Figure 2-1. IBM31T1602 in ISA Indirect Configuration Mode – Host DMA

The IBM31T1602 configuration registers have default power-up settings, determined by the three CFG pins. The default settings are loaded into the configuration registers at the end of the reset cycle, at the falling edge of the RESET line. The configuration registers can be accessed and the default settings overwritten through a pair of I/O ports called the index port and the data port.

The index port is used to address the configuration registers. The data port is used to read from or write to the configuration register that is pointed to by the index port.

To write to a configuration register, the index value of the configuration register is written to the index port. Next, the 8-bit data value destined for the configuration register is loaded in two consecutive write accesses to the data port. To read from a configuration register, the index value of the configuration register is written to the index port, then data is read from the data port.

Note: Only two consecutive write operations to the data port can modify an indirect configuration register. This protection mechanism prevents accidental erasure of any previously set configuration data. A single read from the index or data port may be done at any time.

The table below shows four possible address locations of the index and data ports. The addresses are set by sampling the values on the BADDR0 and BADDR1 pins during power-on reset.

Table 2-2. Index and Data Port Locations

BADDR1	BADDR0	Index	Data
0	0	0398h	0399h
0	1	026Eh	026Fh
1	0	015Ch	015Dh
1	1	002Eh	002Fh

The index port location must be determined after power-on reset. This is done by reading all four index port addresses twice. After a hardware reset, the correct base address is determined if an 88h value is returned on the first read, and a DFh value on the second read. This will signify that the index port has been located successfully.

Reading the index port will return the currently stored index value. However, there may be cases where it is necessary to relocate the index port (e.g. after a soft reset). It is always possible to read out the identification values of 88h and DFh, not just immediately following a hardware reset. These ID bytes will be returned in sequence from the index port within a maximum of four consecutive reads. A read to the index port will return the current index value. A second read will also return the same index value. Further read operations will return the ID bytes of 88h and DFh. In this way, the ID bytes will always appear within four read operations. The reads must be consecutive - no write operations to the index port or read or write operations to the data port can be carried out in between the read operations to the index port.

To illustrate, if the value in the index port is index A3h, then consecutive read operations would return the following sequence of values: A3h, A3h, 88h, DFh, A3h, A3h, 88H, DFh, A3h, etc.

2.3.1. Indirect Configuration Characteristics

- Access to configuration registers through an index port and data port
- Four possible locations for the index port and data port
- No special signal or components required to access the configuration registers
- Default power-up configurations selectable using three configuration pins
- Shared memory, host DMA, or programmed I/O implementation available
- Four possible selectable ISA DMA channels
- Pulse-mode or level-mode interrupts
- UART interrupt and FIR subsystem interrupt can be directed to any one of four IRQ pins; a merged interrupt is also selectable

As noted, IBM31T1602 has the ability to enter a default configuration on power-up. This is accomplished with the CFG pins. The next section describes the different default configurations for ISA Indirect Configuration Host DMA mode.

2.3.2. Configuration Register Power-up Defaults - Indirect Configuration, Host DMA Mode

Table 2-3 lists the power-up default values for all eight of the configuration registers as determined by the state of the three CFG pins. Note that the three configuration pins yield eight possible power-up scenarios.

Relevant IBM31T1602 pins:
MODE2 (pin 13) = 0
MODE1 (pin 12) = 1
MODE0 (pin 87) = 0
CFG2 (pin 36) = see table below
CFG1 (pin 31) = see table below
CFG0 (pin 29) = see table below

Table 2-3. (Page 1 of 2) Power-up Default Values for the Configuration Registers, Host DMA Mode

Configuration Pins			**Register Values at Power-Up**							
2	**1**	**0**	**PDR (Index 02h)**	**IDR (Index 08h)**	**DLS (Index A2h)**	**IRC (Index A3h)**	**UARTH (Index A4h)**	**UARTL (Index A5h)**	**FIRH (Index A6h)**	**FIRL (Index A7h)**
0	0	0	02h	E2h	00h	04h	03h	F8h	03h	00h
0	0	1	02h	E2h	00h	05h	03h	F8h	03h	00h
0	1	0	02h	E2h	00h	01h	02h	F8h	03h	00h

0	1	1	02h	E2h	00h	05h	03h	E8h	03h	10h

Table 2-3. (Page 1 of 2) Power-up Default Values for the Configuration Registers, Host DMA Mode

Configuration Pins			**Register Values at Power-Up**							
2	**1**	**0**	**PDR (Index 02h)**	**IDR (Index 08h)**	**DLS (Index A2h)**	**IRC (Index A3h)**	**UARTH (Index A4h)**	**UARTL (Index A5h)**	**FIRH (Index A6h)**	**FIRL (Index A7h)**
1	0	0	02h	E2h	00h	01h	02h	E8h	03h	10h
1	0	1	02h	E2h	00h	05h	03h	38h	03h	30h
1	1	0	02h	E2h	01h	01h	02h	F8h	03h	00h
1	1	1	02h	E2h	21h	01h	02h	F8h	03h	00h

Note that the PDR register always powers-up with a value of 02h. This indicates that the Enable Power Down bit is set while all other bits are not set. The IDR register is a read-only register which will always return the same value, in this case E2h, to signify host DMA mode. For the remaining six registers, refer to Table 2-4 on page 2-4 for an interpretation of the power-up settings.

Table 2-4. Host DMA Mode Configuration Settings on Power-up

Configuration Pins			IBM31T1602 Configuration								
2	1	0	Controller IR Core	UART Subsystem Address Range	UART at Std. ISA Port	FIR Subsystem Address Range	Internal DMA Channel 1 Mapping (see note 1)	Internal DMA Channel 2 Mapping (see note 2)	Pins Carrying Interrupts for the UART and FIR Subsystems (see note 3)		Shared UART/FIR Subsystem Interrupt Pin
0	0	0	Disabled (see note 4)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0	0	1	Enabled	03F8-03FFh	COM1	0300-0307h	None	None	UIRQ	FIRQ	IRQ4
0	1	0	Enabled	02F8-02FFh	COM2	0300-0307h	None	None	UIRQ	FIRQ	IRQ3
0	1	1	Enabled	03E8-03EFh	COM3	0310-0317h	None	None	UIRQ	FIRQ	IRQ4
1	0	0	Enabled	02E8-02EFh	COM4	0310-0317h	None	None	UIRQ	FIRQ	IRQ3
1	0	1	Enabled	0338-033Fh	non-standard	0330-0337h	None	None	UIRQ	FIRQ	IRQ4
1	1	0	Enabled	02F8-02FFh	COM2	0300-0307h	DRQ0	None	UIRQ	FIRQ	IRQ3
1	1	1	Enabled	02F8-02FFh	COM2	0300-0307h	DRQ0	DRQ1	UIRQ	FIRQ	IRQ3

Note:

Internal DMA channel 1 can be configured for either receive or transmit operation. This is determined by a register in the FIR subsystem of the IBM31T1602. The mapping listed above indicates the external pins that the internal channel is mapped to. Note that the corresponding $\overline{\text{DACKn}}$ is also mapped: DRQ0 means DRQ0 is mapped for the request line and $\overline{\text{DACK0}}$ is mapped for the acknowledge line, for example.

Internal DMA channel 2 is a second internal DMA channel that can be used for dual DMA channel operation (transmit only). The mapping listed above indicates the external pins that internal DMA channel 2 is mapped to. An entry of DRQ1 means that $\overline{\text{DACK1}}$ is also mapped for the acknowledge line.

Advanced Interrupt Configuration is disabled in all cases. In addition, all interrupts are generated in pulse mode, including the shared UART/FIR subsystem interrupt.

The infrared controller is disabled and its subsystems are in a power-down state in this configuration. All other entries for this setting are not applicable (N/A).

The IBM31T1602's core subsystems are disabled and powered-down when all CFG pins are 0.

In the next five cases (rows 2 to 6 of the table), neither of the internal DMA channels are mapped to any of the external DMA request or acknowledge pins of the IBM31T1602. While the UART subsystem is accessible and readily usable for communication at data rates of up to 115.2 kbits/s, FIR communication cannot take place using host DMA immediately. To operate at fast IR data rates, software needs to map one or both of the internal DMA channels to a free external DMA channel via the DLS register and write an appropriate value to the FIR subsystem's Miscellaneous Control Register to select dual DMA channel or single DMA channel operation. Programmed I/O can be used as an alternative to host DMA.

In the second to last case in the table (row 7), only internal DMA channel 1 is mapped to an external DMA channel. This implies single DMA channel operation. Software would be required to toggle the usage of this internal channel back and forth from receive to transmit operation via the Miscellaneous Control Register, as needed.

In the final configuration case in the table, both internal DMA channels are routed to external DMA channels. This can be done for dual DMA channel operation using the Miscellaneous Control Register. In dual DMA channel mode, channel 1 can only be used for receive and channel 2 for transmit. Therefore, in this case, receive is handled by DRQ0 and $\overline{\text{DACK0}}$, while transmit is handled by DRQ1 and $\overline{\text{DACK1}}$.

In all eight cases, the value in any of the configuration registers (except the IDR register) may be changed after power-up by accessing the configuration registers and overwriting the stored value.

2.4. Indirect Configuration - Shared Memory

This configuration is similar to the ISA Indirect Configuration Host DMA mode in that it also uses indexed addressing to access the controller's configuration registers. The difference is that an external local SRAM must be used for temporary data storage. The width of the system address bus is now 20 bits to address the shared memory.

The DRQ and $\overline{\text{DACK}}$ lines are reconfigured in this mode as local memory address lines. The IBM31T1602 will generate the local memory address (MA14:0), the local RAM read $\overline{\text{(RAMRD)}}$, the local RAM write $\overline{\text{(RAMWR)}}$ and RAM select $\overline{\text{(RAMCE)}}$ lines. The data bus is shared with the host and isolated by a bidirectional buffer controlled by the IBM31T1602 via the $\overline{\text{BUFFEN}}$ and BUFFDIR lines. With the local data bus (D7:0), buffered from the host system data bus (SD7:0) local transmit and receive operations can take place without tying up the host system data bus. The IBM31T1602 will arbitrate control of the data bus in cases where the host system and the IBM31T1602's own FIR subsystem request this bus at the same time.

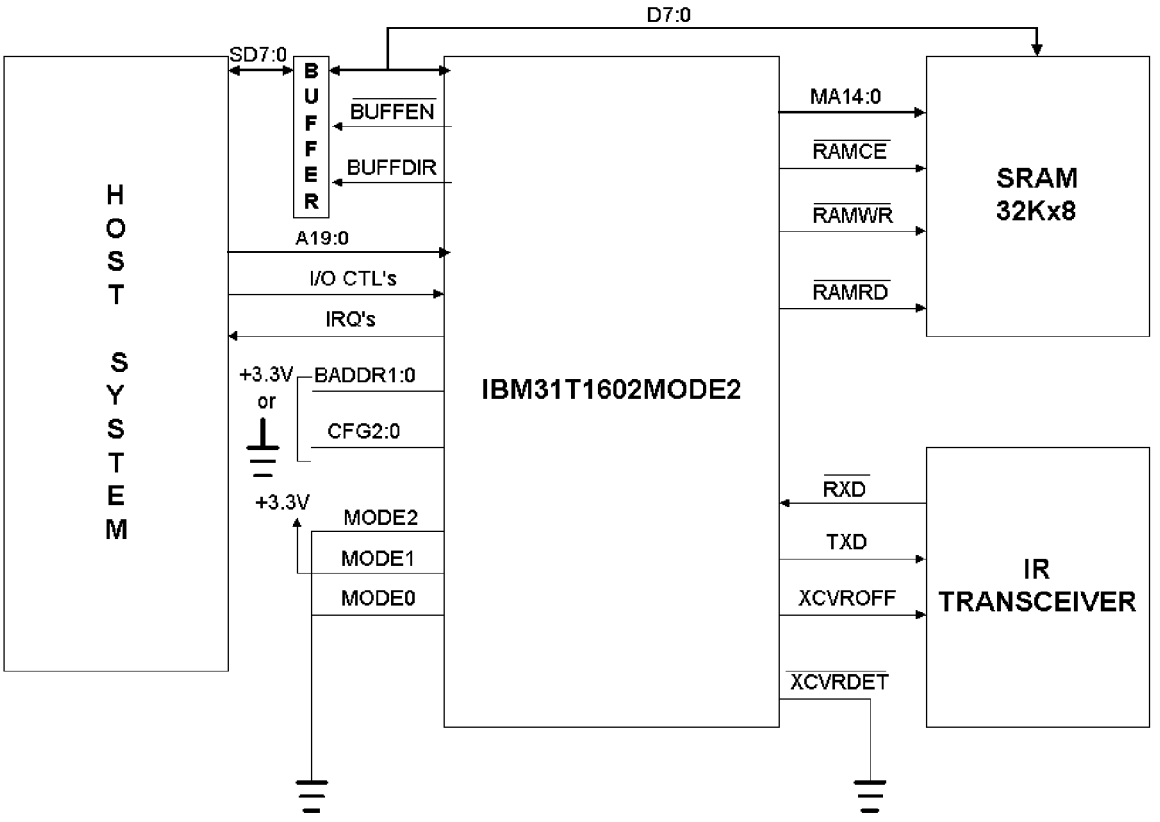


Figure 2-2. IBM31T1602 in ISA Indirect Configuration Mode – Shared Memory

For transmit operations, the host system loads the packet to be transmitted into the local SRAM through memory write instructions. When the data transmission is ready to take place, the IBM31T1602 fetches the packet from the local memory buffer and sends it to the transceiver. Similarly, for receive operations, the IBM31T1602 controller writes data received from the transceiver into the local SRAM. When a complete packet has been received, the IBM31T1602 interrupts the host system, at which point the host reads the packet out of memory.

A shared memory page register is used to control paging of the SRAM into an 8-Kbyte memory window in host system memory space. The maximum size of the SRAM is 32 Kbytes; smaller memory sizes will result in address shadowing. The 8-Kbyte memory window is divided into two pages of 4 Kbytes, the upper for data transmission and the lower for data reception. The upper 4-Kbyte block of memory maps into the upper 16 Kbytes of the SRAM's 32-Kbyte space (4000h-7FFFh), while the lower 4-Kbyte receive buffer maps into the lower 16 Kbytes of the 32-Kbyte SRAM (0000h-3FFFh). The pages may start on any 1-Kbyte boundary.

The next section describes the power-up default configurations for the ISA Indirect Configuration Shared Memory mode.

2.4.1. Configuration Register Power-up Defaults - Indirect Configuration, Shared Memory Mode

Table 2-5 on page 2-6 lists the power-up default values for all eight of the configuration registers as determined by the state of the three CFG pins. Note that the three configuration pins yield eight possible power-up scenarios.

Relevant IBM31T1602 pins:
MODE2 (pin 13) = 0
MODE1 (pin 12) = 1
MODE0 (pin 87) = 1
CFG2 (pin 36) = see table below
CFG1 (pin 31) = see table below
CFG0 (pin 29) = see table below

Table 2-5. Power-up Default Values for the Configuration Registers, Shared Memory Mode (ISA, Indirect Config.)

Configuration Pins			**Register Values on Power-Up**							
2	**1**	**0**	**PDR (Index 02h)**	**IDR (Index 08h)**	**DLS (Index A2h)**	**IRC (Index A3h)**	**UARTH (Index A4h)**	**UARTL (Index A5h)**	**FIRH (Index A6h)**	**FIRL (Index A7h)**
0	0	0	02h	E3h	00h	04h	03h	F8h	03h	00h
0	0	1	02h	E3h	00h	05h	03h	F8h	03h	00h
0	1	0	02h	E3h	00h	01h	02h	F8h	03h	00h
0	1	1	02h	E3h	00h	05h	03h	E8h	03h	10h
1	0	0	02h	E3h	C8h	21h	02h	E8h	03h	10h
1	0	1	02h	E3h	D0h	25h	03h	E8h	03h	10h
1	1	0	02h	E3h	C4h	21h	02h	F8h	03h	00h
1	1	1	02h	E3h	D4h	21h	02h	F8h	03h	00h

The PDR register always powers-up with a value of 02h. This indicates that the Enable Power Down bit is set and all other bits are not set (see the *Softwre Reference Guide* for a description of the other bits). The IDR register, a read-only register, will always return the value of E3h, signifying shared memory mode. For the remaining six registers, refer to Table 2-6 for an interpretation of the power-up settings.

Table 2-6. (Page 1 of 2) Shared Memory Mode Configuration Settings on Power-up

Configuration Pins			2.4.1.1 IBM31T1602 Configuration								
2	1	0	Controller IR Core	UART Subsystem Address Range	UART at Std. ISA Port	FIR Subsystem Address Range	Host Memory Window	Shared Memory 8-Kbyte Window Address (see note 1)	Pins Carrying Interrupts for the UART and FIR Subsystems(see note 2)		Shared UART/FIR Subsystem Interrupt Pin
0	0	0	Disabled (see note 3)	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
0	0	1	Enabled	03F8-03FFh	COM1	0300-0307h	Disabled	N/A	UIRQ	FIRQ	IRQ4
0	1	0	Enabled	02F8-02FFh	COM2	0300-0307h	Disabled	N/A	UIRQ	FIRQ	IRQ3

Table 2-6. (Page 2 of 2) Shared Memory Mode Configuration Settings on Power-up

Configuration Pins			2.4.1.2 IBM31T1602 Configuration								
2	1	0	Controller IR Core	UART Subsystem Address Range	UART at Std. ISA Port	FIR Subsystem Address Range	Host Memory Window	Shared Memory 8-Kbyte Window Address (see note 1)	Pins Carrying Interrupts for the UART and FIR Subsystems(see note 2)		Shared UART/FIR Subsystem Interrupt Pin
0	1	1	Enabled	03E8-03EFh	COM3	0310-0317h	Disabled	N/A	UIRQ	FIRQ	IRQ4
1	0	0	Enabled	02E8-02EFh	COM4	0310-0317h	Enabled	C8000 - C9FFFh	UIRQ	FIRQ	IRQ3
1	0	1	Enabled	03E8-03EFh	COM3	0310-0317h	Enabled	D0000 - D1FFFh	UIRQ	FIRQ	IRQ4
1	1	0	Enabled	02F8-02FFh	COM2	0300-0307h	Enabled	C4000 - C5FFFh	UIRQ	FIRQ	IRQ3
1	1	1	Enabled	02F8-02FFh	COM2	0300-0307h	Enabled	D4000 - D5FFFh	UIRQ	FIRQ	IRQ3

Note:
If the host memory window is disabled, the shared memory window address is not applicable (N/A).
Advanced Interrupt Configuration is disabled in all cases. All interrupts are generated in pulse mode, including the shared UART/FIR subsystem interrupt.
The infrared controller is disabled and the subsystems are in a power-down state in this configuration. All other entries for this setting are not applicable (N/A).

Note that the IBM31T1602's core is powered-down when all of the CFG pins are 0 (first row of the table). All subsystems are disabled.

In the next three cases (rows 2 to 4), the host memory window is disabled. Therefore, while the UART subsystem is accessible and usable for communication at data rates of up to 115.2 kbits/s, FIR communication cannot take place using a shared memory architecture immediately. To operate at fast IR data rates, software is needed to set up a shared memory window base address in the DLS register and enable the host memory window via a bit in the IRC register. Otherwise, a programmed I/O approach could be used.

In the final four scenarios of Table 2-6, a shared memory window base address is set and the host memory window is enabled on a power-up. In all eight cases, the values in the configuration register may be changed after power-up.

2.5. Direct Configuration - Host DMA

This mode of configuration is similar to the one used in Micro Channel systems, where POS (configuration) registers are accessed by driving the $\overline{\text{SETUP}}$ line low during I/O cycles, and address lines A2:0 directly select one of eight configuration registers. Figure 2-3 on page 2-7 illustrates this configuration.

High-speed 1.152 Mbits/s or 4 Mbits/s IR data to be transmitted through the IR transceiver, and data that has been received via the infrared link, are transferred between the host system and the IBM31T1602 controller's FIFO using DMA cycles. Alternatively, a programmed I/O approach may be taken. For low-speed IR communications (115.2 kbits/s and below) the IBM31T1602's internal UART subsystem is compatible with an industry-standard 16550 or 16450 UART.

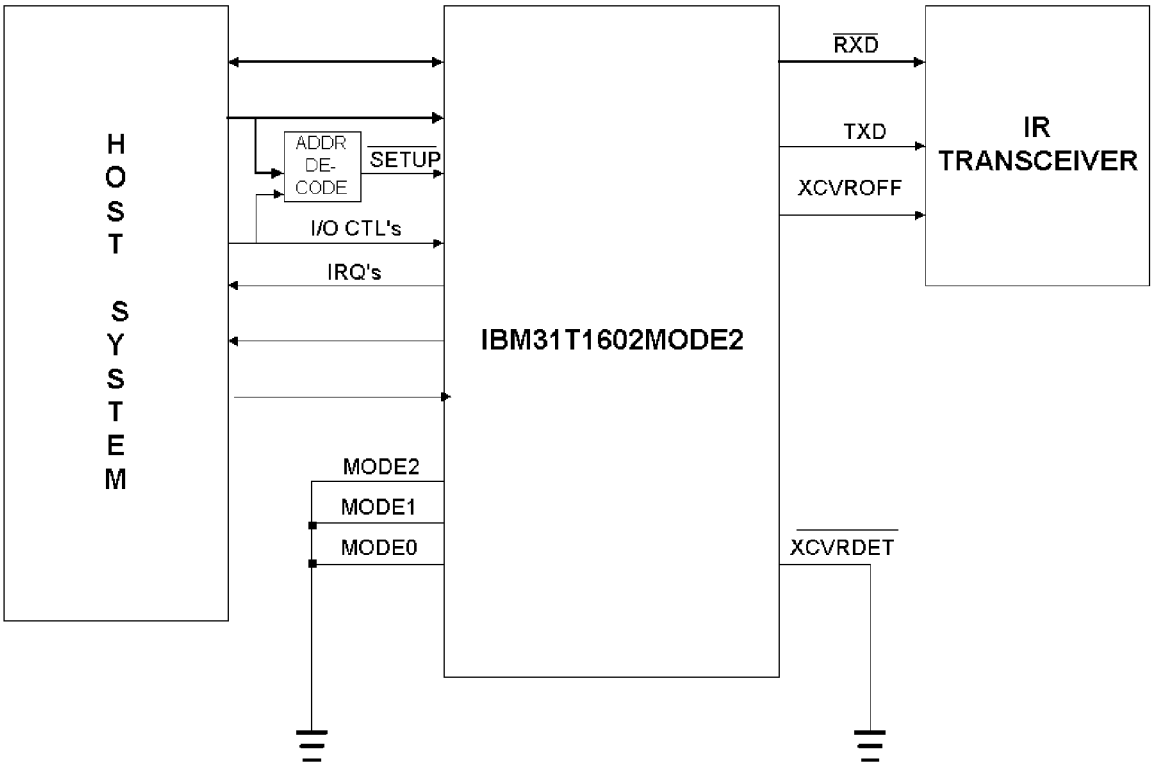


Figure 2-3. IBM13T1602 in ISA Direct Configuration Mode (Host DMA)

Note the $\overline{\text{SETUP}}$ line and address decoder in the above figure: the address decoder must be implemented so that $\overline{\text{SETUP}}$ is driven low for I/O accesses to the IBM31T1602 controller's eight configuration registers.

System address lines SA19:16 are not used in host DMA configuration. The address bus shown above is 16 bits wide (A15:0), which is sufficient for I/O addressing. The SA19:16 pins can be no-connects, or pulled low with individual pull-down resistors to fix their states (recommended). They should not be tied directly to GND as these pins are bidirectional and can be in an undetermined state until the controller is reset on power-up.

Note that the MODE pins are all tied low to set the controller to ISA Direct Configuration Host DMA mode.

2.5.1. Direct Configuration Characteristics

Full flexibility for location and access of configuration registers in I/O space

External logic required to implement and generate a $\overline{\text{SETUP}}$ signal, based on a desired address space
DMA cycles or programmed I/O used for high-speed data communication
Two possible selectable ISA DMA channels
Pulse-mode or level-mode interrupts
UART interrupt and FIR subsystem interrupt can be merged onto one IRQ line or left on separate IRQ lines

2.6. Host DMA Approach vs. Shared Memory Approach for Fast IR

Table 2-7. Host DMA Approach vs. Shared Memory Approach for Fast IR

Host DMA	**Shared Memory**
Uses DMA cycles (under control of the host system's DMA controller) for transfer of data from system memory to and from the controller's FIFO	Employs a local memory device which is mapped into the host system's memory map: memory read and write instructions are used by the host system to transfer data to and from the memory buffer; the controller uses its own internal control logic to move data back and forth from the memory buffer and its FIFO; thus, the memory buffer is shared memory, accessible by the host system and the controller
Requires minimal additional components; low cost	Requires local memory (32 Kbytes of SRAM recommended) plus bidirectional 8-bit data bus buffer
Uses DMA cycles, therefore control of the ISA bus must be taken away from the CPU for data transfers	CPU and ISA bus are not tied up when the controller is accessing the local memory; data bus is isolated so CPU is free for other tasks
Must use free ISA DMA channels; sometimes few channels are free	Requires an 8-Kbyte window in system memory space
Transmit/receive data is transferred once between system memory and the IBM31T1602 FIFO	Transmit/receive data is transferred twice, once between system memory and shared memory, and once between shared memory and the IBM31T1602 FIFO

3 Interfacing Optical Transceivers to the IBM31T1602

3.1. Overview

The IBM31T1602 is a digital controller ASIC with all the necessary logic to modulate and demodulate data according to industry-standard infrared communication protocols. The controller requires an external optical transceiver to convert its electrical output signals to infrared light, and incoming infrared light to electrical input signals.

To interface with optical transceivers, the IBM31T1602 has five dedicated I/O pins. In addition there are four General Purpose Input/Output pins and one Alternate Receiver Data pin that can be used if required. These pins are summarized below.

Table 3-1. Transceiver Interface Signals

Signal	Pin	Description
TXD	7	Transmit Data. Serial data output for information being transmitted. TXD = 1 indicates that the optical transceiver's LED should turn on to generate an infrared pulse. Note that the state of this signal can also be controlled by the state of bit b1 (TXD Force) in the Infrared Transceiver Control Register.
$\overline{\text{TXD}}$	98	Transmit Data. Serial data output for information being transmitted, but opposite in polarity to TXD. $\overline{\text{TXD}}$ = 0 signals the optical transceiver to generate an infrared pulse. In conjunction with TXD, $\overline{\text{TXD}}$ can be used to provide a differential signal pair.
RXD1	97	Receive Data 1. Serial data input channel 1 for information being received via the external optical transceiver. This channel can be programmed to interrupt RXD1=0 as the presence of an infrared pulse as detected by a transceiver, or to interrupt RXD1=1 as an infrared pulse via the Rx Invert bit in the Infrared Transceiver Control 2 Register.
RXD2	96	Receive Data 2. Serial data input channel 2 for information being received via the external optical transceiver. This channel can be programmed to interrupt RXD2=0 as the presence of an infrared pulse as detected by a transceiver, or to interrupt RXD2=1 as an infrared pulse via the Rx Invert bit in the Infrared Transceiver Control 2 Register.
XCVROFF	4	Transceiver Off. This signal is meant to be used to power-off (XCVROFF = 1) or power-on (XCVROFF = 0) an external optical transceiver. The state of this signal is controlled by the state of bit b4 in the Infrared Transceiver Control Register as long as the signal XCVRDET is low (indicating that a transceiver is present and detected). If XCVRDET is high (no transceiver present), then XCVROFF is automatically asserted (XCVROFF = 1).
$\overline{\text{XCVRDET}}$	95	Transceiver Detect. This input signal is used to indicate the presence ($\overline{\text{XCVRDET}}$ = 0) or absence ($\overline{\text{XCVRDET}}$ = 1) of an external optical transceiver. This can be useful for pluggable tethered transceivers. The state of this signal can be monitored via the read-only bit b4 in the Infrared Configuration 3 Register. Note that if the transceiver or other external hardware does not implement this signal, $\overline{\text{XCVRDET}}$ should be tied low if XCVROFF is to be used.
GPIO_A	5	General Purpose Input/Output A. A general purpose I/O signal, controlled by the state of bit b7 in the Infrared Transceiver Control Register.

GPIO_B	6	General Purpose Input/Output B. A general purpose I/O signal, controlled by the state of bit b6 in the Infrared Transceiver Control Register.
GPIO_C	38	General Purpose Input/Output C. A general purpose I/O signal, controlled by the state of bit b5 in the Infrared Transceiver Control Register.
GPIO_D	52	General Purpose Input/Output D. A general purpose I/O signal controlled by the state of bit b0 in the Infrared Transceiver Control Register.

3.2. Interfacing to Transceivers from IBM, Temic, Sharp, and Hewlett-Packard

The following sections describe how to interface five currently available IrDA transceivers to the IBM31T1602:
IBM31T1101 from IBM
IBM31T1100 from IBM
TFDS6000 from Temic **
RY5DD01A from Sharp **
HSDL-1100 from Hewlett-Packard **

3.3. Interface to the IBM31T1101 Transceiver

The IBM31T1101, IBM31T1100 and TFDS6000 transceivers have the same controller-transceiver electrical interface. The connection diagrams are shown in Figure 3-1 on page 3-2 and Figure 3-2 on page 3-3. The electrical interface to these transceivers consists of three signals: transmit data, receive data and a bandwidth-select/power-down pin.

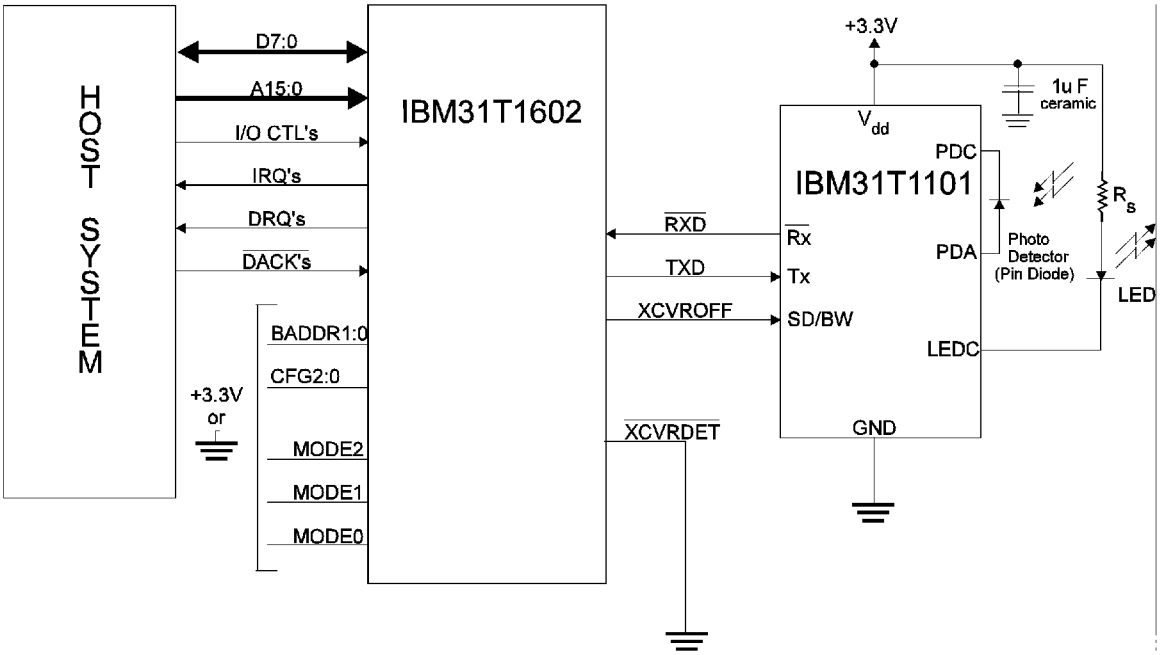


Figure 3-1. IBM31T1602 to IBM31T1101 Optical Transceiver Connections

3.4. Interface to the IBM31T1100 and TFDS6000 Transceivers

The IBM31T1101, IBM31T1100 and TFDS6000 transceivers have the same controller-transceiver electrical interface. The connection diagrams are shown in Figure 3-1 and Figure 3-2 on page 3-3. The electrical interface to these transceivers consists of three signals: transmit data, receive data and a bandwidth-select/power-down pin.

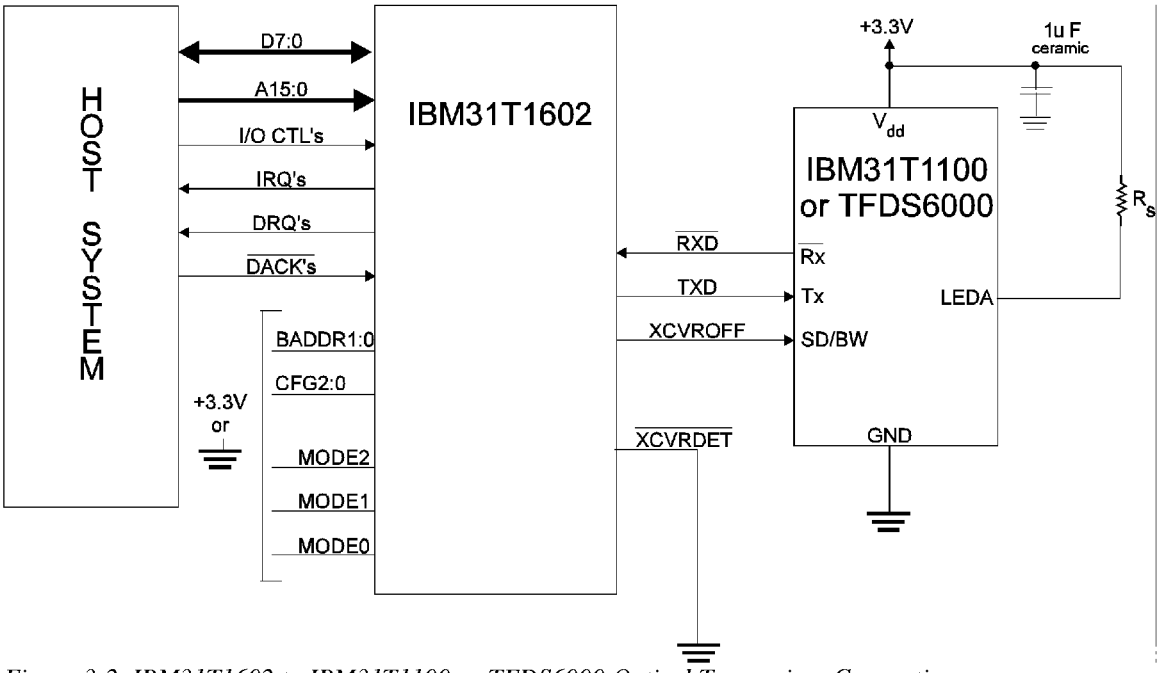


Figure 3-2. IBM31T1602 to IBM31T1100 or TFDS6000 Optical Transceiver Connections

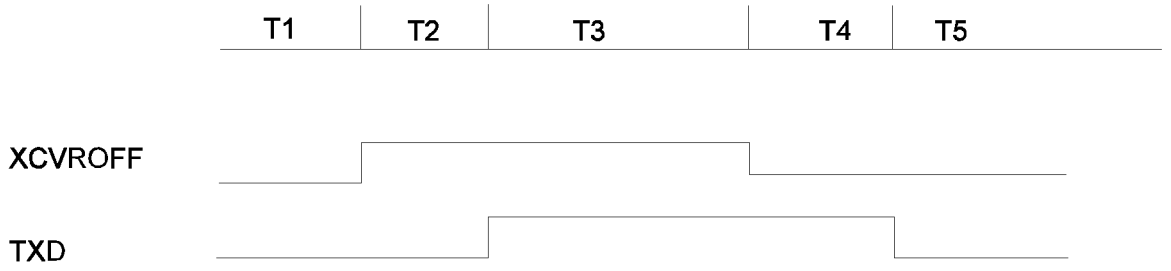
3.4.1. Bandwidth Switching with the IBM31T1101, IBM31T1100 and TFDS6000 Transceivers

Because of the optical pulse width differences between the various infrared data protocols (115.2 kbits/s and below, 1.152 Mbits/s, and 4 Mbits/s), the IBM31T1100, IBM31T1101, and TFDS6000 transceivers need to have their receiver amplifier gain ratio adjusted for proper reception. The transceivers cannot do this automatically; the controller must do the necessary switching. Two serial interface lines are used: the XCVROFF line which acts like a sampling clock (sampling at the falling edge), and the TXD line which provides the speed information (high for 4 Mbits/s IrDA, low for 1.152 Mbits/s and slower IrDA data rates).

In the IBM31T1602, the XCVROFF line is directly driven by the XCVROFF bit (b4) of the Infrared Transceiver Control Register. The TXD line can also be forced to high or low under the control of the TXD Force bit (b1) of the same register. Extreme care should be taken when setting the TXD Force bit to logic 1. *Leaving this bit at a logic 1 value for too long can burn out the LED's of some transceivers, since it directly forces the LED's on.*. The following illustrations show programming examples for the transceivers.

3.4.2. Switching from SIR Mode to FIR Mode

To change from HP-SIR (115.2 kbits/s or lower) mode or 1.152 Mbits/s mode to 4 Mbits/s mode, the TXD and the XCVROFF lines must be pulsed in this fashion:



T1 The transceiver is currently operating in 1.152 Mbits/s or lower IrDA mode.

T2 Set XCVROFF bit in the Infrared Transceiver Register to 1. This drives the XCVROFF line high. The Transceiver enters into a power-down state.

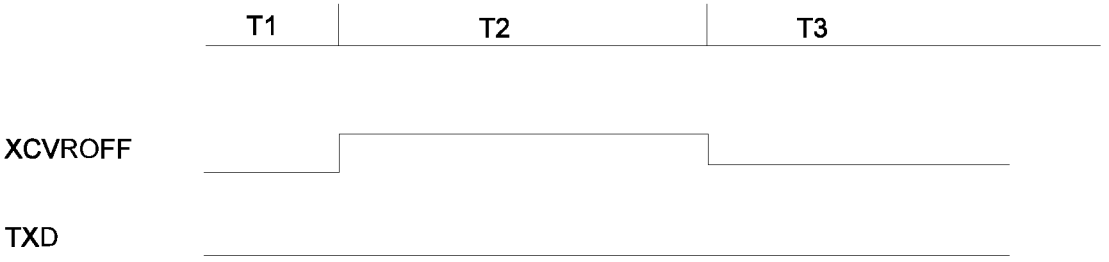
T3 Wait a minimum of 2 µs, then set the TXD Force bit to 1. This drives the TXD line high.[1]

T4 Wait a minimum of 2 µs, then set the XCVROFF bit to 0. The TXD line is sampled by the transceiver and now programmed for 4 Mbits/s IrDA mode.

T5 Wait a minimum of 2 µs, then set the TXD Force bit to 0. Now both the controller and the transceiver are ready for receive or transmit operations.

3.4.3. Switching from FIR Mode to SIR Mode

To change from 4 Mbits/s IrDA mode to 1.152 Mbits/s or lower IrDA mode:



T1 The transceiver is currently operating in 4 Mbits/s IrDA mode. Ensure that data is not being transmitted. It is important that no transmissions take place during this programming sequence since the state of the TXD line must be 0.

T2 Set the XCVROFF bit in the Infrared Transceiver Register to 1. The transceiver enters into a power-down state.

[1] The programmer must be careful when setting the TXD Force Bit to a value of 1. This bit should not be left at a 1 state for long periods, depending on the application. With transceivers where the TXD line directly affects the turning on and off of an LED, the TXD Force Bit = 1 state (which will force the state of the TXD line to be high) will force the LED on. LED's may burn out and be irreparably damaged if left turned on for an extended period.

T3 Wait a minimum of 2 µs, then set the XCVROFF bit to 0. Since the TXD Force bit should always be 0 there should be no need to alter this bit (it is 0 on power-up, and should never be set and left at a 1 value, lest transceiver damage occur). The TXD line is sampled by the transceiver on the high-to-low transition. The transceiver is now programmed for 1.152 Mbits/s or lower speeds IrDA mode. Both the controller and the transceiver are ready for receive or transmit operations.

3.5. Interface to the RY5DD01A (Sharp)

The RY5DD01A transceiver has a single transmit (Input) pin and single receive (Output) pin and does not have a power down or mode control line. The TXD output from the IBM31T1602 connects to the RY5DD01A's Input pin. The RY5DD01A Output is high when an infrared pulse is detected, opposite to the IBM31T1602's $\overline{\text{RXD}}$ pin. Adding an inverter to the RY5DD01A Output line solves this mismatch. The connection diagram is shown below.

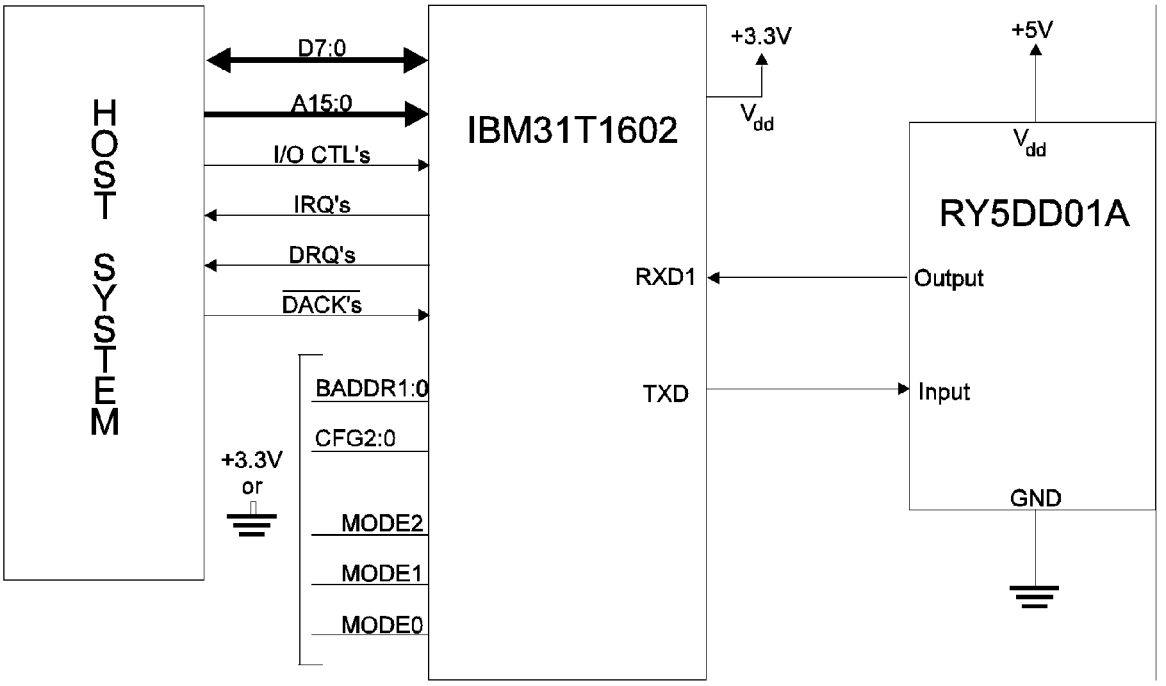


Figure 3-3. IBM31T1602 to RY5DD01A Optical Transceiver Connections

3.6. Interface to the HSDL-1100 (Hewlett-Packard)

The HSDL-1100 transceiver has one transmit data input pin and two receive data output pins, one for low-speed IrDA communication rates (up to 115.2 kbits/s), and one for FIR (1.152 Mbits/s and 4 Mbits/s) and Sharp ASK modulation. Since the IBM31T1602 controller has only one receive data input pin, an external multiplexer is required to combine the two
receive data inputs. Any of the IBM31T1602 General Purpose Output pins (GPO2, GPO1 or GPO0) can be used to control the multiplexer. Application software would set the control bit appropriately for either low-speed IrDA (select RX-A) or high-speed IrDA / Sharp operation (select RX-B).

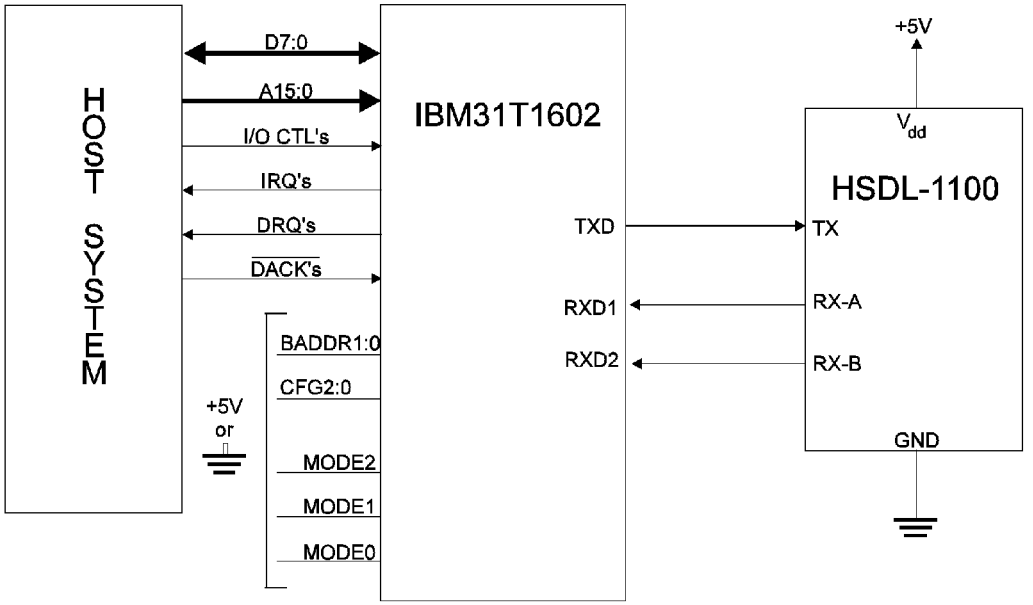


Figure 3-4. IBM31T1602 to HSDL-1100 Optical Transceiver Connections

3.6.1. Using the IBM31T1602 PDK with an HP Transceiver

To interface an HP HSDL-1100 transceiver to the IBM31T1602, assuming the presence of a standard 8-pin mini-DIN infrared dongle connector, make the connections as follows:

HP Transceiver		**8-Pin mini-DIN**		
VCC	----------	PIN 4	VCC	
GND	----------	PIN 3	GND	
TXD	----------<3----------	PIN 1	IRTX	<--->
RXD-A	---------3>----------	PIN 2	IRRX1	<---> IBM31T1602
RXD-B	---------3>----------	PIN 5	ID0_IRRX2	<--->
GND	-------75 Ohm resistor----------	PIN 6	ID1	
	NC	PIN 7	ID2	
	NC	PIN 8	ID3	

The 75 Ohm resistor and NC (no connects) are required to identify the transceiver type to the intelligent adapter logic on the board.

Performance will be improved if buffers are placed where indicated on the above diagram. The buffer from RXD-A is the most important. If buffers are not used, the HP transceiver must have good shielding to avoid picking up noise on the Rx lines.

During Hardware reset the $\overline{\text{PWRDWN}}$ pin must not be active. (It must be 1).

3.7. Sharp Carrier Detect

The Sharp Carrier Detect IRQ is only triggered when the Sharp carrier is on the IR media for 27 microseconds. This is sufficient for baud rates up to and including 38400 bps. For baud rates of 57600 and 115200 bps, at least two and three (respectively) consecutive zeros must be present for the detection of a Sharp carrier. The Sharp carrier detection logic is intended for the detection of Sharp IR data at 9600 bps while the HP demodulator is active. To detect a Sharp carrier when the FIR modulators (288 kbits/s to 4 Mbits/s) are active, power management must be disabled.

3.8. RTS Auto Reset Function

The RTS Auto Reset function (bit 3 register 3, bank 0) requires that the EOM condition is not reset until after the second closing flag is transmitted. Note that the IRQ is generated on the first closing flag. Therefore on very fast machines (Pentium processors, for instance), it is possible to have the IRQ routine reset the EOM prematurely for 576 kbits/s and 288 kbits/s transmission. For most other machines it is only possible for the IRQ routine to reset the EOM prematurely at 288 kbits/s.

The time from IRQ generation until when the EOM can be reset with RTS Auto Reset active can be calculated as follows (8/BitRate):

4 Mbits/s 8/4 Mpbs after 2 micro-seconds
1 Mbits/s 8/1.152 Mbits/s after 7 micro-seconds
576 kbits/s 8/576 kbits/s after 14 micro-seconds
288 kbits/s 8/288 kbits/s after 28 micro-seconds

If the software cannot ensure that a sufficient delay is present, the RTS Auto Reset function should not be used and the RTS should be reset by software in the IRQ handler.

3.9. Programmed I/O Receive for the FIR Subsystem

The following situation concerns the use of a combination of IRQ-driven and polled PIO transfers for fast IR (rather than DMA or Shared Memory). In this scenario, the Rx Data Available IRQ is enabled and the IRQ handler will loop based on the RxStatus (register 7, bank 0) and the Rx Interrupt bit (register 1, bank 0) bits.

After clearing the Rx_FIFO and thus resetting the Rx Data Available bit (bit 3, register 7, bank 0), the IRQ status register may be unstable prior to interrupt generation if another byte is received. To handle this instability, the programmer must do one of the following when using PIO for FIR transfers:
Do not loop on the Rx Interrupt in their IRQ routine.
Validate all IRQ status indications from the appropriate status register (ie.RxStatus or TxStatus register).

On discovery of an invalid status the user may choose to either ignore it (another IRQ will be generated), or reread the interrupt status and process it again.

4 Register Description

4.1. Plug and Play Mode

4.1.1. Configuration Register Access

Plug and Play (PnP) configuration has been implemented in the IBM31T1602 according to the Plug and Play ISA Specification Version 1.0a.

Configuration activity is achieved through three I/O ports
PnP Configuration Address Port, at I/O address 0279h, write-only
PnP Configuration Write Data Port, at I/O address 0A79h, write-only
PnP Configuration Read Data Port, at a variable address

Note that the Configuration Address Port and Configuration Write Data Port are located at fixed I/O addresses. The Configuration Read Data Port is assigned an address by configuration software, anywhere in the range 0203h to 03FFh as long as the address has 11b (binary) in the bits A1:0. Therefore, valid addresses are 0203h, 0207h, 020Bh, 020F, 0213h, 0217h, 021Bh, 021Fh, etc. The configuration program must ensure that the address does not conflict with a register on a non-PnP ISA device.

To access a PnP configuration register, the address of the target configuration register must first be written to the Configuration Address Port (at location 0279h). Note that a read from location 0279h actually reads the LPT1 printer status port. This is why the PnP Configuration Address Port, also at location 0279h, is a write-only register. Then, to write data into the target configuration register, write the data into the Configuration Write Data Port at location 0A79h. To read data from the target configuration register, read the Configuration Read Data Port.

4.1.2. Plug and Play Configuration

PnP configuration follows Version 1.0a of the Plug and Play ISA specification, dated May 5, 1994. A brief summary of the configuration process is described here. For details refer to the Plug and Play ISA specification.

After hardware reset, all plug and play devices are in a locked state called "WaitForKey". In this state the plug and play hardware ignores any access to the plug and play registers.
The Plug and Play BIOS issues a specific series of 8-bit writes to unlock all of the plug and play devices. The values of the writes form a key which take the Plug and Play devices from the "WaitForKey" state to the "Sleep" state. In the "Sleep" state the plug and play devices only respond to a write to the PnP "Wake", "Config Control" or "Set RD_DATA port" register.
When the BIOS writes to the "Wake" register one of two actions can occur:
All PnP devices that have not yet been isolated enter the "Isolation" state (Wake=CSN=0); or
One device that has already been isolated enters the "Config" state ((Wake=CSN)!=0).

After hardware reset, PnP devices are not isolated (CSN=0) so they can only enter the "Isolation" state upon reception of a write to the "Wake" register.
Once the "Isolation" state is entered, a series of paced reads from the "Serial Isolation Register", is used to isolate one plug and play device. At the end of the paced reads, only one PnP card will be left in the "Isolation" state, the rest would have dropped back to the "Sleep" state. What determines which PnP device is left at the end of a particular Isolation sequence is the contents of the device serial Ids for all PnP devices that have still not been isolated. The 64- bit serial ID for a PnP device is unique.

At this time the BIOS assigns a unique number from 1 to 255 (Card Select Number or CSN)[2] to one device. The act of assigning a CSN isolates a device, and puts it into the "Config" state. This device will no longer participate in future isolation sequences, unless its CSN is reset by the BIOS.
Once in the "Config" state, a device can be configured or returned to the "Sleep" state. The BIOS can always bring an individual device into the Config state by using the assigned CSN on a write to the "Wake" register.
Once configured, most of the configuration registers are predefined by the standard. A description of the registers the IBM31T1602 supports follows. The configuration registers are only accessible when a PnP device is in the "Config" state.
After all PnP devices are configured, the BIOS locks out access to the PnP device configuration registers by putting all of them into the "WaitForKey" state. It can access them again, if necessary, by using the key.

4.1.3. Set Read Data Port Address Register (Configuration Location=0x00)

Table 4- 1 Set Read Data Port Address Register (Configuration Location=0x00)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address bit A9	Address bit A8	Address bit A7	Address bit A6	Address bit A5	Address bit A4	Address bit A3	Address bit A2

Bit 7 Address bit A9

This bit sets address bit A9 of the read data port address. Note that address bits A11:10 are always 00b by default, while bits A15:12 are xxxx (don't care) in the read data port address decode.

Bit 6 Address bit A8

This bit sets address bit A8 of the read data port address.

Bit 5 Address bit A7

This bit sets address bit A7 of the read data port address.

Bit 4 Address bit A6

This bit sets address bit A6 of the read data port address.

Bit 3 Address bit A5

This bit sets address bit A5 of the read data port address.

Bit 2 Address bit A4

This bit sets address bit A4 of the read data port address.

Bit 1 Address bit A3

This bit sets address bit A3 of the read data port address.

Bit 0 Address bit A2

This bit sets address bit A2 of the read data port address. Note that address bits A1:0 are always 11b by default.

[2] Unique in the sense that the CSN assigned to the isolated PnP device will not be reassigned to another PnP device during this boot of the machine. The CSN is very much like a device handle.

4.1.4. Serial Isolation Register (Configuration Location=0x01)

Table 4- 2 Serial Isolation Register (Configuration Location=0x01)
Bits 7 – 0
Serial Identifier

Bits 7 – 0 Serial Identifier

The process of obtaining the identifier through this register uses many reads and is described in the Plug and Play specification.

4.1.5. Configuration Control Register (Configuration Location=0x02)

Table 4- 3 Configuration Control Register (Configuration Location=0x02)			
Bits 7 - 3	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	Reset CSN to Zero	Return to Wait For Key State	Reset Bit

Bits 7 – 3 Reserved

These bits are reserved and must be zero.

Bit 2 Reset CSN to Zero

When this bit is set to 1, the &chip.'s Card Select Number (CSN) is reset to zero.

Bit 1 Return to Wait for Key State

When this bit is set to 1, the &chip. returns to the wait for key state. The CSN and configuration registers are not affected. This bit is to be set after the &chip. has been configured and activated.

Bit 0 Reset Bit

When this bit is set to 1, all of the PnP configuration registers are reset to their default state. The CSN is not affected.

4.1.6. Wake Command Register (Configuration Location=0x03)

Table 4- 4 Wake Command Register (Configuration Location=0x03)
Bits 7 – 0
Wake Command Bits

Bits 7 – 0 Wake Command Bits

A CSN is written to these bits. There are a number of actions that can take place, depending on the PnP state of the IBM31T1602 and its CSN:
If the IBM31T1602 is in the sleep state and its CSN is 00h, writing a 00h to this register will cause the IBM31T1602 to move to the isolation state.

If the IBM31T1602 is in the sleep state and its CSN is non-zero, a write to this register with a matching CSN will cause the IBM31T1602 to move to the configure state. If the non-zero CSN does not match its assigned CSN, it will move to the sleep state.
If the IBM31T1602 is in the configure state (its CSN is non-zero), writing a 00h to this register will move the IBM31T1602 to the sleep state.

4.1.7. Resource Data Register (Configuration Location=0x04)

Table 4- 5 Resource Data Register (Configuration Location=0x04)

Bits 7 – 0
Resource Data Bits

Bits 7 – 0 Resource Data Bits

Read operations to this register allow individual bytes of the IBM31T1602's resource data to be read, one at a time. Each read fetches the next byte of the resource data. (The internal pointer in the resource data structure is auto-incremented.) The IBM31T1602's serial identifier and checksum must be read prior to accessing the resource data through this register. In addition, before each read from this register, the status register must be checked to determine if the next byte in the resource data is ready and available to be read through the Resource Data Register. This is required in case the resource data is stored in an external ROM device.

4.1.8. Status Register (Configuration Location=0x05)

Table 4- 6 Status Register (Configuration Location=0x05)

Bits 7 – 1	**Bit 0**
Reserved	Ready Bit

Bits 7 – 1 Reserved

Bit 0 Ready Bit

When this bit is 1, it indicates that the next byte of resource data is ready to be read from the Resource Data Register.

4.1.9. Card Select Number (CSN) Register (Configuration Location=0x06)

Table 4- 7 Card Select Number (CSN) Register (Configuration Location=0x06)

Bits 7 – 0
Card Select Number (CSN)

Bits 7 – 0 Card Select Number (CSN)

Writing a value from 01h to FFh to this register assigns and sets a valid CSN for the IBM31T1602. A CSN of 00h indicates that a CSN has not yet been assigned.

4.1.10. Logical Device Number (LDN) Register (Configuration Location=0x07)

Table 4- 8 Logical Device Number (LDN) Register (Configuration Location=0x07)

Bits 7 – 0
Logical Device Number (LDN)

Bits 7 – 0 Logical Device Number (LDN)

The IBM31T1602 only implements a single logical device and is therefore read-only and always returns the value 00h.

4.1.11. Activate Register (Configuration Location=0x30)

Table 4- 9 Activate Register (Configuration Location=0x30)

Bits 7 – 1	**Bit 0**
Reserved	Activate Bit

Bits 7 – 1 Reserved

These bits are reserved and always return zeroes when read.

Bit 0 Activate Bit

This bit activates the IBM31T1602 on the ISA bus when set to a 1 (1 = Activate, 0 = Deactivate) When this bit is 0 the IBM31T1602 will not respond to any ISA bus transactions other than PnP configuration register accesses. This bit is 0 after a reset or after a 1 is written to the Reset Bit in the Configuration Control Register.

4.1.12. I/O Range Check Register (Configuration Location=0x31)

Table 4- 10 I/O Range Check Register (Configuration Location=0x31)

Bits 7 - 2	**Bit 1**	**Bit 0**
Reserved	Enable Range Check	Pattern Select

Bits 7 – 2 Reserved

These bits are reserved and return zeroes when read.

Bit 1 Enable Range Check

This bit enables I/O range checking when set to 1.

Bit 0 Pattern Select

This bit selects the pattern (0 = AAh, 1 = 55h) to be returned upon reads to configured I/O addresses used by the IBM31T1602. Any reads to the I/O addresses that are configured will return the pattern (either AAh or 55h) if the Enable Range Check bit is set. Note that if the proper pattern is not returned, then most likely a non-PnP device is responding at the same I/O address(es) and the I/O range in the IBM31T1602 needs to be moved.

4.1.13. Power Management Register (Configuration Location=0x38)

Table 4- 11 Power Management Register (Configuration Location=0x38)

Bits 7 – 0
Power Management Bits

This register maps directly to the Power Down Register in ISA Indirect Configuration Register space. For a description of the bits in this register, please refer to "Power Down Register (PDR, Index=0x02)" for additional information.

4.1.14. Shared Memory Base Address Bits 23:16 Register (Configuration Location=0x40)

Table 4- 12 Shared Memory Base Address Bits 23:16 Register (Configuration Location=0x40)
Bits 7 – 0
Shared Memory Base Address Bits 23:16

Bits 7 – 0 Shared Memory Base Address Bits 23:16

If the IBM31T1602 is in Shared Memory mode, these bits are used to set bits 23:16 of the base address of the window into the physical shared memory utilized by the IBM31T1602. Note that bits 23:20 must be set to 0.

4.1.15. Shared Memory Base Address Bits 15:8 Register (Configuration Location=0x41)

Table 4- 13 Shared Memory Base Address Bits 15:8 Register (Configuration Location=0x41)
Bits 7 – 0
Shared Memory Base Address Bits 15:8

Bits 7 – 0 Shared Memory Base Address Bits 15:8

If the IBM31T1602 is in Shared Memory mode, these bits are used to set bits 15:8 of the base address of the window into the physical shared memory utilized by the IBM31T1602. Note that bits 12:8 are read-only and return zeroes.

4.1.16. Shared Memory Control Register (Configuration Location=0x42)

Table 4- 14 Shared Memory Control Register (Configuration Location=0x42)		
Bits 7 – 2	**Bit 1**	**Bit 0**
Reserved	8- or 16-Bit Memory	Range/Limit Usage

Bits 7 – 2 Reserved

These read-only bits are reserved and always read zeroes.

Bit 1 8- or 16-Bit Memory

This bit is read-only and always returns 0, since the IBM31T1602 does not permit selectable 8- or 16-bit memory operation. Memory operation is always 8-bit.

Bit 0 Range/Limit Usage

This bit is read-only and always returns 0, indicating that the Shared Memory Range/Limit Registers are used to indicate the range length (size) of the window into shared memory, and that the base address of the shared memory window must be an address divisible by the shared memory window size.

4.1.17. Shared Memory Range/Limit Bits 23:16 Register (Configuration Location=0x43)

Table 4- 15 Shared Memory Range/Limit Bits 23:16 Register (Configuration Location=0x43)
Bits 7 – 0
Range Bits 23:16

Bits 7 – 0 Range Bits 23:16

Defines the upper bits of the range length. Applies only to Shared Memory mode and is read-only, returning FFh.

4.1.18. Shared Memory Range/Limit Bits 15:8 Register (Configuration Location=0x44)

Table 4- 16 Shared Memory Range/Limit Bits 15:8 Register (Configuration Location=0x44)
Bits 7 – 0
Range Bits 15:8

Bits 7 – 0 Range Bits 15:8

Defines the lower bits of the range length. Applies only to Shared Memory mode and is read-only, returning E0h, which indicates a memory window size of 8 Kbytes.

4.1.19. UART Base Address Upper Byte Register (Configuration Location=0x60

Table 4- 17 UART Base Address Upper Byte Register (Configuration Location=0x60)
Bits 7 – 0
UART Base Address Upper Byte

Bits 7 – 0 UART Base Address Upper Byte

This register is used to assign the upper byte of the I/O base address of the IBM31T1602's internal UART.

4.1.20. UART Base Address Lower Byte Register (Configuration Location=0x61)

Table 4- 18 UART Base Address Lower Byte Register (Configuration Location=0x61)
Bits 7 – 0
UART Base Address Lower Byte

Bits 7 – 0 UART Base Address Lower Byte

This register is used to assign the lower byte of the I/O base address of the IBM31T1602's internal UART. Bits 2:0 are read-only and always return zeroes.

4.1.21. FIR Subsystem Base Address Upper Byte Register (Configuration Location=0x62)

Table 4- 19 FIR Subsystem Base Address Upper Byte Register (Configuration Location=0x62)
Bits 7 – 0
FIR Subsystem Base Address Upper Byte

Bits 7 – 0 FIR Subsystem Base Address Upper Byte
This register is used to assign the upper byte of the I/O base address of the IBM31T1602's internal FIR subsystem.

4.1.22. FIR Subsystem Base Address Lower Byte Register (Configuration Location=0x63)

Table 4- 20 FIR Subsystem Base Address Lower Byte Register (Configuration Location=0x63)
Bits 7 – 0
FIR Subsystem Base Address Lower Byte

Bits 7 – 0 FIR Subsystem Base Address Lower Byte

This register is used to assign the lower byte of the I/O base address of the IBM31T1602's internal FIR subsystem. Bits 2:0 are read-only and always return zeroes.

4.1.23. UART IRQ Select Configuration Register (Configuration Location=0x70)

Table 4- 21 UART IRQ Select Configuration Register (Configuration Location=0x70)	
Bits 7 – 4	**Bits 3 - 0**
Reserved	UART IRQ Select

Bits 7 – 4 Reserved

These bits are reserved.

Bits 3 – 0 UART IRQ Select

These bits select which ISA system IRQ line the IBM31T1602's UART interrupt request line is routed to. The supported values are:
0h (a system IRQ line has not been assigned)
3h (ISA IRQ3 line selected)
4h (ISA IRQ4 line selected)
5h (ISA IRQ5 line selected)
Ah (ISA IRQ10 line selected)
Bh (ISA IRQ11 line selected)
Ch (ISA IRQ12 line selected)
Fh (ISA IRQ15 line selected)

4.1.24. UART IRQ Type Configuration Register (Configuration Location=0x71)

Table 4- 22 UART IRQ Type Configuration Register (Configuration Location=0x71)	
Bits 7 – 2	**Bits 1 - 0**
Reserved	UART IRQ Type

Bits 7 – 2 Reserved

These bits are reserved.

Bits 1 – 0 UART IRQ Type

These bits define the type of interrupt generated from the UART. The supported types are:

Bit 1	Bit 2	Interrupt Type
0	1	Active low, level sensitive
1	0	Low-to-high transition

4.1.25. FIR Subsystem IRQ Select Configuration Register (Configuration Location=0x72)

Table 4- 23 FIR Subsystem IRQ Select Configuration Register (Configuration Location=0x72)	
Bits 7 – 4	**Bits 3 - 0**
Reserved	FIR Subsystem IRQ Select

Bits 7 – 4 Reserved

These bits are reserved.

Bits 3 – 0 FIR Subsystem IRQ Select

These bits select which ISA system IRQ line the IBM31T1602's FIR subsystem interrupt request line is routed to. The supported values are:
0h (a system IRQ line has not been assigned)
3h (ISA IRQ3 line selected)
4h (ISA IRQ4 line selected)
5h (ISA IRQ5 line selected)
Ah (ISA IRQ10 line selected)
Bh (ISA IRQ11 line selected)
Ch (ISA IRQ12 line selected)
Fh (ISA IRQ15 line selected)

4.1.26. FIR Subsystem IRQ Type Configuration Register (Configuration Location=0x73)

Table 4- 24 FIR Subsystem IRQ Type Configuration Register (Configuration Location=0x73)	
Bits 7 – 2	**Bits 1 - 0**
Reserved	FIR Subsystem IRQ Type

Bits 7 – 2 Reserved

These bits are reserved.

Bits 1 – 0 FIR Subsystem IRQ Type

These bits define the type of interrupt generated from the FIR subsystem. The supported types are:

Bit 1	**Bit 2**	**Interrupt Type**
0	1	Active low, level sensitive
1	0	Low-to-high transition

4.1.27. First DMA Channel Configuration Register (Configuration Location=0x74)

Table 4- 25 First DMA Channel Configuration Register (Configuration Location=0x74)	
Bits 7 – 3	**Bits 2 - 0**
Reserved	1st DMA Channel Select

Bits 7 – 3 Reserved

These bits are reserved.

Bits 2 – 0 1st DMA Channel Select

In Host DMA mode these bits select which ISA DMA channel the first IBM31T1602 internal DMA channel is routed to. The supported values are:

0h, DMA channel 0 (DRQ0, -DACK0)
1h, DMA channel 1 (DRQ1, -DACK1)
2h, DMA channel 2 (DRQ2, -DACK2)
3h, DMA channel 3 (DRQ3, -DACK3)
4h, no DMA channel selected

In Shared Memory mode this register is read-only and returns the value 04h.

4.1.28. Second DMA Channel Configuration Register (Configuration Location=0x75)

Table 4- 26 Second DMA Channel Configuration Register (Configuration Location=0x75)

Bits 7 – 3	Bits 2 - 0
Reserved	2nd DMA Channel Select

Bits 7 – 3 Reserved

These bits are reserved.

Bits 2 – 0 2nd DMA Channel Select

In Host DMA mode these bits select which ISA DMA channel the second IBM31T1602 internal DMA channel is routed to. The supported values are:
0h, DMA channel 0 (DRQ0, -DACK0)
1h, DMA channel 1 (DRQ1, -DACK1)
2h, DMA channel 2 (DRQ2, -DACK2)
3h, DMA channel 3 (DRQ3, -DACK3)
4h, no DMA channel selected

In Shared Memory mode this register is read-only and returns the value 04h.

4.2. Indirect Configuration Registers

4.2.1. Power Down Register (PDR, Index=0x02)

Table 4- 27 Power Down Register (PDR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Software Reset	Lock Configuration	En Test Mode	En UART APM	Reserved	En Infrared Wakeup	En Power Down	Power Down

Bit 7 Software Reset

Setting this bit to 1 activates an internal signal which resets the infrared controller. Setting this bit to 0 deactivates the internal reset signal.

Note: Software Reset must be held in the 1 state (active state) for at least 500 ms. Both the UART and FIR subsystem registers are inaccessible during software reset. Software reset does not affect configuration registers; however, the UART and FIR control registers are reset.

Bit 6 Lock Configuration

Setting this bit to 1 prevents all write accesses to configuration registers.

Note: After setting Lock Configuration, only a hardware reset can then clear it.

Bit 5 En Test Mode

This bit is used for manufacturing test only. It is cleared upon reset. Setting this bit will corrupt the proper function of the GPO2, GPO1 and GPO0 pins, because internal signals are multiplexed on these pins.

Bit 4 En UART APM

Setting this bit enables Automatic Power Management (APM) in the UART subsystem. This bit is cleared upon reset. When En Power Down is set to 1, the IBM31T1602 performs the power managing functions by disabling clocks to the subsystems that are not enabled. The UART subsystem has an additional feature in that it can power down its circuit automatically when it is not being accessed, even when the main UART clock is running.

Bit 2 En Infrared Wakeup

Setting this bit to 1 enables wakeup interrupts on the FIR subsystem interrupt request line to occur whenever infrared traffic is detected while the IBM31T1602 is powered down.

Note: After receiving an infrared wakeup interrupt, it is the software's responsibility to take the IBM31T1602 out of power-down in order to receive any incoming infrared data.

Bit 1 En Power Down

Setting this bit to 1 enables the IBM31T1602 to be powered down using the power down bit (b0), or via the $\overline{\text{PWRDWN}}$ pin. It also activates the Power Conservation mode, in which subsystems automatically shut down when they are not being used. For example, when FIR and UART are not enabled, all clocks to the FIR and UART subsystems are disabled, providing the maximum power savings. If FIR is enabled and UART is not, then only the FIR subsystem is running and the UART is still in power-down mode, and vice-versa.

Note: This bit is set to 1 by default. It may be cleared after reset if Power Conservation mode is not desired.

Bit 0 Power Down

Setting this bit to 1 causes all subsystems to be powered down, provided that En Power Down (b1) has already been set to 1. Alternatively, the IBM31T1602 can be powered down by driving the $\overline{\text{PWRDWN}}$ pin low.

4.2.2. Identification Register (IDR, Index=0x08)

Table 4- 28 Identification Register (IDR)

Bits 7 – 0	
IBM31T1602 ID:	
11100010	Host DMA Mode (0xE2)
11100011	Shared Memory Mode (0xE3)

Bits 7 – 0 Identification

In Host DMA mode, this read-only register returns 0xE2 on reads. In Shared Memory mode, it returns 0xE3 on reads.

4.2.3. DMA Line Select Register (DLS, Index=0xA2)

Table 4- 29 DMA Line Select Register (DLS) Host DMA Mode			
Bit 7	**Bits 6 - 4**	**Bit 3**	**Bits 2 - 0**
Reserved	Infrared DRQ 2 Line Select	Reserved	Infrared DRQ 1 Line Select

Bits 6 – 4 **i**DRQ2 Line Select

Selects the external DMA request/acknowledge (DRQn/$\overline{\text{DACKn}}$) output pins to map into the FIR subsystem's internal DMA request (IDRQ2) line.

Bits 2 – 0 iDRQ1 Line Select

Selects the external DMA request/acknowledge (DRQn/$\overline{\text{DACKn}}$) output pins to map into the FIR subsystem's internal DMA request (iDRQ1) line.

4.2.4. Shared Memory Base Address Register (SMBA, Index=0xA2)

Table 4- 30 Shared Memory Base Address Register							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A19	A18	A17	A16	A15	A14	A13	Reserved

Bits 7 – 1 Shared Memory Base Address, A19 - A13

Specifies the base address of the 8 Kbyte system memory window mapped to local memory in the system address space. The memory window is enabled when the IBM31T1602 is in Shared Memory mode and the En Host Mem Window bit (b5 of the Infrared Control Register) is set to 1.

4.2.5. Infrared Control Register (IRC, Index=0xA3)

Table 4- 31 Infrared Control Register (IRC)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Reserved	Reserved	En Host Memory Window	En Level Mode	Advanced Interrupt Configuration	Shared Interrupt Select	Reserved	En Infrared

Bit 5 En Host Memory Window

Setting this bit to 1 enables the 8 Kbyte system memory window specified in the Shared Memory Base Address Register. This bit is only valid in Shared Memory mode.

Bit 4 En Level Mode

Selects the type of interrupt generated when Advanced Interrupt Configuration is enabled (b3=1). Setting this bit to 1 puts the interrupt request output pins in level mode. A level mode interrupt generates an active-low signal that remains in the active state until the interrupt condition is cleared. Setting this bit to 0 puts the interrup request output pins in pulse mode. A pulse mode interrupt generates an active-low pulse ranging from 0.5 ms to 1 ms in duration.

Bit 3 Advanced Interrupt Configuration

Setting this bit to 1 enables Advanced Interrupt Configuration. The Shared Interrupt Select bit (b2) is ignored, and each subsystem's internal interrupt request line can be independently routed to one of four interrupt request output pins in either pulse or level mode: IRQ3, IRQ4, UIRQ, or FIRQ. If both the UART and FIR subsystems drive the same interrupt request line, they form a shared interrupt. The Advanced Interrupt Select bits (b1-b0 of UART Address Low Register and FIR Address Low Register) determine which interrupt request output pin receives the UART and FIR subsystem interrupts respectively.

Setting this bit to 0 puts the interrupt request output pins in pulse mode:
UIRQ becomes the UART subsystem interrupt request line
FIRQ becomes the FIR subsystem interrupt request line
IRQ3 or IRQ4 carry the shared interrupt request line (specified by the Shared Interrupt Select bit)

Bit 2 Shared Interrupt Select

When Advanced Interrupt Configuration is disabled (b3=0), this bit selects the IRQn line that will carry the shared interrupt request. 0 = IRQ3 and 1 = IRQ4.

Bit 0 En Infrared

Setting this bit to 1 enables the Infrared Core module. Setting this bit to 0 disables the Infrared Core module. The infrared core module automatically powers down. The XCVROFF output pin is asserted to power down the external infrared transceiver. Power-down occurs regardless of the setting of En Power Dow n (b1) in the Power Down Register

4.2.6. UART High Address Register (UARTH, Index=0xA4)

Table 4- 32 UART High Address Register (UARTH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 – 0 UART Base Address, A15 - A8

Specifies the high-order base address of the UART subsystem.

4.2.7. UART Low Address Register (UARTL, Index=0xA5)

Table 4- 33 UART Low Address Register (UARTL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2 - 0
A7	A6	A5	A4	A3	Advanced Interrupt Selection

Bits 7 – 3 UART Base Address, A7 - A3

Specifies the low-order base address of the UART subsystem.

Bits 2 – 0 Advanced Interrupt Selection

Selects the interrupt request output pin that will carry the UART subsystem interrupts when Advanced Interrupt Configuration is enabled (b3 of IRC is set to 1).

4.2.8. FIR High Address Register (FIRH, Index=0xA6)

Table 4- 34 FIR High Address Register (FIRH)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 – 0 FIR Base Address, A15 - A8

Specifies the high-order base address of the FIR subsystem.

4.2.9. FIR Low Address Register (FIRL, Index=0xA7)

Table 4- 35 FIR Low Address Register (FIRL)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bits 2 - 0
A7	A6	A5	A4	A3	Advanced FIR Interrupt Selection

Bits 7 – 4 FIR Base Address, A7 - A3

Specifies the low-order base address of the FIR subsystem.

Bits 2 – 0 Advanced FIR Interrupt Configuration

Selects the interrupt request output pin that will carry the FIR subsystem interrupts when Advanced Interrupt Configuration is enabled (b3 of IRC is set to 1).

4.3. Direct Configuration Registers

4.3.1. Identification 0 Register (ID0, Index=0x0)

Table 4- 36 Identification Register 0 (ID0)

Bits 7 – 0
IBM31T1602 ID0: **11100010** Host DMA Mode (0xE2) **11100011** Shared Memory Mode (0xE3)

Bits 7 – 0 Identification 0

Returns 0xE2 on reads in Host DMA mode. Returns 0xE3 on reads in Shared Memory mode.

4.3.2. Identification Register 1 (ID1, Index=0x1)

Table 4- 37 Identification Register 1 (ID1)

Bits 7 – 0	
IBM31T1602 ID1	11011111 (0xDF)

Bits 7 – 0 Identification 1

Returns 0xDF on reads.

4.3.3. Setup Register (SET, Index=0x2)

Table 4- 38 Setup Register (SET)

Bit 7	Bit 6	Bit 5	Bit 4	Bits 3 - 2	Bit 1	Bit 0
En Level Mode	Software Reset	En Infrared Wakeup	En Advanced Interrupt Selection	Advanced Interrupt Selection	En Host Memory Window	En Infrared

Bit 7 En Level Mode

This bit works in conjunction with En Advanced Interrupt (b4). When this bit is 1, it enables level mode interrupt, which is active low. Clearing this bit enables pulse mode interrupt.

Bit 6 Software Reset

Setting this bit to 1 activates an internal signal which resets the infrared controller. Setting this bit to 0 deactivates the internal reset signal.

Note: Software Reset must be held in the 1 state (active state) for at least 500 ms. Both the UART and FIR subsystem registers are inaccessible during software reset. Software reset does not affect configuration registers; however, the UART and FIR control registers are reset.

Bit 5 En Infrared Wakeup

Setting this bit to 1 enables wakeup interrupts on the FIR subsystem interrupt request line to occur whenever infrared traffic is detected while the IBM31T1602 is powered down.

Note: After receiving an infrared wakeup interrupt, it is the software's responsibility to take the IBM31T1602 out of power-down in order to receive any incoming infrared data.

Bit 4 En Advanced Interrupt

When this bit is set to 1 it enables advanced interrupt selection for direct configuration. The FIR and The UART interrupts are merged and can be routed as specified by b3 and b2. When this bit is '0', the FIR interrupt is fixed to the FIRQ pin and the UART interrupt is fixed to the UIRQ pin. Both interrupts become active high. That is, FIRQ is high when FIR interrupt is pending, and low when FIR interrupt is reset.

Bits 3 – 2 Advanced Interrupt Select

When En Advanced Interrupt (b4) is set to 1, the shared interrupt will be routed to one of the four interrupt pins.

Bit 1 En Host Memory Window

Setting this bit to 1 enables the 8 Kbyte system memory window specified in the Shared Memory Base Address Register. This bit is only valid in Shared Memory mode.

Bit 0 En Infrared

Setting this bit to 1 enables the Infrared Core module. Setting this bit to 0 disables the Infrared Core module. The Infrared Core module automatically powers down. The XCVROFF output pin is asserted to power down the external infrared transceiver.

4.3.4. UART Low Index Register (UARTL, Index=0x3)

Table 4- 39 UART Low Address Register (UARTL)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bits 7 – 3 UART Base Address, A7 - A3

Specifies the low-order base address of the UART subsystem.

4.3.5. UART High Address Register (UARTH, Index=0x4)

Table 4- 40 UART High Address Register (UARTH)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 – 0 UART Base Address, A15 - A8

Specifies the high-order base address of the UART subsystem.

4.3.6. FIR Low Address Register (FIRL, Index=0x5)

Table 4- 41 FIR Low Address Register (FIRL)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A7	A6	A5	A4	A3	Reserved	Reserved	Reserved

Bits 7 – 3 FIR Base Address, A7 - A3

Specifies the low-order base address of the FIR subsystem.

4.3.7. FIR High Address Register (FIRH, Index=0x6)

Table 4- 42 FIR High Address Register (FIRH)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
A15	A14	A13	A12	A11	A10	A9	A8

Bits 7 – 0 FIR Base Address, A15 - A8

Specifies the high-order base address of the FIR subsystem.

4.3.8. Local DMA Control Register (LDMAC, Index=0x7)

Table 4- 43 Local DMA Control Register (LDMAC)		
Bits 7 – 4	Bits 3 - 2	Bits 1 - 0
Reserved	iDRQ2 Line Select	iDRQ1 Line Select

Bits 3 – 2 DRQ2 Line Select
Selects the external DRQn/DACKn output pins to map into the FIR subsystem's internal iDRQ2 line.

Bits 1 – 0 iDRQ1 Line Select
Selects the external DRQn/DACKn output pins to map into the FIR subsystem's internal iDRQ1 line.

4.3.9. Shared Memory Base Address Register (SMBA, Index=0x7)

Table 4- 44 Shared Memory Base Address Register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
A19	A18	A17	A16	A15	A14	A13	Reserved

Bits 7 – 1 Shared Memory Base Address, A19 - A13

Specifies the base address of the 8 Kbyte system memory window mapped to local memory in the system address space. The memory window is enabled when the IBM31T1602 is in Shared Memory mode and the En Host Mem Window bit (b1 of the Setup Register) is set to 1.

4.4. UART Control Registers

4.4.1. Receive Buffer Register (RBR, Index=0x0, DLAB=0)

Table 4- 45 Receive Buffer Register (RBR)

Bits 7 – 0
Data Bits 7 - 0

Bits 7 – 0 Receive Data, D7 - D0

Holds deserialized data from the Receive Shift Register (RSR).

4.4.2. Transmit Holding Register (THR, Index=0x0, DLAB=0)

Table 4- 46 Transmit Holding Register (THR)

Bits 7 – 0
Data Bits 7 - 0

Bits 7 – 0 Transmit Data, D7 - D0

Holds transmit data. The Transmit Shift Register (TSR) serializes the data and shifts it out through the selected modulator.

4.4.3. Interrupt Enable Register (IER, Index=0x1)

Table 4- 47 Interrupt Enable Register (IER)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	En Modem Status Interrupt	En Receiver Line Status Interrupt	En Transmitter Holding Register Empty Interrupt	En Received Data Available Interrupt

Bit 3 En Modem Status

Setting this bit to 1 enables the Modem Status interrupt.

Bit 2 En Rx Line Status

Setting this bit to 1 enables the Receiver Line Status interrupt.

Bit 1 En THR Empty

Setting this bit to 1 enables the Transmit Holding Register Empty interrupt.

Bit 0 En Rx Data Available

Setting this bit to 1 enables the Received Data Available interrupt. In FIFO mode, this bit enables the Timeout interrupt.

4.4.4. Interrupt Identification Register (IIR, Index=0x2)

Table 4- 48 Interrupt Identification Register (IIR)

Bits 7 – 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FIFOs Enabled	0	0	Interrupt ID Bit 2	Interrupt ID Bit 1	Interrupt ID Bit 0	Interrupt Pending

Bits 7 – 6 FIFOs Enabled

These bits are set to 11 when the FIFO Enable bit (b0 of FCR) is set to 1.

Bits 3 – 1 Interrupt Identification, ID2 - ID0

Indicates the highest priority interrupt pending. In 16450 mode, ID2 is always 0. See D.2, "UART Interupt Priority Settings Of the Interupt Identification Register" on page D-2.

Bit 0 Interrupt Pending

When set to 0, indicates an interrupt is pending.

4.4.5. FIFO Control Register (FCR, Index=0x2)

Table 4- 49 FIFO Control Register (FCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Rx Trigger Level (MSB)	Rx Trigger Level (LSB)	Reserved	Reserved	Reserved	TxFIFO Reset	RxFIFO Reset	FIFO Enable

Bits 7 – 6 Rx Trigger Level

Specifies the trigger level for the RxFIFO interrupt. When the number of bytes in RxFIFO equal the selected trigger level, a Received Data Available interrupt is set.

Bit 2 TxFIFO Reset

Setting this bit to 1 clears all bytes in the transmit FIFO. However, the Transmit Shift Register (TSR) is not affected. This bit is self-clearing.

Bit 1 RxFIFO Reset

Setting this bit to 1 clears all bytes in the receiver FIFO. However, the Receive Shift Register (RSR) is not affected. This bit is self-clearing.

Bit 0 FIFO Enable

Setting this bit to 1 puts the UART in FIFO mode. Both the transmit and receive FIFOs are enabled. Resetting this bit will clear all bytes in both FIFOs. Also, when changing from FIFO mode to 16450 mode and vice versa, data is automatically cleared from the FIFOs. :note.This bit must be set to 1 before any of the remaining bits of the FCR can be programmed.

4.4.6. Line Control Register (LCR, Index=0x3)

Table 4- 50 Line Control Register (LCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Divisor Latch Access Bit	Set Break	Stick Parity	Parity Select	Parity Enable	Number of Stop Bits	Character Length Select Bit 1	Character Length Select Bit 0

Bit 7 Divisor Latch Access Bit

This bit is used to access the DLL and DLM registers. Table 1-6 on page 1-12 shows all UART Control Registers' address assignment in conjunction with the DLAB. This bit is initialized to 0 after reset. When DLAB is 1, the DLL can be accessed through offset address 0x and the DLM can be accessed through offset address 1x. When DLAB is 0, the RBR/THR can be accessed through offset address 0x and the IER can be accessed through offset address 1x.

Bit 6 Set Break

Setting this bit to 1 causes a break (transmission of all zeros) to be transmitted.

Bit 5 Stick Parity

When even parity is enabled (b3=1 and b4=1), setting this bit to 1 causes the parity bit to be transmitted and checked as a 0. When odd parity is enabled (b3=1 and b4=0), setting this bit to 1 causes the parity bit to be transmitted and checked as a 1. Setting this bit to 0 disables stick parity.

Bit 4 Parity Select

Specifies odd or even parity.

Bit 3 Parity Enable

Setting this bit to 1 enables parity generation and checking during transmission and reception.

Bit 2 Number of Stop Bits

Specifies the number of stop bits transmitted with each serial character. If this bit is set to 1 and the character length is set to 6, 7, or 8 bits, the UART generates two stop bits. If this bit is set to 0, one stop bit is generated regardless of the Character Length setting.

Note: The receiver only checks the first stop bit even if the UART is programmed to receive two stop bits.

Bits 1 – 0 Character Length

Specifies the number of bits in each transmitted or received serial character.

4.4.7. Modem Control Register (MCR, Index=0x4)

Table 4- 51 Modem Control Register (MCR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Loop	IRQ Enable	Output 1	Request to Send	Data Terminal Ready

Bit 4 Loop

Setting this bit to 1 puts the UART into Loopback mode for diagnostic testing of the transmit and receive data paths within the UART.

Bit 3 IRQ Enable

Setting this bit to 1 enables all UART interrupts.

Bit 2 Output 1

Controls the user-designated OUT1 output signal. Setting this bit to 1 forces the Output 1 output signal low (active). Setting this bit to 0 forces OUT1 high (inactive).

Bit 1 Request to Send

Controls the Request to Send (RTS) output signal. Setting this bit to 1 forces the RTS output signal low (active). Setting this bit to 0 forces RTS high (inactive).

Bit 0 Data Terminal Ready

Controls the Data Terminal Ready (DTR) output signal. Setting this bit to 1 forces the DTR output signal low (active). Setting this bit to 0 forces DTR high (inactive).

Note: Although b0, b1, and b2 can be written to and read from, their signals are not connected to any physical pins of the IBM31T1602. They are merely present for maintaining compatibility with existing UART-based software, and do not affect the operation of the controller.

4.4.8. Line Status Register (LSR, Index=0x5)

Table 4- 52 Line Status Register (LSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RxFIFO Error	Transmitter Empty	Transmitter Holding Register Empty	Break Interrupt	Framing Error	Parity Error	Overrun Error	Data Ready

Bit 7 RxFIFO Error

When set to 1, indicates there is at least one parity error, frame error, or break interrupt condition in RxFIFO. This bit is cleared by reading LSR (only if there are no subsequent errors in the FIFO).

Note: In 16450 mode, this bit is always 0.

Bit 6 Transmitter Empty

When set to 1, indicates THR and TSR are both empty. This bit is cleared when THR or TSR contain data. In FIFO mode, this bit is set to 1 when TxFIFO and TSR are both empty.

Bit 5 Transmit Holding Register Empty

When set to 1, indicates the UART is ready to accept a new character for transmission. This occurs when a character is transferred from THR to TSR. If the En Transmitter Holding Register (THR) Empty bit (b1 of IER) is enabled, an interrupt is issued to the host processor. The THRE bit is cleared when data is written to THR. In FIFO mode, this bit is set to 1 when TxFIFO becomes empty, and set to 0 when TxFIFO is written to.

Bit 4 Break Interrupt

When set to 1, indicates a break character was received (i.e. receive data input to the UART was held in logic 0 state for longer than one full-word transmission time). This bit is cleared by reading LSR. When a break occurs in FIFO mode, only one zero character is loaded into the FIFO. The next character transfer is enabled after the receive data input line goes to the logic 1 state (idle) and receives the next valid start bit.

Note: The break interrupt condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 3 Framing Error

When set to 1, indicates the received character had an invalid stop bit (i.e. stop bit was detected as a logic 0). This bit is cleared by reading LSR. In FIFO mode, a framing error is associated with the particular character in the FIFO. The framing error is reported to the host processor when the associated character is at the top of the FIFO.
Note: The framing error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 2 Parity Error

When set to 1, indicates the received character did not have the correct even or odd parity, as specified by the Parity Select bit (b4 of LCR). This bit is cleared by reading LSR. In FIFO mode, parity error is associated with the particular character in the FIFO. The parity error is reported to the host processor when the associated character is at the top of the FIFO.
Note: The parity error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 1 Overrun Error

When set to 1, indicates the host processor was not fast enough in reading the data from RBR before it was overwritten by the next incoming data character. This bit is cleared by reading LSR.

In FIFO mode, if data continues to fill the FIFO beyond the trigger level, an overrun error will occur at the point where the FIFO is full and the next character has completely been received by the shift register (RSR). As data continues to be received, only RSR is overwritten, and no data is transferred to the FIFO.

Note: The overrun error condition generates a Receiver Line Status interrupt when the En Rx Line Status bit (b2 of IER) is enabled.

Bit 0 Data Ready

When set to 1, indicates a complete incoming character was received and transferred to RBR or RxFIFO. This bit is cleared by reading RBR or the FIFO.

Note: LSR is intended for read-only operations. Writing to this register is recommended only for manufacturing test purposes. In FIFO mode, the programmer must load a data byte in RxFIFO in Loopback mode when intending to write to b4-b3. Also, b0 and b7 cannot be written to in FIFO mode.

4.4.9. Modem Status Register (MSR, Index=0x6)

Table 4- 53 Modem Status Register (MSR)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data Carrier Detect	Ring Indicator	Data Set Ready	Clear to Send	Delta Data Carrier Detect	Trailing Edge Ring Indicator	Delta Data Set Ready	Delta Clear to Send

Bit 7 Data Carrier Detect

This bit is the complement of the Data Carrier Detect input. In Loopback mode, this bit is equivalent to the IRQ Enable bit in MCR.

Bit 6 Ring Indicator

This bit is the complement of the Ring Indicator input. In Loopback mode, this bit is equivalent to the Output 1 bit in MCR.

Bit 5 Data Set Ready

This bit is the complement of the Data Set Ready input. In Loopback mode, this bit is equivalent to the Data Terminal Ready bit in MCR.

Bit 4 Clear To Send

This bit is the complement of the Clear to Send input. In Loopback mode, this bit is equivalent to the Request to Send bit in MCR.

Bit 3 Delta Data Carrier Detect

When set to 1, indicates Delta Clear to Send input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by Delta Data Carrier Detect when the En Modem Status bit (b3 of IER) is enabled.

Bit 2 Trailing Edge Ring Indicator

When set to 1, indicates Ring Indicator input to the UART has changed from a low to high state. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by TERI when the En Modem Status bit (b3 of IER) is enabled.

Bit 1 Delta Data Set Ready

When set to 1, indicates Data Set Ready input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.

Note: A Modem Status interrupt is generated by DDSR when the En Modem Status bit (b3 of IER) is enabled.

Bit 0 Delta Clear To Send

When set to 1, indicates Clear to Send input to the UART has changed state since the last time it was read by the CPU. This bit is cleared by reading MSR.
Note: A Modem Status interrupt is generated by DCTS when the En Modem Status bit (b3 of IER) is enabled.

Note: The CTS, DSR, and DCD inputs to the UART are tied high internally and therefore will never change states. The Modem Status Register will always read 0x00.

4.4.10. Scratchpad Register (SCR, Index=0x7)

Table 4- 54 Scratchpad Register (SCR)
Bits 7 – 0
No Function

Bits 7 – 0 Scratchpad Data, D7 - D0

This register has no effect on the UART and may be used to hold data temporarily.

4.4.11. Divisor Latch LSB Register (DLL, Index=0x0, DLAB=1)

Table 4- 55 Divisor Latch LSB Holding Register (DLL)
Bits 7 – 0
Data Bits 7 - 0

Bits 7 – 0 Divisor Latch LSB, D7 - D0

Specifies the low-order byte of the 16-bit divisor used to program the Baud Rate Generator. The Divisor Latch must be loaded during initialization to ensure proper operation of the Baud Rate Generator. See D.3, “Programmable Baud Rate Generator” on page D-3 for divisor settings.

4.4.12. Divisor Latch MSB Register (DLM, Index=0x1, DLAB=1)

Table 4- 56 Divisor Latch MSB Register (DLM)
Bits 7 – 0
Data Bits 7 - 0

Bits 7 – 0 Divisor Latch MSB, D15 - D8

Specifies the high-order byte of the 16-bit divisor used to program the Baud Rate Generator. The Divisor Latch must be loaded during initialization to ensure proper operation of the Baud Rate Generator. See D.3, "Programmable Baud Rate Generator" on page D-3 for divisor settings.

4.5. FIR Control Registers

4.5.1. Master Control Register (All Banks, Index=0x0)

Table 4- 57 Master Control Register: All Banks, Address 0, R/W)

Bit 7	Bit 6	Bit 5	Bits 4 - 0
Interrupt Enable	Tx Enable	Rx Enable	Bank Select

Bit 7 Interrupt Enable

Setting this bit to 1 enables all FIR Controller interrupts.

Bit 6 Tx Enable

Setting this bit to 1 enables the transmitter logic in the FIR Controller. No packets are transmitted until the transmitter has been enabled.

Bit 5 Rx Enable

Setting this bit to 1 enables the receiver logic in the FIR Controller. No packets are received until the receiver has been enabled.

Bits 4 – 0 Bank Select

Selects the current active register bank.

Note: Only banks 0 through 3 are valid.

4.5.2. Master Status Register (Bank=0, Index=0x1)

Table 4- 58 Master Status Register (Bank 0, Address 1, Read Only)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3 - 1	Bit 0
Transceiver Interrupt	Timer Interrupt	Tx Interrupt	Rx Interrupt	Interrupt Identification (ID2-ID0)	Reserved

Bit 7 Transceiver Interrupt

When set to 1, indicates a transceiver insertion/removal event has occurred. See b4 of the Infrared Configuration 3 Register (4.5.23) for more information.

Bit 6 Timer Interrupt

When set to 1, indicates a timer interrupt is pending.

Bit 5 Tx Interrupt

When set to 1, indicates a transmitter interrupt is pending.

Bit 4 Rx Interrupt

When set to 1, indicates a receiver interrupt is pending. The following conditions clear the Rx Interrupt condition:
Reading the Rx Ring Frame Counter Low Register
Issuing a Reset Rx Special Condition Interrupt command
Clearing the Rx Enable bit (b5 of Master Control Register)
Hardware Reset
Software Reset

Bits 3 – 1 Interrupt Identification, ID2 - ID0

This 3-bit identification code provides an alternative method for identifying the interrupt source by indicating the interrupt type and priority level as shown in the following table.

Table 4- 59 Interrupt Identification

Interrupt Type	**ID2**	**ID1**	**ID0**	**Priority**
Rx Special Condition: FIFO Overrun Frame Error EOF Rx Abort Sync/Hunt	1	0	0	Highest
Rx Data Available	1	0	1	Second
Tx Buffer Empty	1	1	0	Third
Tx Special Condition: FIFO Underrun EOM Early EOM	1	1	1	Fourth

4.5.3. Miscellaneous Control Register (Bank=0, Index=0x1)

Table 4- 60 Miscellaneous Control Register (Bank 0, Address 1, Write)

Bits 7 – 6	**Bit 5**	**Bit 4**	**Bit 3**	**Bits 2 - 0**
DMA Channel Select	Controller Loopback	4 Mbits/s Loopback	En Zero Hold Time	Reserved

Bit 7 – 6 DMA Channel Select

Specifies single or dual DMA channel usage. The internal iDRQ1 line carries all channel 1 DMA requests, and iDRQ2 carries all channel 2 DMA requests. See 4.2.3, "DMA Line Select Register (DLS, Index=0xA2)" on page 4-10 for information on mapping internal iDRQ1 and iDRQ2 lines to external DRQn/$\overline{\text{DACKn}}$ pins.
Note: When using Shared Memory mode, DMA channel 1 must be used for receive and DMA channel 2 must be used for send.

Bit 5 Controller Loopback

Setting this bit to 1 causes the FIR Controller's transmit data output to internally loop back to its receive data input. This allows diagnostic testing of the FIR Controller transmit and receive data paths.

Bit 4 4 Mbits/s Loopback

Setting this bit to 1 causes the 4 Mbits/s modem's transmit data output signal to internally loop back to its receive data input. This allows for diagnostic testing of the modem transmit and receive data paths.

Bit 3 En Zero Hold Time

During a DMA I/O Write cycle the IBM31T1602 requires a minimum data hold time (IOW rising edge to data becomes invalid) of 10ns. Some systems reduce the hold time to close to 0ns, causing incorrect data to be loaded into the transmit FIFO. Setting this bit activates a pair of double latches that extend the system data for more than 40ns, thus eliminating the hold time. However, this also delays the data arrival time by 40ns. This bit is cleared upon reset.

4.5.4. RxFIFO Register (Bank=0, Index=0x2)

Table 4- 61 Read Receive FIFO (Bank 0, Address 2, Read Only)

Bits 7 – 0
Data Bits 7 – 0

Bits 7 – 0 Receive Data, D7 - D0

Used to read receive packet data from RxFIFO, when using PIO and not DMA. For performance reasons PIO data transfer is not recommended.

4.5.5. TxFIFO Register (Bank=0, Index=0x2)

Table 4- 62 Write Transmit FIFO (Bank 0, Address 2, Write Only)

Bits 7 – 0
Data Bits 7 – 0

Bits 7 – 0 Transmit Data, D7 - D0

Used to write transmit packet data to TxFIFO, when using PIO and not DMA. For performance reasons PIO data transfer is not recommended.

4.5.6. TxControl 1 Register (Bank=0, Index=0x3)

Table 4- 63 TxControl 1 Register (Bank 0, Address 3, R/W)

Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Modulator Enable /Request to Send	En TxFIFO Ready Int	En FIFO Underrun /EOM Int	TxFIFO Level	Auto Reset RTS	Auto Reset EOM	Tx Idle	Underrun Abort

Bit 7 Modulator Enable/Request To Send

Setting this bit to 1 enables the 1.152 Mbits/s modulator, which is necessary for transmitted data to appear on the TX pins.

Note that the 1.152 Mbits/s demodulator is disabled with is set. The Modulator Enable bit must be set to 1 prior to loading data into the TxFIFO for proper transmission. Therefore it must be set prior to setting the Tx Enable bit in the Master Control Register or

connecting the TX DMA channel with the Miscellaneous Control Register. If no data is contained in and RTS and Tx Enable are set, continuous start flags or continuous ones[3] will be sent, based on the state of the Num Start Flag bit. The Tx Idle bit determines if continuous stop flags (AKA start flags) or ones are sent after the packet while the Modulator Enable and Tx Enable are set. In 1.152 Mpbs loopback mode, the transmitted data will not only be looped back internally to the FIR controller, but it will also appear on the external TX pins.

Setting this bit to 0 enables the 1.152 Mbits/s demodulator which is necessary if any data from the RX pins is to be received. At this time the 1.152 Mbits/s modulator is disabled. In 1.152 Mbits/s loopback mode, transmitted data will be looped back internally to the FIR controller but will not appear on the external TX pins.

For 4 Mbits/s IrDA-FIR modulation, this bit is the request to send control bit.

Setting this bit to 1 along with Tx Enable activates the Request to Send (RTS) signal from the FIR controller to the Mbits/s modem. The Tx Enable bit in the Master Control Register can be set either before or after the setting of RTS. Once the Tx Enable is set until the RTS bit is set, continuous preambles or continuous ones will be transmitted, depending on the state of the Num Start Preamble bit.

The Tx Idle bit determines if continuous preambles or ones are sent after the packet while the RTS and Tx Enable are set.

Setting this bit to 0 deactivates the RTS signal from the FIR controller to the 4 Mbits/s modem.

Bit 6 En TxFIFO Ready Int

Setting this bit to 1 enables TxFIFO Ready interrupts (TxFIFO reaches its threshold level). This is provided for interrupt driven PIO data transfers.

Bit 5 En FIFO Underrun/EOM Int

Setting this bit to 1 enables FIFO underrun and EOM interrupts.

Bit 4 TxFIFO Level

Setting this bit to 1 sets the TxFIFO threshold to half-empty level (less than 8 bytes of transmit data remaining).

Setting this bit to 0 sets the TxFIFO threshold to not-full level.

Bit 3 Auto Reset RTS

Setting this bit to 1 enables automatic deactivation of the modem Request To Send line at the end of transmission.

For back-to-back transmission, it is desirable that the Request To Send signal remain active for the entire duration in which packets are transmitted one by one. It is therefore recommended that Auto Reset RTS be disabled while running back-to-back transmissions. The Auto Reset option is really only intended for quick direction changes

[3] In this document continous ones means the same as an IDLE tx pin to the transceiver. The history behind this is that for most forms of IR modulation a 1 is represented by the absence of IR pulses.

on slow processors or an automatic direction change without the need for EOM interrupt processing.

The Auto Reset RTS mechanism will not engage if the EOM condition is cleared before the final closing flag is transmitted. Therefore, it is recommended that when clearing the EOM and expecting to change direction that the RTS is always reset manually, even if the Auto Reset RTS bit is active.

Bit 2 Auto Reset EOM

Used in back-to-back packet transmissions to enable automatic resetting of the end-of-message (EOM) status indication after a successful packet transmission. This eliminates the requirement to issue a Reset FIFO Underrun/EOM Latch command after every successful packet transmission.

Setting this bit to 1 causes the EOM bit to automatically clear when the TxStatus Register is read. Note that the TX DMA channel should be disconnected (with the Miscellaneous Control Register)[4] or the TX count and DMA controller must be ready with the next packet prior to reading the TxStatus Register, because resetting the EOM condition will start DMA of the next packet.

Setting this bit to 0 causes the EOM bit to remain set after the TxStatus Register has been read. Only a Reset FIFO Underrun/EOM Latch command or a hardware reset can clear it.

Again once the EOM bit is cleared DMA of the next packet will start provided Tx Enable and Tx DMA Enable are set. If these bits are not cleared the DMA for the next packet must be set up prior to clearing the EOM bit.

Bit 1 Tx Idle

Setting this bit to 1 causes the TXD output line to remain in the active state (low) when the transmitter is idle.

Setting this bit to 0 causes the transmitter to transmit continuous flags (1Mbps mode) or continuous preambles (4 Mbits/s mode) when the transmitter is idle.

Bit 0 Underrun Abort

When a FIFO underrun condition occurs, the software has two options before transmission is terminated. One option is to send an abort sequence to the receiving end. The other option is to transmit a CRC and an ending/stop flag following the transmission of the last data byte in TxFIFO.

Setting this bit to 1 causes the transmitter to transmit an abort sequence when underrun occurs.

Setting this bit to 0 causes the transmitter to transmit a CRC and an ending/stop flag immediately following the transmission of the last data byte in TxFIFO before the underrun condition occurred.

[4] Disconnecting the TX DMA Channel with the Miscellaneous Control Register holds off the DMA and as a result holds off transmitting the next packet.

4.5.7. TxControl 2 Register (Bank=0, Index=0x4)

Table 4- 64 TxControl 2 Register (Bank 0, Address 4, R/W)				
Bit 7	**Bit 6**	**Bits 5 - 4**	**Bit 3**	**Bits 2 – 0**
Reserved	En Tx CRC	SIR Interaction Pulse (SIP) Control	Num Start Flag/Preamble	Early EOM Interrupt Level

Bit 7 Reserved

This bit must be set to 0 for proper transmit operation

Bit 6 En Tx CRC

Setting this bit to 1 enables automatic CRC generation of all outgoing packets. The CRC is automatically generated by the transmitter logic and transmitted after the data field, but before the ending flag. Setting this bit to 0 disables CRC generation. This allows transmission of packets already containing a valid CRC.

Note: The En Tx CRC bit is set to 1 on power-up.

Bit 5-4 SIR Interaction Pulse (SIP) Control

Commands the FIR modems to send a SIR Interaction Pulse (SIP) based on the bit setting. A 01 bit setting instructs the FIR modems to transmit a SIP at the end of the current packet. A 10 bit setting instructs the FIR modems to transmit a SIP immediately.

Note: SIP Control bits are self-clearing.

Bit 3 Num Start Flag/Preamble

Specifies the number of starting flags (1Mbps mode) or preambles (4 Mbits/s mode) to transmit for a given packet.

Setting this bit to 1 causes only two starting flags (1Mbps mode) or a single preamble (4 Mbits/s mode) to be transmitted per packet.

Setting this bit to 0 causes several starting flags (1Mbps mode) or preambles (4 Mbits/s mode) to be transmitted. Since the transmitter does not start transmitting data until the FIFO is half full, or the entire packet is stored, the transmitter continues to transmit starting flags/preambles. Therefore, the number of starting flags/preambles transmitted is controlled by the rate at which the FIFO is filled. For 4M it can be increased by delaying the setting of the RTS bit, in 1M and 4M it can be increased by delaying connecting the TX DMA channel with the Miscellaneous Control Register.

Bits 2 – 0 Early EOM Interrupt Level

Specifies the number of bytes that must remain in Tx Byte Count before an Early EOM interrupt is generated. The reason for having an interrupt occur before transmission has actually completed is to allow enough time for the software to enter the proper interrupt handler routine, turn the DMA channel around for reception (Single DMA mode), or prepare for another back-to-back transmission. Once in the interrupt handler routine, the software can poll the EOM bit in TxStatus Register to determine exactly when the

transmission ends. (Note if the TxStatus Register is polled the Auto Reset EOM option must not be used for obvious reasons.)

Select
2 1 0
---
0 0 0 Interrupt by EOM
0 0 1 EOM interrupt occurs when the remaining count is 16
0 1 0 EOM interrupt occurs when the remaining count is 32
0 1 1 EOM interrupt occurs when the remaining count is 64
1 0 0 EOM interrupt occurs when the remaining count is 128
1 0 1 EOM interrupt occurs when the remaining count is 256
1 1 0 EOM interrupt occurs when the remaining count is 512
1 1 1 EOM interrupt occurs when the remaining count is 1042

4.5.8. TxStatus Register (Bank=0, Index=0x5)

Table 4- 65 Transmit Status Register (Bank 0, Address 5, Read Only)

Bits 7 – 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	FIFO Underrun	EOM	TxFIFO Ready	Early EOM

Bit 3 FIFO Underrun

When set to 1, indicates TxFIFO ran out of data before the transmitter could finish transmitting all the data (i.e. TxFIFO is empty, and the Tx Byte Count value is greater than zero). This bit must be reset by an explicit FIFO Underrun/EOM Latch command

Bit 2 End of Message

When set to 1, indicates transmission completed successfully. The EOM interrupt occurs immediately after the CRC and ending flag have been transmitted. If Auto Reset EOM (b2 of TxControl 1 Register) is enabled, the EOM bit will automatically clear when the TxStatus Register is read. The EOM bit can also be cleared by a Reset FIFO Underrun/EOM Latch command from the Reset Command Register.

Again once the EOM bit is cleared DMA of the next packet will start provided Tx Enable is set and the TX DMA channel is connected. If these conditions are not met, the DMA for the next packet must be set up prior to clearing the EOM bit.

Bit 1 TxFIFO Ready

When set to 1, indicates TxFIFO is ready for more data transfers. When the En TxFIFO Ready Int bit (b6 of the TxControl 1 Register) is set, an interrupt is generated whenever this condition becomes true. Alternatively, this bit may be polled when the interrupt is disabled. When TxFIFO is full, this bit is set to 0. This bit is provided for PIO data transmission.

Bit 0 Early EOM

When set to 1, indicates the Tx Byte Count has reached the count level set by the Early EOM Interrupt Level (b2-b0 in TxControl 2 Register) bits. This bit is cleared by reading TxStatus.

4.5.9. RxControl Register (Bank=0, Index=0x6)

Table 4- 66 Receive Control Register 1 (Bank 0, Address 6, R/W)						
Bit 7	**Bit 6**	**Bits 5 - 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
RxFIFO Level	En Rx CRC	Rx Address Mode	En Sync/Hunt Change Int	Reserved	En RxFIFO Ready Int	En Rx Special Cond Int

Bit 7 RxFIFO Level

Setting this bit to 1 sets the RxFIFO threshold to half-full (more than 8 bytes of receive data are still remaining in FIFO). Setting this bit to 0 sets the RxFIFO threshold to not empty (more than 1 byte of receive data remaining in FIFO).

Bit 6 En Rx CRC

Setting this bit to 1 enables automatic CRC checking of all incoming packets. Setting this bit to 0 disables CRC checking. Disabling this bit results in no CRC errors being reported.
Note: The En Rx CRC bit is set to 1 on power-up.

Bits 5 – 4 Rx Address Mode
Specifies the type of address filtering to apply for determining which receive frames to accept.
Note: Packets with a universal address 0x7F are always accepted.

Bit 3 En Sync/Hunt Change Int

Setting this bit to 1 enables Sync/Hunt Change interrupts.

Bit 1 En RxFIFO Ready Int

Setting this bit to 1 enables RxFIFO Ready interrupts. This bit is provided for interrupt driven PIO data transfer.

Bit 0 En Rx Special Cond Int

Setting this bit to 1 enables the following receive special condition interrupts:
Overrun
Frame Error
End of Frame (EOF)
Rx Abort

4.5.10. RxStatus Register (Bank=0, Index=0x7)

Table 4- 67 Receive Status Register (Bank 0, Address 7, Read Only)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Rx Abort	Frame Error	FIFO Overrun Int	EOF	Rx Data Available	Sync/Hunt Change	Rx Pin	Reserved

Bit 7 Rx Abort

When set to 1, indicates that an abort sequence was detected in the receive data stream of the current packet. In 1Mbps mode, the abort sequence is characterized by seven or more consecutive 1's in the data stream. In 4 Mbits/s mode, the abort sequence is represented by two or more illegal symbols after a valid start flag but before a complete stop flag; or

an illegal symbol, which is not part of a valid stop flag field, received any time after a valid start flag.

Note: This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 6 Frame Error

When set to 1, indicates a CRC or alignment error was detected in the incoming data stream. This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 5 FIFO Overrun Int

When set to 1, indicates the host processor was not fast enough in removing the data from RxFIFO before it overflowed with receive data.

Note: FIFO overrun is a non-recoverable error. The receiver terminates reception as soon as the overrun condition is detected. Upon receiving the overrun interrupt, the host processor must issue a Reset Rx Special Condition Interrupt command from the Reset Command Register in order to re-enable the receiver for packet reception.

Bit 4 End-of-Frame

When set to 1, indicates an ending/stop flag or abort sequence was detected in the incoming data stream. This bit is automatically cleared upon detection of the beginning/start flag of the next incoming packet.

Bit 3 Rx Data Available

When set to 1, indicates RxFIFO is not empty (i.e. the FIFO contains receive data). When set to 0, indicates RxFIFO is empty. The Rx Data Available bit, when set, does not cause an interrupt; rather it is used to unload the FIFO by polling.

Note: RxFIFO Level (b7 of RxControl Register) has no effect on the Rx Data Available bit.

Bit 2 Sync/Hunt Change

When set to 1, indicates a transition or status change occurred on the internal Sync/Hunt signal. The following conditions cause the Sync/Hunt signal to change states:
When an Enter Hunt Mode command is issued
Valid SDLC start or stop flag is detected (1Mbps mode)
Valid preamble or stop flag is detected (4 Mbits/s mode)

If the En Sync/Hunt Change Int bit (b3 of RxControl Register) is enabled, the setting of the Sync/Hunt Change bit causes an interrupt to the host processor. Reading the RxStatus Register after the interrupt has occurred clears the Sync/Hunt Change bit.

Note: If the En Sync/Hunt Change Int bit is disabled, reading the RxStatus Register will provide the status of the Sync/Hunt signal directly and will not clear this bit.

Bit 1 Rx Pin

This bit can be used to read the active Rx pin of the chip. It is useful for determining the quiescent polarity of a transceiver or for reading low speed consumer IR(TV) data streams.

Note: The values of Rx Abort, Frame Error, and End-of-Frame status bits are stored in a status FIFO. The status FIFO is a 3-bit extension of the RxFIFO (i.e. RxFIFO is 11 bits wide, of which 8 bits are for receive data and 3 bits for the status). During packet reception, each FIFO entry will have an 8-bit receive data field and a 3-bit status field associated with that received byte. Thus, when the RxStatus Register is read, the values of Rx Abort, Frame Error, and End-of-Frame are read out from the top of the status FIFO. Reading the RxStatus Register does not advance the FIFO pointer. Only reading the FIFO data itself will advance the FIFO pointer.

4.5.11. Reset Command Register (Bank=0, Index=0x7)

Table 4- 68 Reset Command Register (Bank 0, Address 7, Write Only)

Bits 7 - 4	**Bits 3 - 0**
Reset Command	Reserved

Bits 7 – 4 Reset Command

Used to send a reset signal to the appropriate hardware in order to clear a particular status condition, a counter, or general reset. Issuing an Enter Hunt Mode command sets the Sync/Hunt Change status bit from a 0 to a 1.

Note: These bits are self-clearing (i.e. a programmer does not need to reset the Reset Command bit value to 0000).

4.5.12. Frame Address Register (Bank=1, Index=0x1)

Table 4- 69 Frame Address Register (Bank 1, Address 1, Write Only)

Bits 7 – 1	**Bit 0**
Rx Frame Address	Reserved and set to 0

Bits 7 – 1 Rx Frame Address, A7-A1

Specifies the address value that must be contained in the address field of incoming frames. Bit 0 is not checked and is always 0. See also the Rx Address Mode setting (b5-b4 in RxControl Register) in 4.5.9, "RxControl Register (Bank=0, Index=0x6)" on page 4-26.

4.5.13. Rx Byte Count Low Register (Bank=1, Index=0x2)

Table 4- 70 Rx Byte Count Low Byte (Bank 1, Address 2, Read Only)

Bits 7 – 0
Rx Byte Count

Bits 7 – 0 Rx Byte Count, D7-D0

Provides a running count (low-order value) of the number of bytes of data being received. This information is useful when receiving back-to-back packets.

4.5.14. Rx Byte Count High Register (Bank=1, Index=0x3)

Table 4- 71 Rx Byte Count High Byte (Bank 1, Address 3, Read Only)	
Bits 7 – 4	**Bits 3 - 0**
Reserved	Rx Byte Count

Bits 3 – 0 Rx Byte Count, D11-D8

Provides a running count (high-order value) of the number of bytes ofdata being received. This information is useful when receiving back-to-back packets.

4.5.15. Rx Ring Frame Pointer Low Register (Bank=1, Index=0x4)

Table 4- 72 Receive Ring Frame Pointer (RFP) Low Byte (Bank 1, Address 4, Read Only)
Bits 7 – 0
Ring Frame Pointer (RFP)

Bits 7 – 0 Ring Frame Pointer (RFP), D7-D0

Used in back-to-back packet reception to provide the end-of-packet pointer value (i.e. a pointer to the last byte of a frame received in RxBuffer).

The RFP value is initially set to 0000. This does not necessarily mean that the pointer is initially pointing to the end of a packet received. Thus, software should not use the RFP value for any computation prior to receiving the first packet.

Note: The order of byte access to the Ring Frame Pointer is critical for ensuring valid pointer values are always obtained. The programmer must ensure that the low byte is read first, followed by the high byte.

4.5.16. Rx Ring Frame Pointer High Register (Bank=1, Index=0x5)

Table 4- 73 Receive Ring Frame Pointer (RFP) High Byte (Bank 1, Address 5, Read Only)	
Bits 7 – 6	**Bits 5 - 0**
Reserved	Ring Frame Pointer (RFP)

Bits 5 – 0 Ring Frame Pointer (RFP), D13-D8

Used in back-to-back packet reception to provide the end-of-frame pointer value (i.e. a pointer to the last byte of a frame received in RxBuffer). See 4.5.15, “Rx Ring Frame Pointer Low Register (Bank=1, Index=0x4)”.

4.5.17. Tx Byte Count Low Register (Bank=1, Index=0x6)

Table 4- 74 Tx Byte Count Low Byte (Bank 1, Address 6, R/W)
Bits 7 – 0
Byte Count Bit 7 - 0

Bits 7 – 0 Tx Byte Count, D7 - D0

Provides a running count of the number of bytes remaining to be transmitted. Before enabling transmission, software loads this register with the low-order byte length of the data packet. Each time TxFIFO is written to, the value of this counter decrements by 1.

When the counter reaches zero, the transmitter ceases to make DMA requests. Transmission continues until TxFIFO is depleted.

4.5.18. Tx Byte Count High Register (Bank=1, Index=0x7)

Table 4- 75 Tx Byte Count High Byte (Bank 1, Address 7, R/W)

Bits 7 – 4	**Bits 3 - 0**
Reserved	Byte Count Bits 11 - 8

Bits 3 – 0 Tx Byte Count, D11 - D8

Specifies the high-order byte length of the data packet to be transmitted. See 4.5.17, "Tx Byte Count Low Register (Bank=1, Index=0x6)".

4.5.19. Infrared Configuration 1 Register (Bank=2, Index=0x1)

Table 4- 76 Infrared Configuration 1 Register (Bank 2, Register 1, R/W)

Bits 7 – 4	**Bits 3 - 0**
Infrared Speed Setting for 1.152 Mbits/s mode	Infrared Modulation Scheme

Bits 7 – 4 Infrared Speed Setting for 1.152 Mbits/s mode

Specifies the data rate for 1.152 Mbits/s IrRDA-FIR modulation. For HP-SIR/IrDA-SIR and Sharp ASK, the data rate is set via divisor latch registers in the UART.

IR Speed Bits				
7	6	5	4	Infrared Data Rate (1.152 Mbits/s mode)
0	0	0	0	1.152 Mbits/s
0	0	0	1	576 kbits/s
0	0	1	0	288 kbits/s
0	0	1	1	Reserved
1	X	X	X	Reserved
X	1	X	X	Reserved

Bits 3 – 0 Infrared Modulation Scheme

Specifies the modulation mode for infrared communication.

IR Modulation Bits				
3	2	1	0	Infrared Modulation
0	0	0	0	HP-SIR/IrDA-SIR
0	0	0	1	Sharp ASK
0	0	1	0	1.152 Mbits/s IrDA-FIR
0	0	1	1	TV Direct
0	1	0	0	4 Mbits/s IrDA-FIR
0	1	1	X	Reserved
0	1	X	1	Reserved
1	X	X	X	Reserved

4.5.20. Infrared Transceiver Control Register 1 (Bank=2, Index=0x2)

Table 4- 77 Transceiver Control Register (Bank 2, Register 2, R/W)							
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GPIO_A	GPIO_B	GPIO_C	XCVROFF	Echo On	IRBUSY	TXD Force	GPIO_D

Bit 7 General Purpose Input/Output, GPIO_A

Setting this bit to 1 causes the external GPIO_A pin to be asserted. Setting this bit to 0 causes the external GPIO_A pin to be deasserted.

Bit 6 General Purpose Input/Output, GPIO_B

Setting this bit to 1 causes the external GPIO_B pin to be asserted. Setting this bit to 0 causes the external GPIO_B pin to be deasserted.

Bit 5 General Purpose Input/Output, GPIO_C

Setting this bit to 1 causes the external GPIO_C pin to be asserted. Setting this bit to 0 causes the external GPIO_C pin to be deasserted.

Bit 4 XCVROFF

Setting this bit to 1 causes the external XCVROFF pin to be asserted. Setting this bit to 0 causes the external XCVROFF pin to be deasserted.

Note: That the XCVROFF pin will always be asserted regardless of this bit setting if the macro is in power down mode.

Bit 3 Echo On

Setting this bit to 1 enables the SIR optical modem to loop back its modulated transmit data to its receive path. This bit is set to 0 on power-up.

Use of this feature as an optical loopback capability may not be reliable as the integrity of the fed back signal is a function of the capability of the IR transceiver to cleanly receive its own transmitted signal. Receiver saturation may prove to be a problem.

Bit 2 IRBUSY

Setting this bit to 1 causes the external IRBUSY pin to be asserted. Setting this bit to 0 causes the external IRBUSY pin to be deasserted. When IRBUSY is active, shutdown of the controller is inhibited.

Bit 1 TXD Force

Setting this bit to 1 causes the external TXD pin to be asserted. Setting this bit to 0 causes the external TXD pin to be deasserted.

Note: This bit must be set to 0 for normal operation. Also, this bit is set to 0 on power-up.

Bit 0 General Purpose Input/Output, GPIO_D

Setting this bit to 1 causes the external GPIO_D pin to be asserted. Setting this bit to 0 causes the external GPIO_D pin to be deasserted.

4.5.21. Infrared Transceiver Control Register 2 (Bank=2, Index=0x3)

Table 4- 78 Infrared Transceiver Control Register 2 (Bank 2, Register 3, R/W)						
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1 - 0
Drive GPIO_A	Drive GPIO_B	Drive GPIO_C	Drive GPIO_D	Rx Invert	Rx Select	IRQ Merge

Bit 7 Drive GPIO_A

This bit controls whether the GPIO_A pin is in an input or output state. When the bit is set, the pin is in an output state. On reset the pin is in an output state.

Bit 6 Drive GPIO_B

This bit controls whether the GPIO_B pin is in an input or output state. When the bit is set, the pin is in an output state. On reset the pin is in an output state.

Bit 5 Drive GPIO_C

This bit controls whether the GPIO_C pin is in an input or output state. When the bit is set, the pin is in an output state. On reset the pin is in an output state.

Bit 4 Drive GPIO_D

This bit controls whether the GPIO_D pin is in an input or output state. When the bit is set, the pin is in an output state. On reset the pin is in an input state.

Bit 3 Rx Invert

This bit controls whether the Rx channel is active high (1) or active low (0).

Bit 2 Rx Select

This bit selects which Rx pin is routed to the demodulators. 0 selects the primary Rx channel (RXD1), 1 selects the auxiliary channel (RXD2).

Bits 1 - 0 IRQMerge1, IRQMerge0

These two bits control the Dynamic Interrupt Merge function. This feature allows for a software driver to force the merging of the FIR and the UART interrupts dynamically. Setting these two bits to 1 is another way to disable all interrupts to the host system.

Table 4- 79 IRQMerge		
IRQMerge1	**IRQMerge0**	**Effect**
0	0	No merge. Default mode.
0	1	Merged IRQ appears at UIRQ pin.
1	0	Merged IRQ appears at FIRQ pin.
1	1	Interrupt disabled.

4.5.22. General Purpose Timer Register (Bank=2, Index=0x4)

Table 4- 80 General Purpose Timer Register (Bank 2, Register 4, R/W)
Bits 7 – 0
Timer Value

Bits 7 – 0 Timer Value, D7 - D0

Specifies the initialization value for the down-counter. The counter has a period of 128 us. When the counter reaches a value of zero, an interrupt is generated.

4.5.23. Infrared Configuration 3 Register (Bank=2, Index=0x5)

Table 4- 81 Infrared Configuration 3 Register (Bank 2, Register 5, R/W)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
En Sharp CD Int	Sharp Carrier Detect Int	Reserved	$\overline{\text{XCVRDET}}$	En Transceiver Change Int	Transceiver Change Int	En Timer Int	Timer Int

Bit 7 En Sharp CD Int

Setting this bit to 1 enables Sharp Carrier Detect interrupts. To clear the interrupt, software must write a 0 to this bit.

Bit 6 Sharp Carrier Detect Interrupt

When set to 1, this read-only status bit indicates a 500 KHz Sharp DASK carrier has been detected.

Bit 4 $\overline{\text{XCVRDET}}$

This read-only status bit indicates the state of the external $\overline{\text{XCVRDET}}$ input pin. When $\overline{\text{XCVRDET}}$ is high (inactive), it indicates the infrared transceiver is not connected to the IBM31T1602 controller chip, and the XCVROFF output pin will be asserted. When $\overline{\text{XCVRDET}}$ is low (active), the transceiver is connected to the IBM31T1602 controller, and the XCVROFF output pin will be controlled directly by the XCVROFF control bit (b4 of the Infrared Transceiver Control Register, see 4.5.20, "Infrared Transceiver Control Register 1 (Bank=2, Index=0x2)" on page 4-30).

Bit 3 En Transceiver Change Int

Setting this bit to 1 enables Transceiver Change interrupts.

Bit 2 Transceiver Change Int

When set to 1, indicates the infrared transceiver was either inserted or removed from the IBM31T1602 controller chip and caused an interrupt. To clear the interrupt, software must write a 1 to this bit. This bit is self-clearing.

Bit 1 En Timer Int

Setting this bit to 1 enables Timer interrupts.

Bit 0 Timer Int

When set to 1, indicates a timer interrupt is pending. A timer interrupt occurs when the value in the Timer Register reaches zero. To clear the interrupt, software must write a 1 to this bit. This bit is self-clearing.

4.5.24. Modem Tuning Register (Bank=2, Index=6)

Power-up Default 00000000

4.5.24.1 Pre-demodulation Pulse Shaping

The rationale for the Modem Tuning Register will be described before detailing the function of the bits.

It has been found that electrical pulses from transceiver receive pins can vary significantly in 4 Mbits/s PPM mode. This is due to the large dynamic range that IrDA transceivers must handle, as well as gain vs. noise issues. The other modulation schemes within IrDA are more tolerant of pulse width variations and noise. One reason is because a distinction between double and single width pulses is not required. Another reason is that the other modulation schemes have wider pulses.

The pulses in a 4 Mbits/s PPM IrDA stream are nominally either 125 ns (single pulse) or 250 ns (double-pulse) wide. The demodulator must differentiate between single and double-pulse widths. In practice, the single-width electrical pulse from the transceiver can vary widely from 20 to 200 ns. Similarly, the double-width electrical pulse can vary from 140 to 320 ns.

Factors that cause such wide variances are:

Distance from transmitter.
Ambient noise.
Make and model of transceiver

The pulse shaping logic addresses these problems, and is controlled via the Modem Tuning Register. This function allows the macro to be tuned to operate optimally with virtually any transceiver on the market today. This gives the system integrator total flexibility in transceiver selection.

The pulse shaping logic is a small amount of additional logic between the active receive pin and the base 4 Mbits/s demodulator. It adjust the incoming stream to meet the requirements of the base 4 Mbits/s demodulation. The base 4 Mbits/s demodulator accepts 84 ns to 166 ns pulses as valid single pulses, and 208 to 290 ns pulses as valid double-pulses[5].

4.5.24.2 Basic Pulse Shaping Operation

Pre-demodulation pulse shaping will selectively lengthen pulses ('add' operation) or shorten pulses ('chop' operation). The add and chop operations are controlled by "add level" and "chop level" respectively. These levels can be set or disabled directly (by the user) or automatically (by the adaptive logic). Pulses are modified only if they fall into the range set by the current add/chop level.

There are 3 add/chop levels. The add/chop levels increase in steps of 20.93 ns. For example, an "add level" of 2 will lengthen pulses that are between 41.7 ns and 84 ns to 84 ns (base 4 Mbits/s demodulator's minimum single pulse width) and it will lengthen pulses that are between 167 ns and 208 ns to 208 ns (base 4 Mbits/s demodulator's minimum double-pulse width). A "chop level" of '1' will shorten the pulses between 166 ns and 187 ns to 166 ns (base 4 Mbits/s demodulator's maximum single pulse width) and the pulses between 290 ns and 312 ns to 290 ns (base 4 Mbits/s demodulator's maximum double-pulse width).
An add/chop level of '0' disables the corresponding operation.
The following tables illustrate how the different levels will alter the effective limits for single and double pulses.

[5] The exact boundary between single and double-pulses in the base 4 Mbits/s is determined by the 4 M Int. Treshold bit.

Table 4- 82 Active Add Levels and Corresponding 4 Mbits/s Pulse Minimum Limits		
Add Level	**Effective minimum single-pulse widths**	**Effective minimum double-pulse widths**
1	62.5 ns	187 ns
2	41.7 ns	167 ns
3	20.9 ns	145 ns

Table 4- 83 Active Chop Levels and Corresponding 4 Mbits/s Pulse Maximum Limits		
Chop Level	**Effective maximum single-pulse widths**	**Effective maximum double-pulse widths**
1	187 ns	312 ns
2	208 ns	333 ns
3	229 ns	354 ns

The add and chop levels can be controlled independently. However, some combinations of add and chop level conflict at the boundary between single-width and double-width pulses. In such cases, the pulse shaping logic will determine which operation will occur. Normally the user would enable either an add or a chop level but not both.

4.5.24.3 Adaptive Operation

The active chop/add levels can either be set to a fixed value through the Modem Tuning Register or can be set dynamically during the preamble phase of a 4 Mbits/s packet. This dynamic mode of operation is referred to as Adaptive Operation.

Adaptive operation relies on the fact that the preamble phase only contains 125 ns optical pulses. Since no 250 ns optical pulses are present during the preamble, the adaptive pre-demodulation pulse-shaping logic can then decide what appropriate add/chop level is required for the remainder of this packet. To set the level, a single pulse is measured[6] approximately half way through the preamble, at which point most transceivers produce stable pulse widths. The exact pulse measured is 25 pulses after the preamble sequence is first detected. It takes 5 to 10 valid pulses for the base demodulator to detect the preamble. A valid pulse is one that is not merged with an adjacent pulse and that is positioned correctly.

Adaptive operation adjusts the add/chop levels automatically, on a packet-by-packet basis. The measured pulse will activate an add level, a chop level or neither. It will not simultaneously activate an add **and** a chop level.

4.5.24.3.1 Tuning Adaptive Add Operation

Before measuring the preamble sample, the add level will be set according to the Add Level bits of the Modem Tuning Register, thus effectively setting an absolute minimum pulse width. An absolute minimum is needed to reject noise pulses.

Once the preamble sample has been taken, the add level is automatically adjusted so that the effective minimum single-pulse width is either 20.9 or 41.7 ns less than the measured preamble sample. The 20.9 or 41.7 ns adjustment is controlled by the Adaptive Add Tuning bit. However, the effective minimum single-pulse width will never be greater than 84 ns which corresponds to add operation disabled, i.e. add level = 0.

[6] This measurement is a digital sample based on the 48 MHz oscillator, thus having a granularity of 20.9 ns.

The minimum double-pulse width is also adjusted based on the add level selected by the adaptive logic. See Table 4-82 for a cross reference between add levels and pulse minimums.
After a complete packet is received, the add level reverts to the programmed setting in effect before the adaptive adjustment which occurs for each packet.

4.5.24.3.2 Tuning Adaptive Chop Operation

Before measuring the preamble sample, the chop level will be set to 3 thus effectively setting a maximum single pulse of 229 ns.

Once the preamble sample has been taken, the chop level is automatically adjusted so that the effective maximum single-pulse width is 62.5, 41.7 or 20.8 ns greater than the measured preamble sample. The adjustment is controlled by the Chop Level bits. However, the effective maximum single pulse width will never be less than 166 ns, which corresponds to chop operation disabled, i.e., chop level = 0.

The maximum double-pulse width is also adjusted based on the chop level selected by the adaptive logic. See 4-83 for a cross-reference between chop levels and pulse maximums.

After a complete packet is received, the chop level reverts to 3.

4.5.24.4 4 Mbits/s Tuning Options

The bits in the Modem Tuning Register behave differently based on the modem selected. The following description is solely applicable to the 4 Mbits/s modem.

Table 4- 84 Modem Tuning Register in 4 Mbits/s Mode (Bank = 2, Index 6, R/W)

BITS 7-6	BIT 5	BIT 4	BIT 3	BIT 2	BITS 1-0
Add Level	Enable Adaptive Add Operation	Adaptive Add Tuning	Integrator Threshold	Enable Adaptive Chop Operation	Chop Level

BITS 7-6 Add Level

When the adaptive add operation is disabled, these bits set the add level directly. Note that the add level does not have a direct binary correlation to BITS 7-6.

Table 4- 85 Add Level Bit Settings

Add Level BIT 7	Add level BIT 6	Corresponding Add Level	Single-Pulse Minimum	Double-Pulse Minimum
0	0	1	62.5 ns	187 ns
0	1	0 (disabled)	84 ns	208 ns or 188 ns[7]
1	0	2	41.7 ns	167 ns

[7] See "Integrator Threshold bit"

Table 4- 85 Add Level Bit Settings				
Add Level BIT 7	**Add level BIT 6**	**Corresponding Add Level**	**Single-Pulse Minimum**	**Double-Pulse Minimum**
1	1	3	20.9 ns	145 ns

When the adaptive add operation is enabled these bits determine the add level prior to the adaptive adjustment. See section "Adaptive Operation".

BIT 5 Enable Adaptive Add Operation

Setting this bit enables Adaptive Add Operation. Clearing this bit disables Adaptive Add Operation. See section "Adaptive Operation" above.

BIT 4 Adaptive Add Tuning

This bit is '0' upon reset and is only used when Adaptive Add Operation is enabled (see BIT 5 above). During Adaptive Add Operation, this bit determines whether the effective minimum single-pulse width is either 20.9 ns or 41.7 ns less than the measured preamble sample. If this bit is '0', the effective minimum single-pulse width will be 41.7 ns less than the sampled-pulse and when set to '1' it will be 20.9 ns less than the sample (refer to the section "Tuning Adaptive Add Operation").

BIT 3 Integrator Threshold

This bit is reset to '0'. The 4 Mbits/s modem determines if a value is a '1' or a '0' by integrating the number of samples that are '1' during a symbol bit time. At 48 MHz there are six samples per symbol time (125 ns). The pulse minimum is achieved by stretching single pulses to 85 ns or double-pulses to 208 ns before the integrating logic. This bit determines whether four or three 48 MHz samples are required for a bit to be considered valid. The default is four samples. It can lowered to three for greater jitter tolerance for short pulses but, if set, it affects the pulse minimums for back-to-back pulses as follows:

Table 4- 86 4 Mbits/s Jitter Tolerances				
Pulse Width	**Single pulse jitter tolerance based on 4 Mbits/s Int setting**		**Double-pulse jitter tolerance based on 4 Mbits/s Int setting**	
	0	1	0	1
21 ns	Fail or 20 ns	Fail or 40 ns	Single only	Single only
42 ns	Fail or 20 ns	Fail or 40 ns	Single only	Single only
63 ns	Fail or 20 ns	Fail or 40 ns	Single only	Single only
83 ns	20 ns	40 ns	Single only	Single only
104 ns	40 ns	40 ns	Single only	Single only
125 ns	40 ns	40 ns	Single only	Single only
146 ns	40 ns	40 ns	Single or 20 ns	Single or 40 ns
167 ns	40 ns	20 ns	Single or 20 ns	Single or 40 ns
188 ns	20 ns or 40 ns	Double or 20 ns	Single or 20 ns	20 ns or 40 ns
208 ns	Double or 40 ns	Double or 20 ns	20 ns	40 ns
228 ns	Double or 40 ns	Double or 20 ns	40 ns	40 ns
250 ns	Double only	Double only	40 ns	40 ns

Table 4- 86 4 Mbits/s Jitter Tolerances				
Pulse Width	**Single pulse jitter tolerance based on 4 Mbits/s Int setting**		**Double-pulse jitter tolerance based on 4 Mbits/s Int setting**	
	0	1	0	1
271 ns	Double only	Double only	40 ns	40 ns
292 ns	Double only	Double only	40 ns	20 ns
313 ns	Double only	Double only	20 ns or 40 ns	Fail or 20 ns
333 ns	Double only	Double only	Fail or 40 ns	Fail or 20 ns
354 ns	Double only	Double only	Fail or 40 ns	Fail or 20 ns

The integration point starts on (includes) dump when the previous pulse time was 0 but starts 1 sample after the dump when the previous sample was 1 (i.e., a back-to-back pulse). The position just after dump is the ideal position. This gives 85 ns pulses a 21 ns forward jitter (whole pulse) tolerance, but does not give the second part of a back-to-back pulse a forward jitter tolerance, this is not desired because dump for the second part of a back-to-back pulse will already have been adjusted based upon the appearance of the previous edge. This is also why single pulse jitter tolerance is 20 ns at the border condition and not 0,[8]. The integration period for the second pulse period will have been adjusted by 20 ns (in the case of trailing (backward) (whole pulse) jitter, forward jitter tolerance is 40 ns).

BIT 2 Enables Adaptive Chop Operation
Setting this bit enables Adaptive Chop Operation. Clearing this bit disables Adaptive Chop Operation. See section "Adaptive Operation".

BITS 1-0 Chop Level
When the Adaptive Chop Operation is disabled, these bits set the chop level directly. See the table below.

Table 4- 87 Chop Level Bit Setting (Adaptive Chop Operation Disabled)				
Chop Level BIT 1	**Chop Level BIT 0**	**Corresponding Chop Level**	**Single-Pulse Maximum**	**Double-Pulse Maximum**
0	0	0 (disabled)	165 or 187 ns[9]	290 or 312[10]
0	1	1	187 ns	312 ns
1	0	2	208 ns	333 ns
1	1	3	229 ns	354 ns

When the Adaptive Chop Operation is enabled, its adjustment is controlled by these chop level bits. Refer to the table below. See section "Tuning Adaptive Chop Operation" for more details.

Table 4- 88 Tuning Adaptive Chop Operation		
Chop Level BIT 1	**Chop Level BIT 0**	**Adaptive Chop Level Adjustment**

[8] This of course is without the chop circuitry engaged.
[9] See Integrator Threshold bit.
[10] See Integrator Threshold bit.

Table 4- 88 Tuning Adaptive Chop Operation		
0	0	62.5 ns
0	1	41.7 ns
1	0	20.9 ns

4.5.24.5 1.152 Mbits/s and SIR Tuning Options

Table 4- 89 Modem Tuning Register in 1.152 Mbits/s and SIR Modes (Bank = 2, Index 6, R/W)					
BITS 7-6	**BIT 5**	**BIT 4**	**BIT 3**	**BIT 2**	**BITS 1-0**
Pulse Minimum	N/A	N/A	N/A	N/A	N/A

BITS 7-6 Pulse Minimum

These two bits control the minimum pulse width that is accepted by the active demodulator as a valid pulse. Pulse widths below minimum are ignored.

Table 4- 90 Pulse Minimum Settings			
Pulse Minimum BIT 7	**Pulse Minimum BIT 6**	**1.152 Mbits/s Pulse Minimum**	**SIR Pulse Minimum[11]**
0	0	104 ns	751 ns
0	1	125 ns	917 ns
1	0	83 ns	586 ns
1	1	63 ns	419 ns

4.5.25. Shared Memory Page Register (Bank=3, Index=0x1)

Table 4- 91 Shared Memory Page Register (Bank 3, Register 1, R/W)	
Bits 7 – 4	**Bits 3 – 0**
Transmit Page	Receive Page

In shared memory mode this register controls the paging of RAM connected locally to the controller to a smaller memory window in host system memory space. This RAM is used for transmit and receive buffers.

When the controller is in ISA mode, 8 Kbytes of system memory space is mapped using this page register into 32 Kbytes of local RAM. The 8 Kbytes of system memory space is divided into a lower block of 4 Kbytes, which acts as the receive buffer, and an upper 4 Kbyte block of memory, which is the transmit buffer. The lower 4 Kbyte receive buffer maps into the lower 16 Kbytes of local RAM according to the Receive Buffer Page value, while the upper 4 Kbyte transmit buffer maps into the upper 16 Kbytes of local RAM as per the setting of the Transmit Page Buffer.

In PCMCIA mode, 8 Kbytes of system memory can also be mapped into 32 Kbytes of local memory as described above for ISA operation, or shared memory paging can be disabled via bit b6 in the TxDMA Start Address High Register (see 4.5.27, "TxDMA Start Address High Register (Bank=3, Index=0x3)" on page 4-38). If shared memory paging is disabled, the full 32 Kbytes of local memory (upper 16 Kbytes for

[11] Applies to both HP SIR and Sharp ASK modes.

transmit, lower 16 Kbytes for receive) is mapped directly into 32 Kbytes of system memory space. Note that the maximum shared memory size is 32 Kbytes and this is dictated by the controller design. Shared memory sizes less than 32 Kbytes will result in address shadowing.

The address mapping is done in the following manner:

System address bits are SA12 - SA0 (8K)
Shared Memory Address bits are SMA14 - SMA0 (32K)

The Shared Memory Address bits are generated as follows: SA12 => SMA14 SA9 to SA0 => SMA9 to SMA0
IF SA12 = 1 (host access transmit buffer)
TxPage3 to 0 + SA11 to 10 => SMA13 to SMA10
IF SA12 = 0 (host access receive buffer)
RxPage3 to 0 + SA11 to 10 => SMA13 to SMA10

So, for example:
SA12-0 is 0x0CA5, RxPage3-0 is 0x3
SMA14-0 becomes 001 1000 1010 0101

And also:
SA12-0 is 0x1CA5, TxPage3-0 is 0xA
SMA14-0 becomes 111 0100 1010 0101

Wraparound is automatic at the 16 Kbyte boundary.

Bits 7 – 4 Transmit Page Buffer, TxPage3 - TxPage0

These 4 bits determine the base address of a 4 Kbyte memory page in the upper 16 Kbytes of shared memory. The 4 bits allow for 16 possible locations for the Transmit Page Buffer, i.e. the page may start on any 1 Kyte boundary within the upper 16 Kbytes of shared memory.

Bits 3 – 0 Receive Page Buffer, RxPage3 - RxPage0

These 4 bits determine the base address of a 4 Kbyte memory page in the lower 16 Kbytes of shared memory. The 4 bits allow for 16 possible locations for the Receive Page Buffer, i.e. the page may start on any 1 Kbyte boundary within the lower 16 Kbytes of shared memory.

4.5.26. TxDMA Start Address Low Register (Bank=3, Index=0x2)

Table 4- 92 TxDMA Start Address Low Byte (Bank 3, Register 2, R/W)
Bits 7 – 0
TxDMA Start Address

Bits 7 – 0 TxDMA Start Address, A7-A0

Specifies the low-order starting address of transmit packet data in shared memory.

4.5.27. TxDMA Start Address High Register (Bank=3, Index=0x3)

Table 4- 93 TxDMA Start Address High Byte (Bank 3, Register 3, R/W)	
Bits 7 – 6	**Bits 5 - 0**
Reserved	TxDMA Start Address

Bits 5 – 0 TxDMA Start Address, A13 - A8

Specifies the high-order starting address of transmit packet data in shared memory.

4.5.28. Revision ID Register (Bank=3, Index=0x7)

Table 4- 94 Revision ID Register (Bank 3, Register 7, Read Only)
Bits 7 – 0
Revision ID

Bits 7 – 0 Revision ID, ID7 - ID0

These bits indicate the revision level of the Infrared Controller series. The IBM31T1602 returns 0x04, indicating revision level 4.

5 Electrical Specifications

5.1. Recommended Operating Conditions

Table 5-1. Recommended Operating Conditions					
Parameter	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Power Supply	V_{dd}	4.75	5.0	5.25	V
Operating Ambient Temperature	Ta	0		.+60	C

5.2. Power Requirements

Table 5-2. Power Requirements (Preliminary Estimate)	
Mode of Operation	**Typical Power at V_{dd}=3.3**
Hard Powerdown	11 mW
Soft Powerdown	23 mW
IrDA-SIR/HP-SIR	52 mW
Sharp ASK	52 mW
IrDA-FIR, 1.152 Mbits/s	60 mW
IrDA-FIR, 4 Mbits/s	75 mW

Note: Power Conservation mode enabled

5.3. DC Specifications

All TTL I/O interface specifications are from 3.0 V to 3.8 V.

5.3.1. Driver DC Voltage Specifications (in Volts)

Table 5-3. Driver DC Voltage Specifications (in Volts)						
Function	**MAUL**	**MPUL**	**LPUL**	**MPDL**	**LPDL**	**MADL**
TTL	5.50	3.80	2.40	0.50	0.00	-0.50

5.3.2. Driver DC Currents at Rated Voltages

Table 5-4. Driver DC Currents at Rated Voltages				
Driver Type	**V_{high} (V)**	**I_{high} (mA)**	**V_{low} (V)**	**I_{low} (mA)**
4-mA TTL Driver Outputs	2.40	-4.00	0.50	4.00
6-mA TTL Driver Outputs	2.40	-6.00	0.50	6.00
12-mA TTL Driver Outputs	2.40	-8.00	0.50	12.00
24-mA TTL Driver Outputs	2.40	-8.00	0.50	24.00

5.3.3. Receiver DC Voltage Specifications (in Volts)

Table 5-5. Receiver DC Voltage Specifications (in Volts)						
Function	**MAUL**	**MPUL**	**LPUL**	**MPDL**	**LPDL**	**MADL**
TTL	5.50	5.50	2.00	0.80	0.00	-0.50

5.3.4. Receiver DC Current Specifications

Table 5-6. Receiver DC Current Specifications		
Function	**Iil (µa)**	**Iih (µa)**
All receivers, no pull-up	>-1 at V_{in} =LPDL	<1 at V_{in} =MPUL
All receivers with pull-up	-250 at V_{in} =LPDL	<1 at V_{in} =MPUL

Definition of terms:

MAUL (Maximum Allowable Up Level)

The maximum voltage that may be applied for extended periods without affecting the specified reliability.

Circuit functionality is not implied.

MPUL (Most Positive Up Level)

The most positive voltage that maintains circuit functionality. The maximum positive logic level.

LPUL (Least Positive Up Level)

The least positive voltage that maintains circuit functionality. The minimum positive logic level.

MPDL (Most Positive Down Level)

The most positive voltage that maintains circuit functionality. The maximum negative logic level.

LPDL (Least Positive Down Level)

The least positive voltage that maintains circuit functionality. The minimum negative logic level.

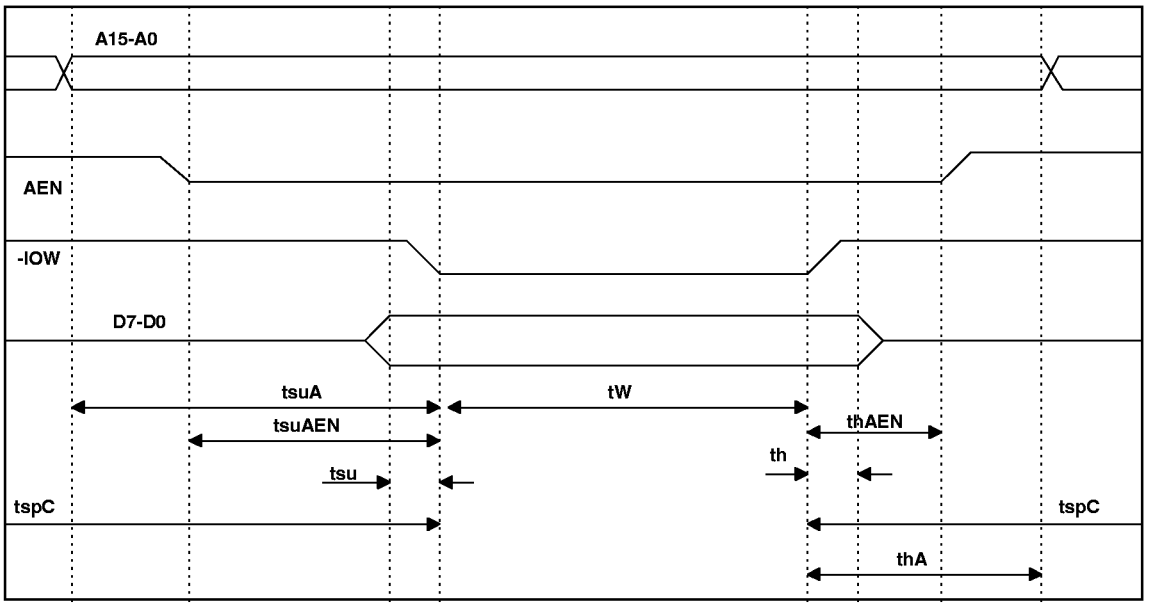
MADL (Minimum Allowable Down Level)

The minimum voltage that may be applied for extended periods without affecting the specified reliability.

Circuit functionality is not implied.

6 Timing Diagrams

6.1. IBM31T1602 in Host DMA Mode, ISA I/O Write Cycle

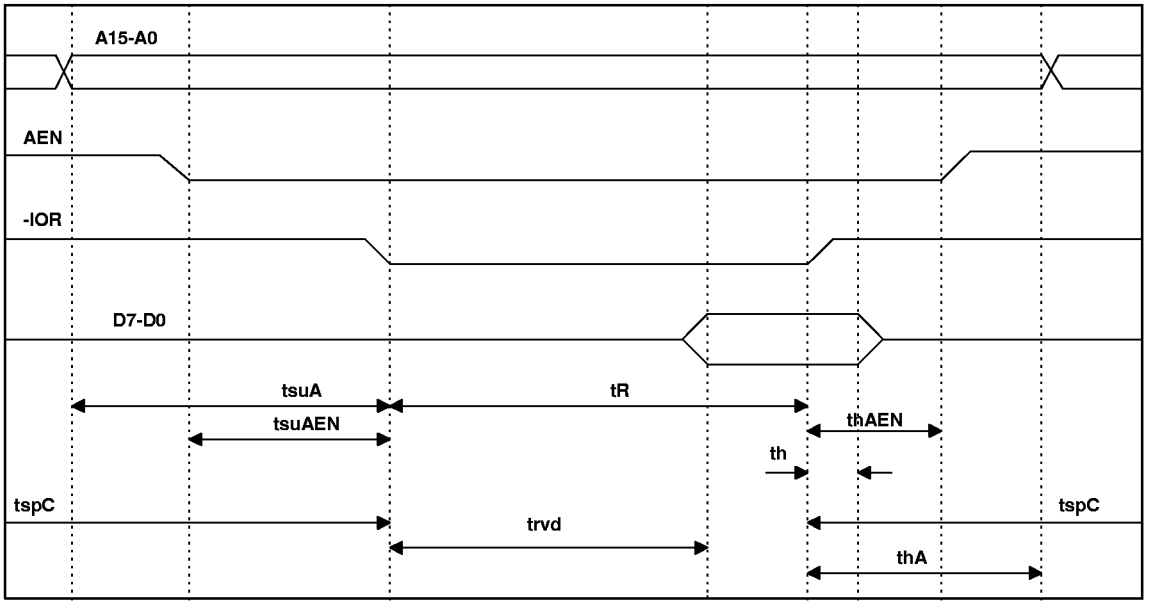


ISA Host I/O Write Timing Specification

Table 6-1. ISA Host I/O Write Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	AEN Setup Time	20	
tsu	Data Setup Time	0	
tW	Write Time	209	
th	Data Hold Time	20	
thAEN	AEN Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.2. IBM31T1602 in Host DMA Mode, ISA I/O Read Cycle

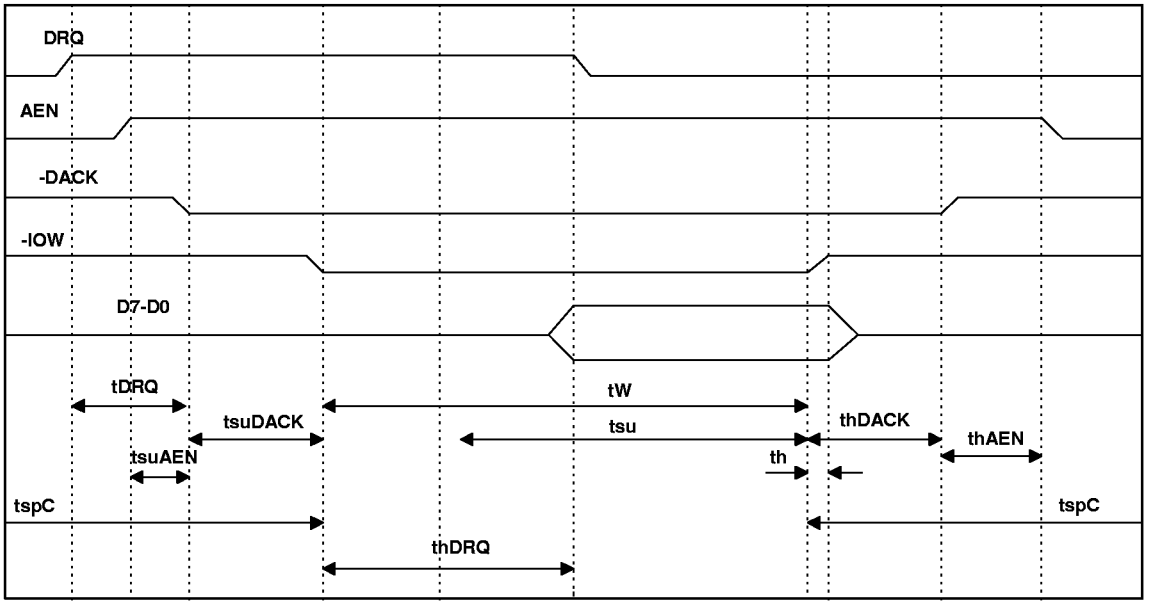


ISA Host I/O Read Timing Specification

Table 6-2. ISA Host I/O Read Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	AEN Setup Time	20	
tsu	Data Setup Time		84
tW	Write Time	168	
th	Data Hold Time	0	30
thAEN	AEN Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.3. IBM31T1602 in Host DMA Mode, ISA DMA Read Cycle (I/O Write)

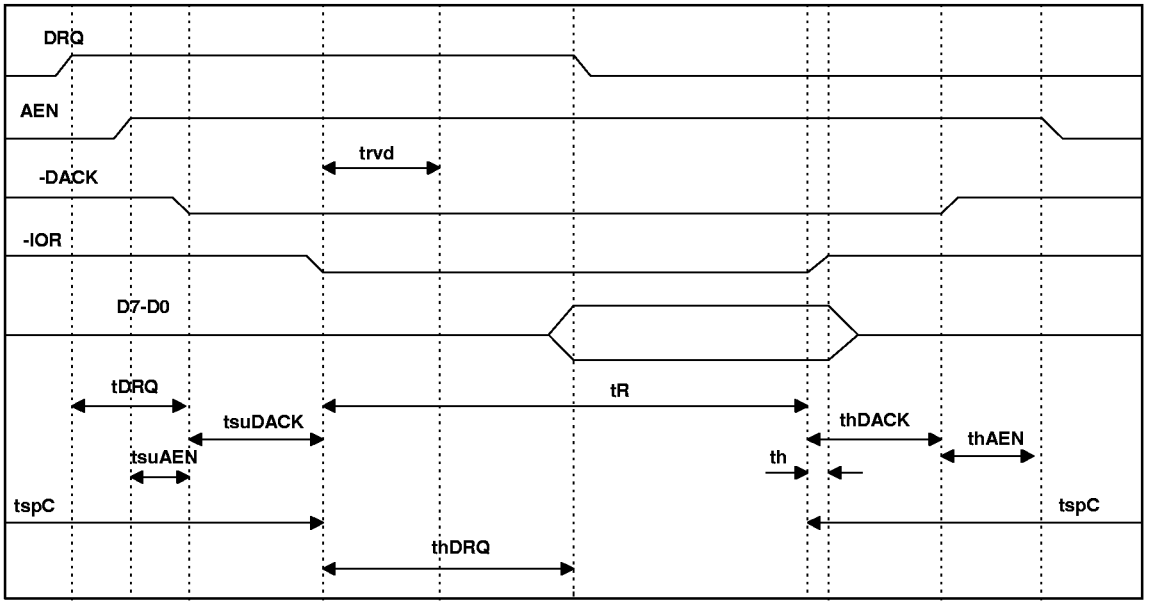


6.3.1. ISA DMA Read (I/O Write) Timing Specification

Table 6-3. ISA DMA Read (I/O Write) Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tDRQ	DMA Request Setup Time (on first transfer)	0	
tsuAEN	AEN Setup Time (on first transfer)	0	
tsuDACK	DMA Acknowledge Setup Time (on first transfer)	20	
thDRQ (on last transfer)	DMA Request Deassertion from Active IOW		160
tW	Write Time	209	
tsu	Data Setup Time	42	
th	Data Hold Time	10	
thDACK	DMA Acknowledge (on last transfer)	20	
thAEN	AEN Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.4. IBM31T1602 in Host DMA Mode, ISA DMA Write Cycle (I/O Read)

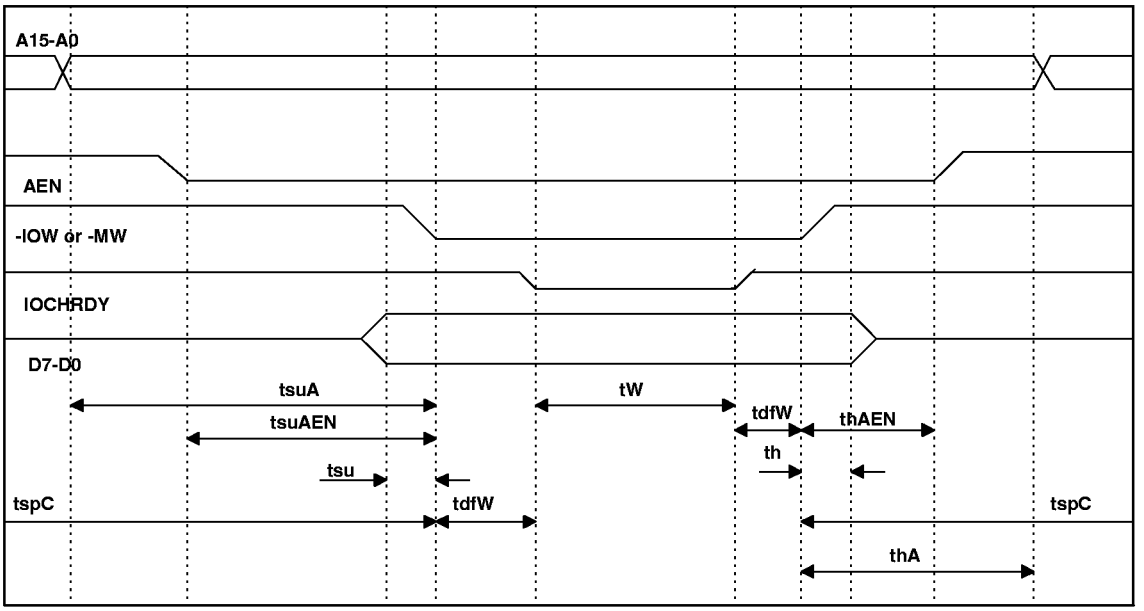


6.4.1. ISA DMA Write (I/O Read) Timing Specification

Table 6-4. ISA DMA Write (I/O Read) Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tDRQ	DMA Request Setup Time (on first transfer)	0	
tsuAEN	AEN Setup Time (on first transfer)	0	
tsuDACK	DMA Acknowledge Setup Time (on first transfer)	20	
thDRQ (on last transfer)	DMA Request Deassertion from Active IOW		160
trvd	Data Valid from Active IOR		31
tR	Read Time	168	
th	Data Hold Time	0	30
thDACK	DMA Acknowledge (on last transfer)	20	
thAEN	AEN Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.5. IBM31T1602 in Shared Memory Mode, ISA I/O or Memory Write Cycle with Wait State

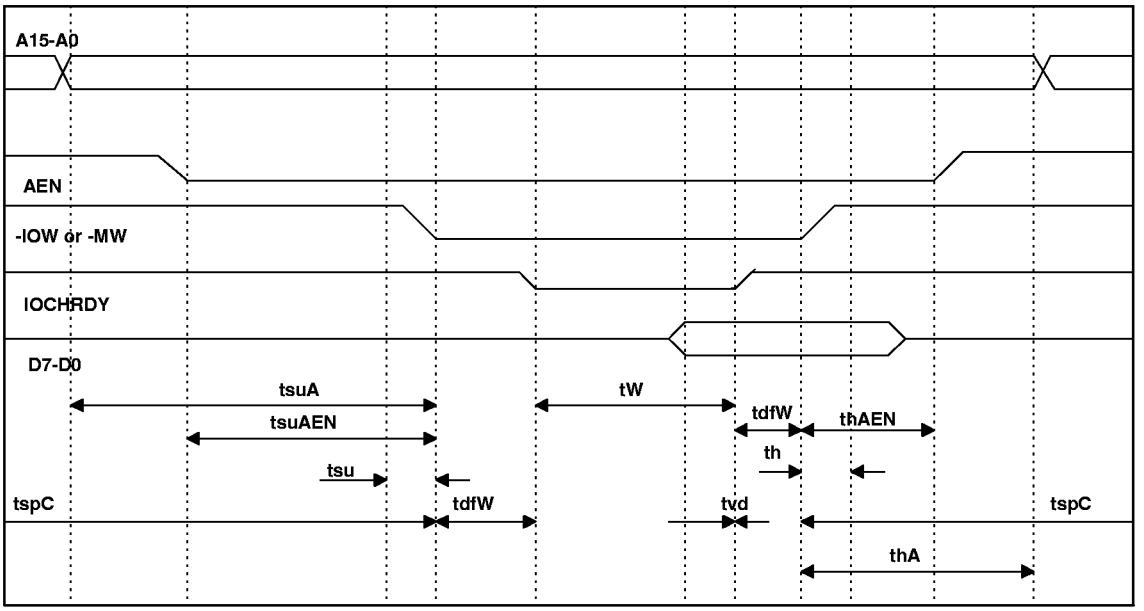


Host I/O Write with Wait State Timing Specification

Table 6-5. Host I/O Write with Wait State Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	AEN Setup Time	20	
tsu	Data Setup Time	0	
tdfW	IOCHRDY Assertion Delay	1	20
tW	IOCHRDY Time	280	6250
tdrW	IOCHRDY Hold Time	1	
th	Data Hold Time	8	
thAEN	AEN Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.6. IBM31T1602 in Shared Memory Mode, ISA I/O or Memory Read Cycle with Wait State

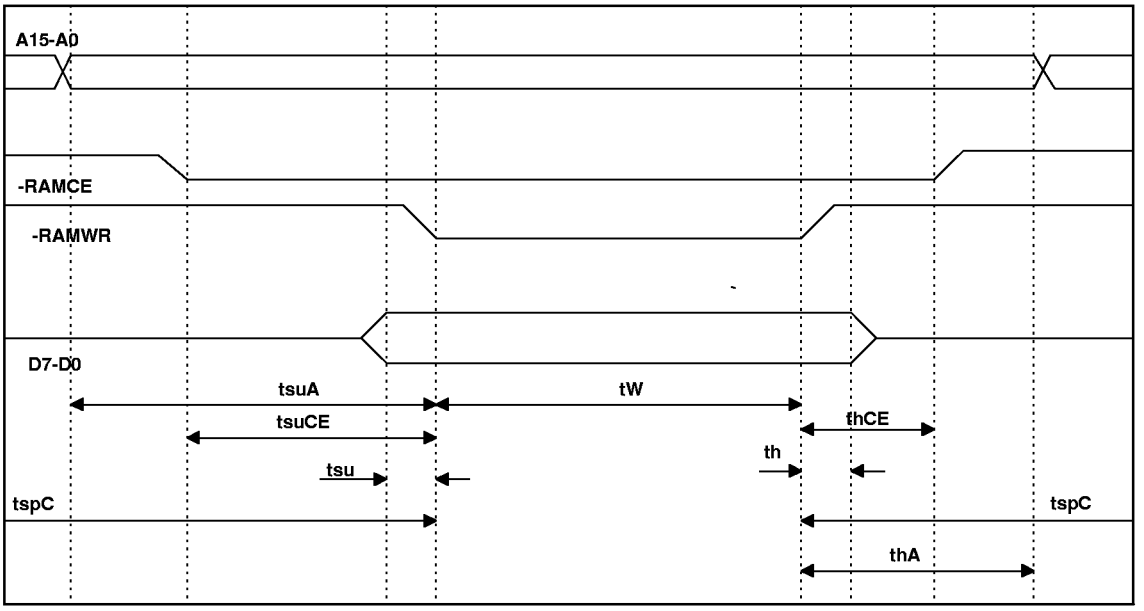


Host I/O Read with Wait State Timing Specification

Table 6-6. Host I/O Read with Wait State Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	20	
tsuAEN	AEN Setup Time	20	
tvd	Data Valid to IOCHRDY Deassertion	0	
tdfW	IOCHRDY Assertion Delay	1	20
tW	IOCHRDY Time	280	6250
tdrW	IOCHRDY Hold Time	0	
th	Data Hold Time	0	30
thAEN	AEN Hold Time	20	
thA	Address Hold Time	20	
tspC	Command (Access) Separation Time	131	

6.7. IBM31T1602 in Shared Memory Mode, Local Memory Write Cycle

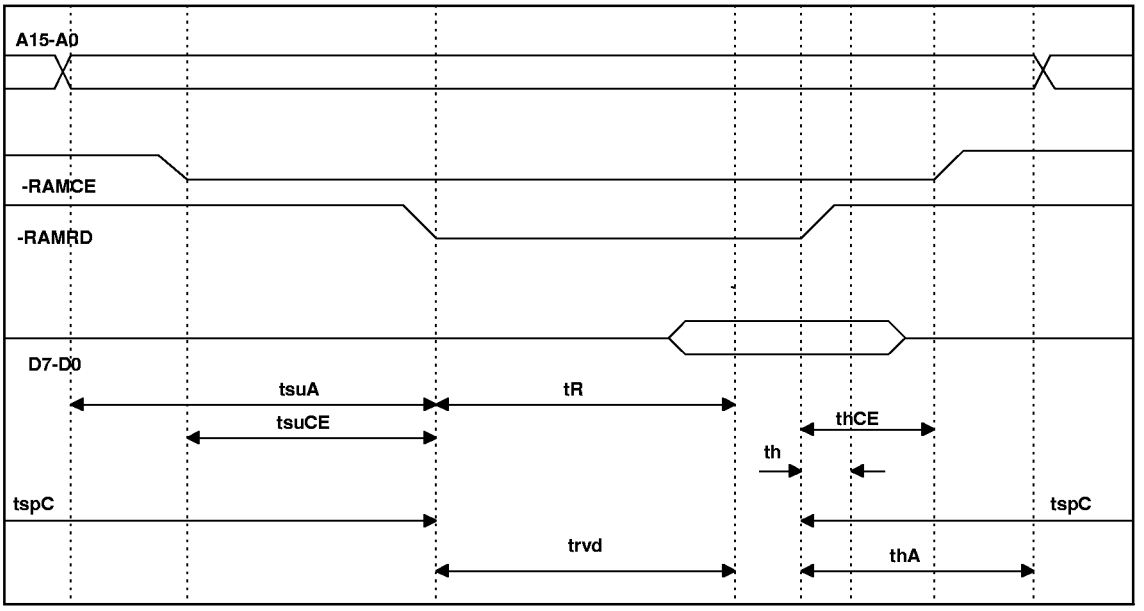


Local Shared Memory Write Timing Specification

Table 6-7. Local Shared Memory Write Timing Specification

Symbol	Description	Min (ns)	Max (ns)
tsuA	Address Setup Time	40	
tsuCE	RAMCE Setup Time	40	
tsu	Data Setup Time	0	
tW	IOCHRDY Time	209	
th	Data Hold Time	40	
thCE	RAMCE Hold Time	40	
thA	Address Hold Time	40	
tspC	Command (Access) Separation Time	96	

6.8. IBM31T1602 in Shared Memory Mode, Local Memory Read Cycle



Local Shared Memory Read Timing Specification

Table 6-8. Local Shared Memory Read Timing Specification

Symbol	Description	Min (ns)	Max (ns)
TsuA	Address Setup Time	40	
TsuCE	RAMCE Setup Time	40	
Tsrvd	Data Valid from active RAMRD		
TR	Read Time	200	
Th	Data Hold Time	0	40
ThCE	RAMCE Hold Time	40	
ThA	Address Hold Time	40	
TspC	Command (Access) Separation Time	96	

Appendix A : Application Notes

A.1 : Metastability in FIR subsystem

Applies to: Host DMA mode and Programmed I/O but not Shared Memory in cases where the -IOR and -IOW host control signals are asynchronous with respect to the IBM31T1602's main clock.
1.152 Mbits/s and 4 Mbits/s

Scenario Possibility of incorrect transmission or reception; hardware CRC generator/checker cannot be relied upon to detect this.

Workaround Implement a software CRC generator/checker to catch for rare transmission/reception problems, or use shared memory mode instead.

The alternative fix is to ensure that transitions on the -IOR and -IOW lines occur on the falling edge of the IBM31T1602's main 48 Mhz clock. This may actually be the design point in some embedded systems with a common master clock that is used for derivation for I/O command signal timings as well as IBM31T1602 operation. If this is not the cases, a small external circuit (for instance using a PAL) can be used to ensure the timing alignment. the IBM31T1602. This avoids the metastability condition. It can be

Impact System dependant. The workaround is more of a performance impact than a functional impact. On fast machines the impact is low. However, on slower machines there is a greater impact. The workaround does work effectively and has been tested.

A.2 : Premature reset of EOM with Auto Reset RTS on

Applies to: Host DMA mode, Shared Memory and Programmed I/O modes
1.152 Mbits/s

Scenario Possibility of premature reset of EOM if running on a very fast machine, especially with 576 kbps or 288 kbps data rates; if the interrupt handler is quick enough, it is possible that it may reset the EOM bit before the second closing flag is transmitted. (The transmitter interrupt is generated after the first closing flag.) If auto reset RTS is enabled, the RTS bit will not actually be automatically reset because the Auto Reset RTS logic only executes the reset after a second closing flag is sent. the problem created is that the 1.152 Mbits/s internal modem will not receive any data with the RTS bit set to one. quickly and if Auto Reset RTS is on, request.

This results in a scenerio where a packet has been sent with one closing flag (which meets the IrDA specification of a minimum of one closing flag), and the EOM bit has been reset, but the RTS bit is not automatically reset. If the RTS bit is left high, the 1.152 Mbits/s modulator continutes to be in the enabled state while the 1.152, Mbits/s demodulator remains in the disabled state. With the demodulator disabled, data reception will not occur. The RTS bit must be set to zero in order for the receive path to become active.

Note that the reason Auto Reset RTS is ofter utilized is that on slow machines, when using a dual-DMA channel approach in Host DMA mode for example, the interrupt handler may be too slow when resetting the RTS bit during the turn-around from transmit to receive. On fast machines it may not be necessary to even use Auto Reset RTS due to the speed of execution of the interrupt handler. But on slower machines where Auto Reset RTS is used and the interrupt handler can reset the EOM before the second closing flag is sent than this application note is an issue.

Workaround Disable Auto Reset RTS and use the software interrupt handler to reset RTS after packet transmission, or, disregard the issue if the machine is slow enough or clear the TX Enable bit after resetting the EOM bit since this automatically resets the RTS bit, or guarantee a one byte time delay in the interrrupt handler before clearing the EOM bit. A one byte

delay can be implemented by repeated I/O reads to a register in the &chip. (e.g. approximently 16 reads for the 1.152 Mbits/s data rate, 32 reads for 576 kbps, and 64 reads for 288 kbps).

Impact Low; multiple workaround exists.

A.3 : Interrupt Status Bits Stability

Applies to: Programmed I/O mode only (not Host DMA or Shared Memory)
1.152 Mbits/s and 4 Mbits/s

Scenario Possibility of unstable interrupt status bit states (inter. Pending and interrupt IDs) if further bytes are being received into the RxFIFO.

Workaround Verify all interrupt with the RxStatus and TxStatus registers. If interrupt does not seem valid, ignore it since a further interrupt will occur and can be processed.

Impact Low. Programmed I/O mode is expected to be used less frequently than host DMA/shared memory.

A.4 : Sharp Carrier Detection when in IrDA-FIR mode

Applies to: Host DMA, Shared Memory and Programmed I/O modes
Receiving Sharp ASK, when controller is set to IrDA-FIR

Scenario Sharp ASK carrier detection will not operate unless Power Conservation mode is disabled.

Workaround Disable Power Conservation mode if expecting Sharp transmissions while waiting in IrDA-FIR mode.

Impact Very low; it is anticipated that usually the controller would be in IrDA-SIR if expecting Sharp; or disable Pwr. Con.

A.5 : Sharp Carrier Detection when in IrDA-SIR mode

Applies to: Rcving Sharp ASK, when controller is set to IrDA-SIR

Scenario Sharp ASK carrier detection works properly for all data rates up to 38400 bps on one "zero" transmission, but for 57600 bps and 115200 bps one "zero" transmission is insufficient (two and three zeroes respectively are required for proper detection).

Workaround The controller is not specified for 115200 bps in Sharp ASK mode so the issue may be mute. For 57600 bps it also may be mute. How are connections initiated and by what sequence?. Development does not have the proprietary ASK specification.

Impact Anticipated to be extremely low but needs further investigation into the Sharp ASK protocol, or do not wait in IrDA-SIR mode (go to Sharp-ASK mode) if expecting 57600 bps Sharp data.

A.6 : Hard vs. Soft Powerdown for Plug and Play Shared Memory Mode

Applies to: Only to Plug and Play, Shared Memory mode and no others.
All data rates.

Scenario If a soft powerdown is used to power down the controller and Infrared Wakeup is enabled:

Then the Plug and Play subsystem must be returned to the WaitForKey state in order for the infrared wakeup subsystem logic to become active.

Workaround After setting bit 0 in the Power Management Register to set soft powerdown, software must return to the WaitForKey state to active the IR wakeup logic.

Scenario If the external hard powerdown pin is used to power down the controller, Infrared Wakeup is disabled and the Plug and Play subsystem is in the WaitForKey state.

Then the IRBUSY bit in the FIR controller and the external IRBUSY pin will go active. This is not the correct behaviour for IRBUSY, which is used to signal that the controller is busy with a transmit or receive operation.

Workaround It is recommended that soft powerdown be used as the means to put the controller into powerdown for Plug and Play Shared Memory mode (the same power savings are realized as with hard powerdown). See the above workaround. Alternatively, software could be written so as to ignore IRBUSY in this particular situation if IRBUSY is a meaningful indicator to the code.

Scenario If the external hard powerdown pin is used to power down the controller, Infrared Wakeup is enabled and the Plug and Play subsystem is in the WaitForKey state.

Then the IRBUSY bit in the FIR controller and the external IRBUSY pin will oscillate and the controller will not even correctly enter into power down mode. In fact, the controller may even consume more power with switching going on internally.

Workaround It is recommended that soft powerdown be used as the means to put the controller into powerdown for Plug and Play Shared Memory mode (the same power savings are realized as with hard powerdown). See the above workaround.

Impact Very low. Use soft powerdown instead of hard powerdown.

A.7 : RTS bit is write-only

Applies to: Host DMA, Shared Memory and Programmed I/O modes
1.152 Mbits/s and 4 Mbits/s

Scenario The RTS bit is now specified as a write-only bit. Reading this bit yields an internal modem state, not the state of the RTS bit that was set.

Workaround Writes to this bit continue to be valid, however do not expect to obtain meaningful information from this bit by reading it.

Impact Extremely low. Controller software should not need to read this bit and make decisions, only to write it.

Appendix B : IR Modulation Schemes

HP-SIR Modulation

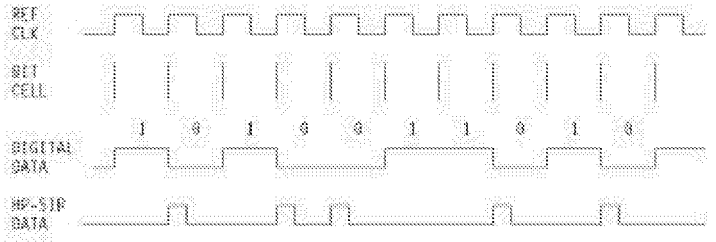


Figure B.1 HP-SIR Modulation

The HP-SIR modulation used for low speed IrDA (up to 115.2 kbits/s) can be either a pulse, 3/16 of the bit time wide, or 1.6 &mu.s wide, at the start of the bit time for a zero value. 1.6 &mu.s is 3/16 of the bit time for the highest baud rate of 115.2 kbits/s. For a one value, no pulse is sent. Data is sent on a byte basis with a Start and Stop bit sent with each byte.

B.2 : Sharp Modulation

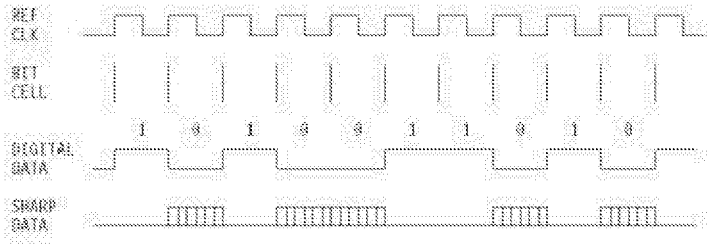


Figure B.2 SHARP ASK Modulation

Sharp Modulation is called either Amplitude Shift Keying (ASK) or Digital Amplitude Shift Keying (DASK). The infrared light is modulated with a sub-carrier with a duty cycle of 50 percent. The sub-carrier has a nominal value of 500 KHz but can range from 450 KHz to 550 KHz. When a zero is sent, the modulated infrared carrier is sent for the entire bit time. For a one, the carrier is not transmitted.

As with the HP mode, data is sent one byte at a time with a Start and Stop bit. An odd parity bit is included with each byte.

B.3 : 1.152 Mbits/s Modulation

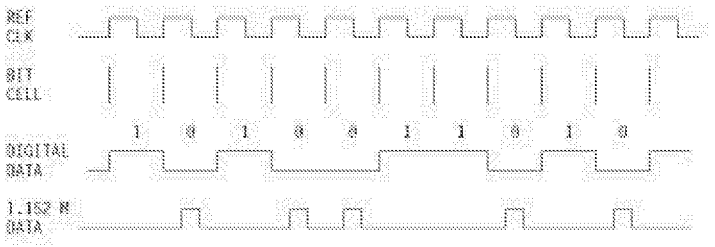


Figure B.3 1.152 Mbps Modulation

1.152 Mbits/s modulation is called RZI/Flash. For a zero bit a pulse 4/16 of the bit time is sent at the middle of the bit time. For a one value, no pulse is sent.

Data is sent using an SDLC protocol, with flags and bit stuffing used to synchronize and extract the data.

B.4 : 4 Mbits/s 4PPM Modulation

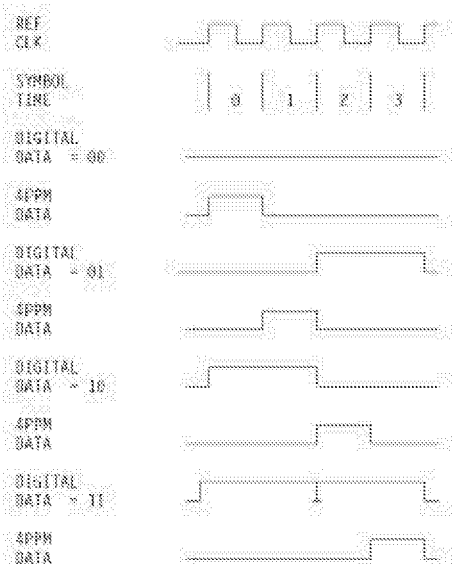


Figure B-4 4 PPM Modulation

Four Position Pulse Modulation (4 PPM) encodes two data bits into one of four possible pulse positions. For every two data bits, only one PPM pulse will be sent.

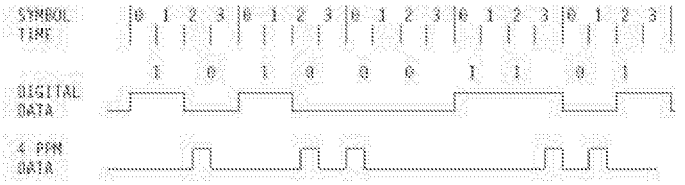


Figure B-5 4 Mbps 4 PPM Modulation

B.4.1 : 4 Mbits/s 4 PPM Format

PREAMBLE	START FLAG	LINK LAYER FRAMER	STOP FLAG

Figure B-6 4 Mbits/s 4 PPM Frame Format

The format of the 4 Mbits/s 4 PPM frame is:

1. Preamble
   - 1000 0000 1010 1000
   - Repeated 16 times
2. Start Flag
   - 0000 1100 0000 1100 0110 0000 0110 0000

Link Layer Frame

Stop Flag

0000 1100 0000 1100 0000 0110 0000 0110

B.4.2 : 4 PPM Baud Rate

The symbol time or pulse width for the 4 Mbits/s 4 PPM modulation is 125 ns. Each 4 PPM symbol will occur once every 500 ns or at a data rate of 2 M symbols/second. The baud rate will then be two times the data rate because each symbol represents two bits or 4 Mbits/s.

Baud Rate = Symbol rate x bits/symbol
= 2 Mbits/s X 2
= 4 Mbits/s

Appendix C : Indirect Configuration Register Default Settings

Indirect Configuration Register Default Settings			
MODE0 CFG2 CFG1 CFG0	**Register**	**Bits 7-0**	**Notes**
X000	**IRC**	0 0 0 0 0 1 0 0	All functions are disabled.
	FIRH	0 0 0 0 0 0 1 1	
	FIRL	0 0 0 0 0 0 0 0	
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
X001	**IRC**	0 0 0 0 0 1 0 1	UART = 0x3F8 - 0x3FF (COM1)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x300 - 0x307
	FIRL	0 0 0 0 0 0 0 0	IRQ4 used
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
X010	**IRC**	0 0 0 0 0 0 0 1	UART = 0x2F8 - 0x2FF (COM2)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x300 - 0x307
	FIRL	0 0 0 0 0 0 0 0	IRQ3 used
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
X011	**IRC**	0 0 0 0 0 1 0 1	UART = 0x3E8 - 0x3EF (COM3)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x310 - 0x317
	FIRL	0 0 0 1 0 0 0 0	IRQ4 used
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
0100	**IRC**	0 0 0 0 0 0 0 1	UART = 0x2E8 - 0x2EF (COM4)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x310 - 0x317
	FIRL	0 0 0 1 0 0 0 0	IRQ3 used
	DLS	0 0 0 0 0 0 0 0	
	UARTL	1 1 1 0 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
0101	**IRC**	0 0 0 0 0 1 0 1	UART = 0x338 - 0x33F (COM3)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x330 - 0x337
	FIRL	0 0 1 1 0 0 0 0	IRQ4 used
	DLS	0 0 0 0 0 0 0 0	
	UARTL	0 0 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 1	
0110	**IRC**	0 0 0 0 0 0 0 1	UART = 0x2F8 - 0x2FF (COM2)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x300 - 0x307
	FIRL	0 0 0 0 0 0 0 0	IRQ3 used
	DLS	0 0 0 0 0 0 0 1	DMA channel 1 connected to FIR DMA channel 1
	UARTL	1 1 1 1 1 0 0 0	
	UARTH	0 0 0 0 0 0 1 0	
0111	**IRC**	0 0 0 0 0 0 0 1	UART = 0x2F8 - 0x2FF (COM2)
	FIRH	0 0 0 0 0 0 1 1	FIR = 0x300 - 0x307
	FIRL	0 0 0 0 0 0 0 0	IRQ3 used
	DLS	0 0 1 0 0 0 0 1	DMA channel 1 and 2 connected to FIR DMA channel 1 and 2

Indirect Configuration Register Default Settings			
MODE0 **CFG2** **CFG1** **CFG0**	**Register**	**Bits 7-0**	**Notes**
	UARTL **UARTH**	1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 0	respectively
1100	**IRC** **FIRH** **FIRL** **DLS** **UARTL** **UARTH**	0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 1 1 0 0 1 0 0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 1 0	UART = 0x2E8 - 0x2EF (COM4) FIR = 0x310 - 0x317 IRQ3 used Local Memory window enabled at system memory location 0xC800:0x0000-0x1FFF
1101	**IRC** **FIRH** **FIRL** **DLS** **UARTL** **UARTH**	0 0 1 0 0 1 0 1 0 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 1 1 0 1 0 0 0 0 1 1 1 0 1 0 0 0 0 0 0 0 0 0 1 1	UART = 0x3E8 - 0x3EF (COM3) FIR = 0x310 - 0x317 IRQ4 used Local Memory window enabled at system memory location 0xD000:0x0000-0x1FFF
1110	**IRC** **FIRH** **FIRL** **DLS** **UARTL** **UARTH**	0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 1 1 0 0 0 1 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 0	UART = 0x2F8 - 0x2FF (COM2) FIR = 0x300 - 0x307 IRQ3 used Local Memory window enabled at system memory location 0xC400:0x0000-0x1FFF
1111	**IRC** **FIRH** **FIRL** **DLS** **UARTL** **UARTH**	0 0 1 0 0 0 0 1 0 0 0 0 0 0 1 1 0 0 0 0 0 0 0 0 1 1 0 1 0 1 0 0 1 1 1 1 1 0 0 0 0 0 0 0 0 0 1 0	UART = 0x2F8 - 0x2FF (COM2) FIR = 0x300 - 0x307 IRQ3 used Local Memory window enabled at system memory location 0xD400:0x0000-0x1FFF

Appendix D : UART Information

D.1 : UART Reset Control

UART Reset Control		
Register/Signal	**Reset Control**	**Reset State**
IER	Chip Reset	0000 0001 (see note 1)
IIR	Chip Reset	0000 0001
FCR	Chip Reset	0000 0000
LCR	Chip Reset	0000 0000
MCR	Chip Reset	0000 0000
LSR	Chip Reset	0110 0000
MSR	Chip Reset	xxxx 0000 (see note 2)
Signal SOUT	Chip Reset	High
Receiver Line Status Interrupt	Read LSR/Chip Reset	Low/Hi-Z
Receive Data Available Interrupt	Read LSR/Chip Reset	Low/Hi-Z
THR Empty Interrupt	Read IIR/Write THR/Chip Reset	Low/Hi-Z
Modem Status Interrupt	Read MSR/Chip Reset	Low/Hi-Z
RTS	Chip Reset	High
DTR	Chip Reset	High
RxFIFO	Chip Reset/RxFIFO Rest	All Bits Low
TxFIFO	Chip Reset/TxFIFO Rest	All Bits Low
Note: Boldface bits are permanently low Bits 7-4 are driven by the input signals		

D.2 : UART Interrupt Priority Settings Of the Interrupt Identification Register

The following table shows the priority level of the interrupts for the Interrupt Identification register when an interrupt is pending.

UART Interrupt Priority Settings Of Interrupt Identification Register When An Interrupt Is Pending						
ID2	**ID1**	**ID0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	1	1	Highest	Receiver Line Status	Overrun Error Parity Error Framing Error Break Interrupt	Reading LSR
0	1	0	Second	Receive Data Available	Receiver Data Available FIFO Trigger Level Reached	Reading RBR FIFO drops below trigger level
1	1	0	Second	Character Timeout	No characters have been read from or written to RxFIFO during the last 4 character times, and there is at least 1 character in RxFIFO during this time	Reading RBR
0	0	1	Third	THR Empty	Transmitter Holding Register Empty	Reading IIR Register (if source of interrupt) Writing to THR
0	0	0	Fourth	Modem Status	Clear To Send (CTS) Data Set Ready (DSR) Ring Indicator (RI) Data Carrier Detect (DCD)	Reading MSR

D.3 : Programmable Baud Rate Generator

Table D-3 provides the divisor latch settings for programming the Baud Rate Generator. The Baud Rate Generator accepts a 1.8462 MHz clock generated from chip clock, and divides it by any divisor from 1 to 2^{16}-1. The output frequency of the Baud Rate Generator is 16 times the Baud [divisor# = (frequency input) ÷ (baud rate * 16)], and is used to drive the receiver and transmitter logic of the UART.

Note: Using a divisor of zero is not recommended.

UART Divisor Latch Settings

Desired Baud Rate	**Decimal Divisor**
50	2304
75	1536
110	1047
134.5	857
150	768
300	384
600	192
1200	96
1800	64
2000	58
2400	48
3600	32
4800	24
7200	16
9600	12
19.2K	6
38.4K	3
57.6K	2
115.2K	1

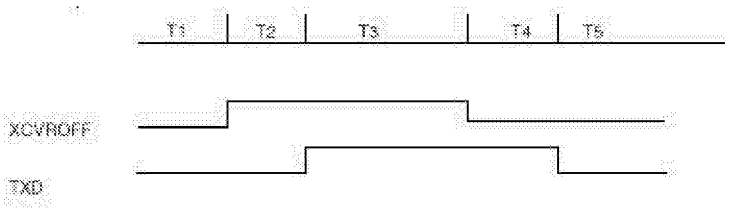
Appendix E : Bandwidth Switching with the IBM31T1101, IBM31T1100 and TFDS6000 Transceivers

Because of the optical pulse width differences between the various infrared data protocols (115.2 kbits/s and below, 1.152 Mbits/s, and 4 Mbits/s), the IBM31T1100, IBM31T1101, and TFDS6000 transceivers need to have their receiver amplifier gain ratio adjusted for proper reception. The transceivers cannot do this automatically; the controller must do the necessary switching. Two serial interface lines are used: the XCVROFF line which acts like a sampling clock (sampling at the falling edge), and the TXD line which provides the speed information (high for 4 Mbits/s IrDA, low for 1.152 Mbits/s and slower IrDA data rates).

In the IBM31T1602, the XCVROFF line is directly driven by the XCVROFF bit (b4) of the Infrared Transceiver Control Register. The TXD line can also be forced to high or low under the control of the TXD Force bit (b1) of the same register. Extreme care should be taken when setting the TXD Force bit to logic 1. *Leaving this bit at a logic 1 value for too long can burn out the LED's of some transceivers, since it directly forces the LED's on.* The following illustrations show programming examples for the transceivers.

E.1 : Switching from SIR Mode to FIR Mode

To change from HP-SIR (115.2 kbits/s or lower) mode or 1.152 Mbits/s mode to 4 Mbits/s mode, the TXD and the XCVROFF lines must be pulsed in this fashion:



T1 The transceiver is currently operating in 1.152 Mbits/s or lower IrDA mode.

T2 Set XCVROFF bit in the Infrared Transceiver Register to 1. This drives the XCVROFF line high. The transceiver enters into a power-down state.

T3 Wait a minimum of 2 µs, then set the TXD Force bit to 1. This drives the TXD line high.[12]

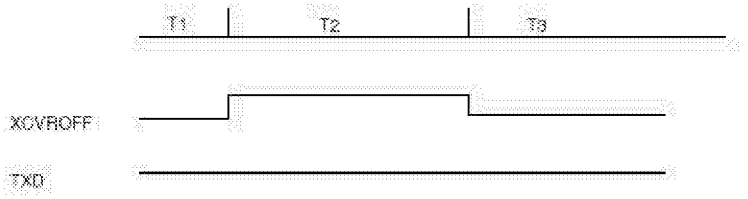
T4 Wait a minimum of 2 µs, then set the XCVROFF bit to 0. The TXD line is sampled by the transceiver and now programmed for 4 Mbits/s IrDA mode.

T5 Wait a minimum of 2 µs, then set the TXD Force bit to 0. Now both the controller and the transceiver are ready for receive or transmit operations.

[12] The programmer must be careful when setting the TXD Force Bit to a value of 1. This bit should not be left at a 1 state for long periods, depending on the application. With transceivers where the TXD line directly affects the turning on and off of an LED, the TXD Force Bit = 1 state (which will force the state of the TXD line to be high) will force the LED on. LED's may burn out and be irreparably damaged if left turned on for an extended period.

E.2 : Switching from FIR Mode to SIR Mode

To change from 4 Mbits/s IrDA mode to 1.152 Mbits/s or lower IrDA mode:



T1 The transceiver is currently operating in 4 Mbits/s IrDA mode. Ensure that data is not being transmitted. It is important that no transmissions take place during this programming sequence since the state of the TXD line must be 0.

T2 Set the XCVROFF bit in the Infrared Transceiver Register to 1. The transceiver enters into a power-down state.

T3 Wait a minimum of 2 µs, then set the XCVROFF bit to 0. Since the TXD Force bit should always be 0 there should be no need to alter this bit (it is 0 on power-up, and should never be set and left at a 1 value, lest transceiver damage occur). The TXD line is sampled by the transceiver on the high-to-low transition. The transceiver is now programmed for 1.152 Mbits/s or lower speeds IrDA mode. Both the controller and the transceiver are ready for receive or transmit operations.

Appendix F : Internal Resource Data Structure

The IBM31T1602 allows the designer to define a custom PnP resource data structure by storing it in a serial PROM equivalent to a Xicor X24C01. Unlike the PCMCIA serial PROM data, the bits of the resource data bytes in the serial PROM should be stored such that the low bit(0) of the byte is shifted out before the high bit(7) of the byte. It is stored this way because this is the order in which the Identification bits are checked during the isolation sequence.

Internally the IBM31T1602 has two PnP resource data structures which will be used if a serial PROM is not detected. To force the use of the internal resource data structure, the designer should pull the SER_DATA pin high, with a resistor. Which resource data structure is used depends on the data transfer mode (Host DMA) or (Local DMA [13]).

F.1 : Internal Resource Data Structure - Host DMA

Internal Resource Data Structure - Host DMA		
Position	**Value**	**Description**
0x0000	0x24	Byte 0 of serial ID = 36
0x0001	0x4d	Byte 1 of serial ID = 77
0x0002	0x20	Byte 2 of serial ID = 32
0x0003	0x10	Byte 3 of serial ID = 16
0x0004	0xff	Byte 4 of serial ID = 255
0x0005	0xff	Byte 5 of serial ID = 255
0x0006	0xff	Byte 6 of serial ID = 255
0x0007	0xff	Byte 7 of serial ID = 255
0x0008	0xa9	Check sum for ID
0x0009	0x0a	Short resource. Plug and Play Version number
0x000a	0x10	=16
0x000b	0x00	=0
******	****	End of Resource
0x000c	0x82	ANSI ID string
0x000d	0x16	Bits 7-0 of length
0x000e	0x00	Bits 15-8 of length
0x000f	0x33	"3"
0x0010	0x31	"1"
0x0011	0x54	"T"
0x0012	0x31	"1"
0x0013	0x36	"6"
0x0014	0x30	"0"
0x0015	0x32	"2"
0x0016	0x20	" "
0x0017	0x49	"I"
0x0018	0x52	"R"
0x0019	0x20	" "
0x001a	0x43	"C"
0x001b	0x6f	"o"
0x001c	0x6e	"n"
0x001d	0x74	"t"
0x001e	0x72	"r"

[13] Shared memory

0x001f	0x6f	"o"
0x0020	0x6c	"l"
0x0021	0x6c	"l"
0x0022	0x65	"e"
0x0023	0x72	"r"
0x0024	0x00	\0
******	****	End of Resource
0x0025	0x47	Short resource. I/O port identifier 1(UART)
0x0026	0x01	=1 Decode 16 bit ISA address
0x0027	0x30	=48 Minimum Address bits 7:0
0x0028	0x00	=0 Minimum Address bits 15:8
0x0029	0xf8	=248 Maximum Address bits 7:0
0x002a	0xff	=255 Maximum Address bits 15:8
0x002b	0x08	=8 (Align on 8 byte boundary)
0x002c	0x08	=8 (8 contiguous ports required)
******	****	End of Resource
0x002d	0x23	Short resource. IRQ MASK (UART)
0x002e	0x38	=56 IRQ bits 7-0, 5,4 and 3 set
0x002f	0xac	=172 IRQ bits 15-8, 15,13,11 and 10 set
0x0030	0x09	=9 Low Level sensitive and high edge sensitive supported
******	****	End of Resource
0x0031	0x47	Short resource. I/O port identifier 1(FIR)
0x0032	0x01	=1 Decode 16 bit ISA address
0x0033	0x30	=48 Minimum Address bits 7:0
0x0034	0x00	=0 Minimum Address bits 15:8
0x0035	0xf8	=248 Maximum Address bits 7:0
0x0036	0xff	=255 Maximum Address bits 15:8
0x0037	0x08	=8 (Allign on 8 byte boundary)
0x0038	0x08	=8 (8 contiguous ports required)
******	****	End of Resource
0x0039	0x23	Short resource. IRQ MASK (FIR)
0x003a	0x38	=56 IRQ bits 7-0, 5,4 and 3 set
0x003b	0xac	=172 IRQ bits 15-8, 15,13,11 and 10 set
0x003c	0x09	=9 Low Level sensitive and high edge sensitive supported
******	****	End of Resource
0x003d	0x2a	Short resource. Primary DMA channel
0x003e	0x0f	=15 DMA0-3 can be used
0x003f	0x08	=8 8 bit DMA only
******	****	End of Resource
0x0040	0x2a	Short resource. Secondary DMA channel
0x0041	0x0f	=15 DMA0-3 can be used
0x0042	0x08	=8 8 bit DMA only
******	****	End of Resource
0x0043	0x79	END TAG
0x0044	0xb5	Value for Checksum to be 0

F.2 : Internal Resource Data Structure - Local DMA

Internal Resource Data Structure - Local DMA		
Position	**Value**	**Description**
0x0000	0x24	Byte 0 of serial ID = 36
0x0001	0x4d	Byte 1 of serial ID = 77

0x0002	0x20	Byte 2 of serial ID = 32
0x0003	0x10	Byte 3 of serial ID = 16
0x0004	0xff	Byte 4 of serial ID = 255
0x0005	0xff	Byte 5 of serial ID = 255
0x0006	0xff	Byte 6 of serial ID = 255
0x0007	0xff	Byte 7 of serial ID = 255
0x0008	0xa9	Check sum for ID
0x0009	0x0a	Short resource. Plug and Play Version number
0x000a	0x10	=16
0x000b	0x00	=0
******	****	End of Resource
0x000c	0x47	Short resource. I/O port identifier 1(UART)
0x000d	0x01	=1 Decode 16 bit ISA address
0x000e	0x08	=8 Minimum Address bits 7:0
0x000f	0x00	=0 Minimum Address bits 15:8
0x0010	0xf8	=248 Maximum Address bits 7:0
0x0011	0xff	=255 Maximum Address bits 15:8
0x0012	0x08	=8 (Align on 8 byte boundary)
0x0013	0x08	=8 (8 contiguous ports required)
******	****	End of Resource
0x0014	0x23	Short resource. IRQ MASK (UART)
0x0015	0x38	=56 IRQ bits 7-0, 5,4 and 3 set
0x0016	0xac	=172 IRQ bits 15-8, 15,13,11 and 10 set
0x0017	0x09	=9 Low Level sensitive and high edge sensitive supported
******	****	End of Resource
0x0018	0x47	Short resource. I/O port identifier 1(FIR)
0x0019	0x01	=1 Decode 16 bit ISA address
0x001a	0x08	=8 Minimum Address bits 7:0
0x001b	0x00	=0 Minimum Address bits 15:8
0x001c	0xf8	=248 Maximum Address bits 7:0
0x001d	0xff	=255 Maximum Address bits 15:8
0x001e	0x08	=8 (Align on 8 byte boundary)
0x001f	0x08	=8 (8 contiguous ports required)
******	****	End of Resource
0x0020	0x23	Short resource. IRQ MASK (FIR)
0x0021	0x38	=56 IRQ bits 7-0, 5,4 and 3 set
0x0022	0xac	=172 IRQ bits 15-8, 15,13,11 and 10 set
0x0023	0x09	=9 Low Level sensitive and high edge sensitive supported
******	****	End of Resource
0x0024	0x81	=129 Memory descriptor
0x0025	0x09	Bits 7-0 of length.
0x0026	0x00	Bits 15-8 of length.
0x0027	0x01	=1 Writable,8bit Not cacheable
0x0028	0x20	=32 Address minimum bits 15-8
0x0029	0x00	=0 Address minimum bits 23-16
0x002a	0xe0	=224 Address maximum bits 15-8
0x002b	0x0f	=15 Address maximum bits 23-16
0x002c	0x00	=0 Alignment bits 7-0
0x002d	0x20	=32 Alignment bits 15-8 (8K)
0x002e	0x20	=32 Range Length bits 15-8
0x002f	0x00	=0 Range Length bits 23-16
******	****	End of Resource
0x0030	0x79	END TAG

0x0031	0xc5	Value for Checksum to be 0

7 Appendix G : Pinout Cross Reference

Notes on the following table:

All inputs and outputs are TTL compatible.

The pull-up resistor option guarantees that a logic `1' is applied to the internal receiver circuit when the input pin is left floating. Because of $V_t$, shift of the receiver isolation device, the user should not expect a logic `1's voltage at the external net. The external voltage will be slightly lower even though a logic `1' is shown in the truth table.

Table G-1 Pinout Cross Reference

Pin	**I/O**	**Maximum Output Current**	**Input Capacity**	**ISA Plug and Play Mode**		**ISA Indirect Configuration Mode**		**ISA Direct Configuration Mode**	
				Shared Memory	Host DMA	Shared Memory	Host DMA	Shared Memory	Host DMA
48	Input		4 pF	A15	A15	A15	A15	A15	A15
47	Input		4 pF	A14	A14	A14	A14	A14	A14
46	Input		4 pF	A13	A13	A13	A13	A13	A13
44	Input		4 pF	A12	A12	A12	A12	A12	A12
43	Input		4 pF	A11	A11	A11	A11	A11	A11
42	Input		4 pF	A10	A10	A10	A10	A10	A10
41	Input		4 pF	A9	A9	A9	A9	A9	A9
35	Input		4 pF	A8	A8	A8	A8	A8	A8
34	Input		4 pF	A7	A7	A7	A7	A7	A7
33	Input		4 pF	A6	A6	A6	A6	A6	A6
32	Input		4 pF	A5	A5	A5	A5	A5	A5
30	Input		4 pF	A4	A4	A4	A4	A4	A4
28	Input		4 pF	A3	A3	A3	A3	A3	A3
23	Input		4 pF	A2	A2	A2	A2	A2	A2
21	Input		4 pF	A1	A1	A1	A1	A1	A1
20	Input		4 pF	A0	A0	A0	A0	A0	A0
88	Bidirectional	4 mA	4 pF	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$	$\overline{\text{PWRDWN}}$
54	Output	4 mA	4 pF	IRBUSY	IRBUSY	IRBUSY	IRBUSY	IRBUSY	IRBUSY
22	Bidirectional	4 mA	4 pF			BADDR0	BADDR0		
24	Bidirectional	4 mA	4 pF			BADDR1	BADDR1		
99	Output	6 mA	4 pF	IRQ11	IRQ11	IRQ11	IRQ11		
36	Bidirectional	4 mA	4 pF			CFG2	CFG2		
31	Bidirectional	4 mA	4 pF			CFG1	CFG1		
29	Bidirectional	4 mA	4 pF			CFG0	CFG0		

Table G-1 Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	ISA Plug and Play Mode		ISA Indirect Configuration Mode		ISA Direct Configuration Mode	
				Shared Memory	Host DMA	Shared Memory	Host DMA	Shared Memory	Host DMA
56	Output	4 mA	0.6 pF	$\overline{\text{BUFFEN}}$	$\overline{\text{BUFFEN}}$	$\overline{\text{BUFFEN}}$	$\overline{\text{BUFFEN}}$	$\overline{\text{BUFFEN}}$	$\overline{\text{BUFFEN}}$
49	Output	6 mA	0.6 pF	IRQ3	IRQ3	IRQ3	IRQ3	IRQ3	IRQ3
50	Output	6 mA	0.6 pF	IRQ4	IRQ4	IRQ4	IRQ4	IRQ4	IRQ4
86	Bidirectional	6 mA	0.6 pF	IRQ5	IRQ5	IRQ5	IRQ5	$\overline{\text{SETUP}}$	$\overline{\text{SETUP}}$
91	Bidirectional	4 mA	0.6 pF	SA19		SA19		SA19	
67	Bidirectional	4 mA	0.6 pF	SA18		SA18		SA18	
63	Bidirectional	4 mA	0.6 pF	SA17		SA17		SA17	
58	Bidirectional	4 mA	0.6 pF	SA16		SA16		SA16	
72	Bidirectional	24 mA	0.6 pF	D7	D7	D7	D7	D7	D7
71	Bidirectional	24 mA	0.6 pF	D6	D6	D6	D6	D6	D6
69	Bidirectional	24 mA	0.6 pF	D5	D5	D5	D5	D5	D5
68	Bidirectional	24 mA	0.6 pF	D4	D4	D4	D4	D4	D4
65	Bidirectional	24 mA	0.6 pF	D3	D3	D3	D3	D3	D3
64	Bidirectional	24 mA	0.6 pF	D2	D2	D2	D2	D2	D2
61	Bidirectional	24 mA	0.6 pF	D1	D1	D1	D1	D1	D1
60	Bidirectional	24 mA	0.6 pF	D0	D0	D0	D0	D0	D0
18	Input		4 pF	RESET	RESET	RESET	RESET	RESET	RESET
93	Input		4 pF	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$	$\overline{\text{IOR}}$
94	Input		4 pF	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$	$\overline{\text{IOW}}$
1	Input		4 pF	$\overline{\text{MR}}$		$\overline{\text{MR}}$		$\overline{\text{MR}}$	High
25	Input		4 pF	$\overline{\text{MW}}$		$\overline{\text{MW}}$		$\overline{\text{MW}}$	High
92	Input		4 pF	AEN	AEN	AEN	AEN	AEN	AEN
83	Output	6 mA		IRQ15	IRQ15	FIRQ	FIRQ	FIRQ	FIRQ
82	Output	6 mA		IRQ10	IRQ10	UIRQ	UIRQ	UIRQ	UIRQ
27	Output	24 mA		IOCHRDY		IOCHRDY		IOCHRDY	
55	Output	4 mA		BUFFDIR	BUFFDIR	BUFFDIR	BUFFDIR	BUFFDIR	BUFFDIR
79	Output	6 mA		MA14	DRQ0	MA14	DRQ0	MA14	DRQ0
80	Output	6 mA		MA13	DRQ1	MA13	DRQ1	MA13	DRQ1
81	Output	6 mA		MA12	DRQ2	MA12	DRQ2	MA12	
77	Output	6 mA		MA11	DRQ3	MA11	DRQ3	MA11	
76	Output	6 mA		MA10		MA10		MA10	
75	Output	6 mA		MA9		MA9		MA9	

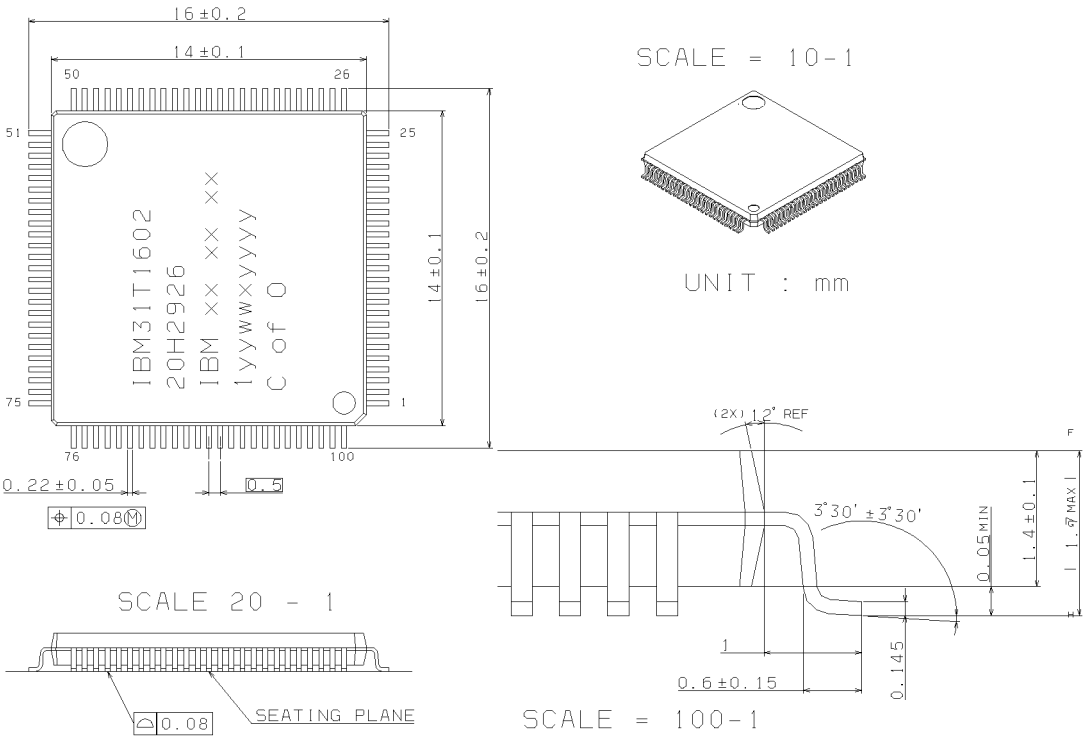
Table G-1 Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	ISA Plug and Play Mode		ISA Indirect Configuration Mode		ISA Direct Configuration Mode	
				Shared Memory	Host DMA	Shared Memory	Host DMA	Shared Memory	Host DMA
74	Output	6 mA		MA8		MA8		MA8	
16	Bidirectional	4 mA	0.6 pF	MA7	$\overline{\text{DACK0}}$	MA7	$\overline{\text{DACK0}}$	MA7	$\overline{\text{DACK0}}$
15	Bidirectional	4 mA	0.6 pF	MA6	$\overline{\text{DACK1}}$	MA6	$\overline{\text{DACK1}}$	MA6	$\overline{\text{DACK1}}$
17	Bidirectional	4 mA	0.6 pF	MA5	$\overline{\text{DACK2}}$	MA5	$\overline{\text{DACK2}}$	MA5	
14	Bidirectional	4 mA	0.6 pF	MA4	$\overline{\text{DACK3}}$	MA4	$\overline{\text{DACK3}}$	MA4	
11	Output	4 mA	0.6 pF	MA3		MA3		MA3	
9	Output	4 mA	0.6 pF	MA2		MA2		MA2	
3	Output	4 mA	0.6 pF	MA1		MA1		MA1	
19	Output	4 mA		MA0		MA0		MA0	
85	Output	6 mA	0.6 pF	IRQ13	IRQ13	IRQ13	IRQ13		
40	Output	4 mA		$\overline{\text{RAMCE}}$		$\overline{\text{RAMCE}}$		$\overline{\text{RAMCE}}$	
45	Output	4 mA		$\overline{\text{RAMRD}}$		$\overline{\text{RAMRD}}$		$\overline{\text{RAMRD}}$	
51	Output	4 mA		$\overline{\text{RAMWR}}$		$\overline{\text{RAMWR}}$		$\overline{\text{RAMWR}}$	
7	Output			TXD	TXD	TXD	TXD	TXD	TXD
98	Output			$\overline{\text{TXD}}$	$\overline{\text{TXD}}$	$\overline{\text{TXD}}$	$\overline{\text{TXD}}$	$\overline{\text{TXD}}$	$\overline{\text{TXD}}$
4	Output	4 mA		XCVROFF	XCVROFF	XCVROFF	XCVROFF	XCVROFF	XCVROFF
5	Bidirectional	12 mA		GPIO_A	GPIO_A	GPIO_A	GPIO_A	GPIO_A	GPIO_A
6	Bidirectional	12 mA		GPIO_B	GPIO_B	GPIO_B	GPIO_B	GPIO_B	GPIO_B
38	Bidirectional	12 mA		GPIO_C	GPIO_C	GPIO_C	GPIO_C	GPIO_C	GPIO_C
52	Bidirectional	12 mA		GPIO_D	GPIO_D	GPIO_D	GPIO_D	GPIO_D	GPIO_D
95	Input		4 pF	$\overline{\text{XCVRDET}}$	$\overline{\text{XCVRDET}}$	$\overline{\text{XCVRDET}}$	$\overline{\text{XCVRDET}}$	$\overline{\text{XCVRDET}}$	$\overline{\text{XCVRDET}}$
96	Input		4 pF	RXD2	RXD2	RXD2	RXD2	RXD2	RXD2
97	Input		4 pF	RXD1	RXD1	RXD1	RXD1	RXD1	RXD1
90	Input		4 pF	CLK48	CLK48	CLK48	CLK48	CLK48	CLK48
100	Output								
26	Bidirectional	4 mA	0.6 pF						
13	Input	12 mA	4 pF	MODE2	MODE2	MODE2	MODE2	MODE2	MODE2
12	Input		4 pF	MODE1	MODE1	MODE1	MODE1	MODE1	MODE1
87	Input		4 pF	MODE0	MODE0	MODE0	MODE0	MODE0	MODE0
2	Input			RXDIEN	RXDIEN	RXDIEN	RXDIEN	RXDIEN	RXDIEN
39	Input			TME	TME	TME	TME	TME	TME
8	Power			VDD	VDD	VDD	VDD	VDD	VDD

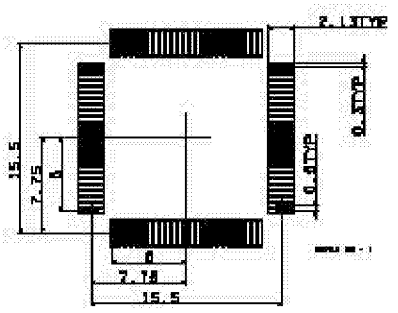
Table G-1 Pinout Cross Reference

Pin	I/O	Maximum Output Current	Input Capacity	ISA Plug and Play Mode		ISA Indirect Configuration Mode		ISA Direct Configuration Mode	
				Shared Memory	Host DMA	Shared Memory	Host DMA	Shared Memory	Host DMA
37	Power			VDD	VDD	VDD	VDD	VDD	VDD
57	Power			VDD	VDD	VDD	VDD	VDD	VDD
62	Power			VDD	VDD	VDD	VDD	VDD	VDD
70	Power			VDD	VDD	VDD	VDD	VDD	VDD
78	Power			VDD	VDD	VDD	VDD	VDD	VDD
89	Power			VDD	VDD	VDD	VDD	VDD	VDD
10	Power			VSS	VSS	VSS	VSS	VSS	VSS
53	Power			VSS	VSS	VSS	VSS	VSS	VSS
59	Power			VSS	VSS	VSS	VSS	VSS	VSS
66	Power			VSS	VSS	VSS	VSS	VSS	VSS
73	Power			VSS	VSS	VSS	VSS	VSS	VSS
84	Power			VSS	VSS	VSS	VSS	VSS	VSS

Appendix H : Packaging Information



H.1 : IBM31T1602 Footprint



Appendix I : Ordering Information

The information provided is believed to be accurate and reliable. IBM reserves the right to make changes to the product described without notice. No liability is assumed as a result of its use nor for any infringement of the rights of others.

This document may contain preliminary information and is subject to change by IBM without notice. IBM assumes no responsibility of liability for any use of the information contained herein. Nothing in this document shall operate as an express or implied license or indemnity under the intellectual property rights of IBM or third parties. Products described in this document are not intended for use in implantation or other direct life support applications where malfunction may result in direct physical harm or injury to persons.

NO WARRANTIES OF ANY KIND, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE ARE OFFERED IN THIS DOCUMENT.

IBM Microelectronics Division
1580 Route 52, BLdg. 504
Hopewell Junction, NY
12533-6531

The IBM home page can be found at http://www.ibm.com.

The IBM Microelectronics Division home page can be found at http://www.chips.ibm.com.

The IBM Microelectronics Division infrared home page can be found at:http://www.chips.ibm.com/products/infrared.

Document Number: GH45-5292-01

Part Number: 08H4427