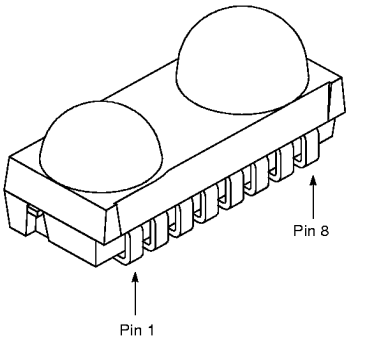
Features

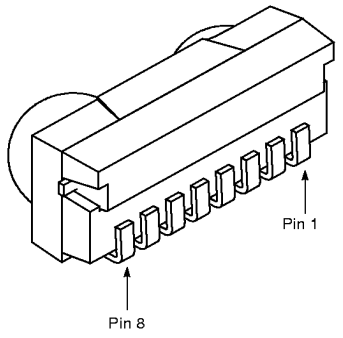
- IrDA, HP-SIR, Local Talk and Sharp ASK
- Ultracompact package:
  - H 4.0 mm x D 4.8 mm x L 9.6 mm
- Data rates from 9600 bit/s to 4 Mbit/s
- Supply voltage 2.7 V to 5.25 V
- Power Shutdown mode (<50 nA)
- Low power consumption
  - ~2 mA @ 2.7 V
  - ~3.3 mA @ 5.25 V
- Zero external resistors required
- Digital Serial Interface:
  Programmable LED current: 10 mA to 500 mA

Description

Responding to the volumetric constraints of today's ultra-compact and power conscious portable products, IBM has developed the next generation in infrared wireless communication transceivers. The transceiver has been designed to support up to 4 Mbit/s IrDA™, HP-SIR™, Local Talk™ and Sharp ASK™ modes. The device combines an LED, photodiode, programmable LED driver and a fully differential receiver into a single integrated package.

Pin Assignments





Pin Number	Symbol	Description
1	LEDA	LED Anode
2	LEDC	LED Cathode
3	TX	Transmit Data
4	$\overline{RX}$	Receive Data
5	SCLK/SD	Serial Interface Clock/Shutdown
6	V_{CC}	Positive Supply (Power)
7	NC	No Connect
8	GND	Ground

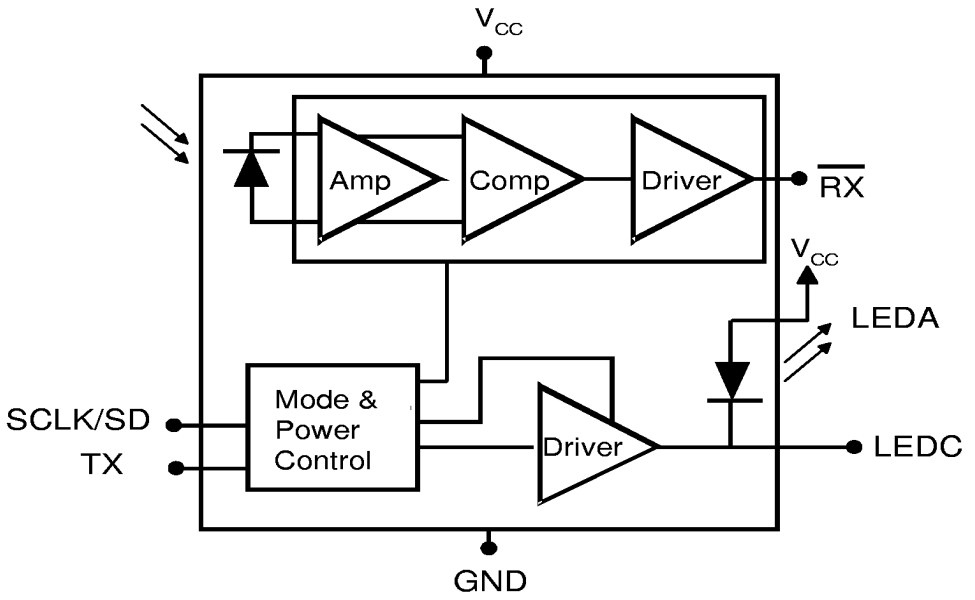
Input/Output Functional Description

Symbol	I/O Type	Polarity	Function
$\overline{RX}$	Output	Active Low	This output indicates received serial data. It is a push-pull CMOS driver capable of driving a standard CMOS or TTL load. No external pull-up or pull-down resistor is required. This output may switch indeterminately when the module is transmitting. This output pin is in tri-state mode when the module is in shutdown mode and during digital serial programming operations.
TX	Input	Active High	This CMOS input is used to transmit serial data when SCLK/SD is low. An on-chip protection circuit disables the LED driver if the TX pin is asserted for longer than 100 µs. When used in conjunction with the SCLK/SD pin, this pin also provides control signals to the internal digital serial interface and legacy mode subsystems.
SCLK/SD	Input	Active High	This CMOS input functions in two modes: Digital Serial Interface and Legacy. Digital Serial Interface Mode: The SCLK/SD pin functions as the rising edge clock signal upon which the TX pin is sampled for digital serial interface programming operations. Through the digital serial interface, features including receiver bandwidth, transmit power (5 power settings) and shutdown mode may be set. Legacy Mode: In 'Legacy Mode', simple power management and bandwidth switching are available in a fashion identical to the original IBM 31T11xx Transceiver Modules (IBM31T1100A, 1100B, 11SL, 11SV and 11TV). Assertion of this pin high for a period of time exceeding 400 µs places the module into shutdown mode. On the falling edge of this signal, the state of the TX pin is sampled and used to set receiver low bandwidth (TX = Low) or high bandwidth (TX = High) mode. See Figures 7 and 8 for timings.
V_{CC}	Positive Supply	-	Connect to positive power supply (2.7 V to 5.25 V). Placement of a 1.0 µF to 10.0 µF ceramic decoupling capacitor as close as possible to the V_{CC} pin is recommended.
GND	Ground (Power)	-	Connect to power supply ground. A solid ground plane is recommended.
NC	No Connect	-	This pin must be left unconnected.
LEDA	Input	-	This pin can be connected directly to V_{CC}. No series resistor is required.
LEDC	Output	-	LED cathode. Leave this pin unconnected. This pin may be monitored to determine the state of the LED.

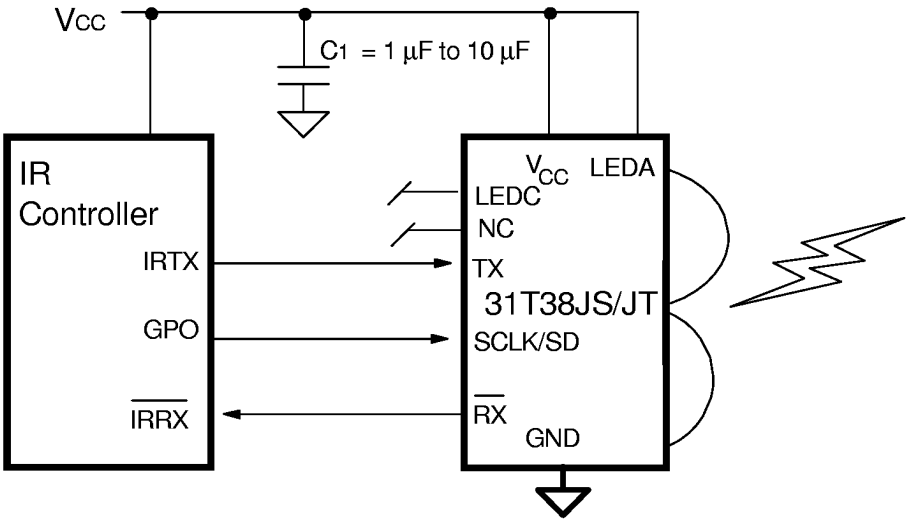
Ordering Information

Part Number	Order Quantity	Description	PCB Mounting Orientation
IBM31T38JS	1000/Reel	3V Integrated Transceiver - Side View	Packaged in Component Carrier Reel for Side-View Mounting on PCB
IBM31T38JT	1000/Reel	3V Integrated Transceiver - Top View	Packaged in Component Carrier Reel for Top-View Mounting on PCB

Block Diagram



Minimum IBM Low-Power Integrated Infrared Transceiver Circuit Diagram



Absolute Maximum Ratings

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{CC}	Supply Voltage	-0.5		5.5	V	
PD	Power Dissipation			745	mW	
T_J	Junction Temp.			125	°C	
T_{STG}	Storage Temp.	-25		85	°C	
T_{SOLDER}	Soldering Temp.			240	°C	See “Reflow Soldering” section in Application Notes
I_{LED}	LED Current (Peak)			710	mA	$t_{on} \leq 25\%$
	Any pin voltage	-0.5		Vcc+0.5	V	

Recommended Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{CC}	Supply Voltage	2.7		5.25	V	
T_A	Ambient Operating Temperature	-25		75	°C	

DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
I_{CC}	Supply Current; Listening		2.2	3.25	mA	Typical value obtained at Vcc=3.3V
I_{CC}	Supply Current; Receiving		7	27	mA	Interface and optical input power dependent
I_{SD}	Supply Current; Shutdown			50	nA	$V_{SD}=V_{CC}$

Receiver DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{OL}	$\overline{RX}$ Output Low Voltage			0.5	V	
I_{OL}	Static Sink Current on $\overline{RX}$			2.4	mA	2.2KΩ load.
V_{OH}	$\overline{RX}$ Output High Voltage	V_{CC}-0.5			V	
I_{OH}	Static Source Current on $\overline{RX}$			2.4	mA	2.2KΩ load.
R_L	$\overline{RX}$ Resistive Load	2.2			kΩ	
C_L	$\overline{RX}$ Capacitive Load			50	pF	

Transmitter DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IL}	TX Input Voltage Low			0.8	V	
V_{IH}	TX Input Voltage High	2.4			V	
C_i	Input Capacitance			5	pF	

SCLK/SD DC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
V_{IL}	SCLK/SD Input Voltage Low			0.8	V	
V_{IH}	SCLK/SD Input Voltage High	2.4			V	
C_i	Input Capacitance			5	pF	

Optical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
E_{min}	Minimum Detection Irradiance 9.6-115.2 kbit/s, SIR		2	4	$\mu W/cm^2$	9.6 kbit/s to 115.2 kbit/s
E_{min}	Minimum Detection Irradiance 1.152Mbit/s, MIR		2.5	4	$\mu W/cm^2$	1.152 Mbit/s
E_{min}	Minimum Detection Irradiance 4 Mbit/s, FIR		7	8	$\mu W/cm^2$	4 Mbit/s
t_r, t_f	LED Optical Rise/Fall Time			40	ns	
t_{xpw}	SIR Optical Pulse Width	1.41		22.13	µs	TX Input Pulse Width = 3/16 duty cycle
t_{xpw}	MIR Optical Pulse Width	147		261	ns	TX Input Pulse Width = 217ns
t_{xpw}	FIR Optical Pulse Width	115		135	ns	TX Input Pulse Width = 125ns
I_e	Output Radiant Intensity	100	200	325	mW/sr	TX Pulsed High @ 2MHz and 25%, SCLK/SD=Low, V_{CC}=3.3 V, α=0°, $\alpha = \pm 15°$, T_A=25°C
α	Output Radiant Half Intensity Angle	±15			°	
λ_p	Peak Wavelength	850	870	900	nm	
	Optical Overshoot			10	%	

AC Electrical Characteristics

Symbol	Parameter	Min	Typical	Max	Unit	Conditions
t_r	$\overline{RX}$ Rise Time			60	ns	
t_f	$\overline{RX}$ Fall Time			50	ns	
t_{SU},t_H	TX Setup and Hold to SCLK/SD Falling Edge	20			ns	For legacy programming
t_{SU},t_H	TX Setup and Hold to SCLK/SD Rising Edge	20			ns	For serial interface programming
t_w	$\overline{RX}$ Pulse Width (SIR)	1.0		2.1	µs	57.6kHz@3/32 duty cycle
t_w	$\overline{RX}$ Pulse Width (1.152Mbit/s)	100		600	ns	576kHz@12.5% duty cycle
t_w	$\overline{RX}$ Pulse Width (4Mbit/s, single pulse)	80		165	ns	2MHz@25% duty cycle
t_w	$\overline{RX}$ Pulse Width (4Mbit/s, double pulse)	210		290	ns	1MHz@25% duty cycle
t_L	Receiver Latency			100	µs	
t_{RXEN}	$\overline{RX}$ Valid After Shutdown			200	µs	
t_{LEDP}	LED Protection Time-out			100	µs	
I_{LED}	Peak Transmit Current	10		710	mA	25% duty cycle, LED power setting dependent
I_{LED}	Average Transmit Current	5		150	mA	25% duty cycle, LED power setting dependent

Note: $\overline{RX}$ pulse widths measured with respective data rate's average duty cycle from 0cm distance to minimum IrDA spectral irradiance limit. All $\overline{RX}$ measurements are done with R_L=2.2 KΩ, C_L=50 pF.

Timing Diagrams

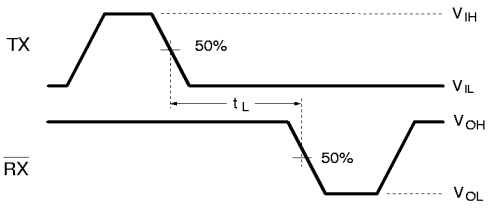


Figure 1. Latency Timing

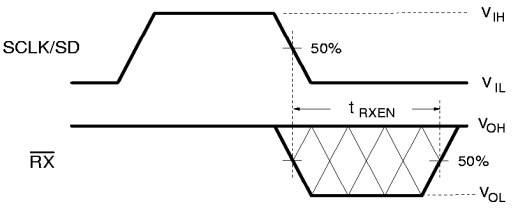


Figure 2. $\overline{RX}$ Valid after Shutdown

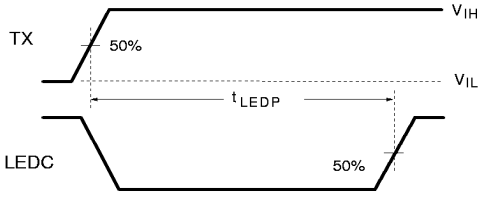


Figure 3. LED Protection Timing

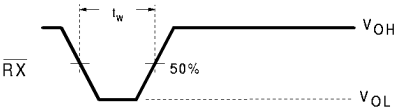


Figure 4. $\overline{RX}$ Timing 1.2 and 4 Mbit/s Mode

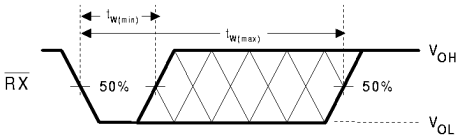


Figure 5. $\overline{RX}$ Timing, SIR mode. The output may be indeterminate in the shaded area. Spurious transitions may occur.

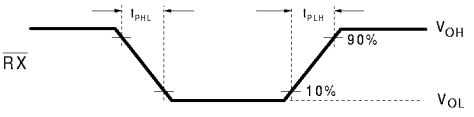


Figure 6. $\overline{RX}$ Rise and Fall Timing Measurements

Bandwidth Programming (Legacy Mode)

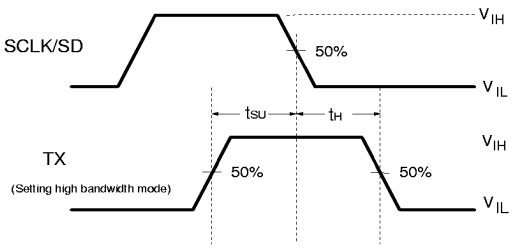


Figure 7. Setting the Receiver to High BW Mode

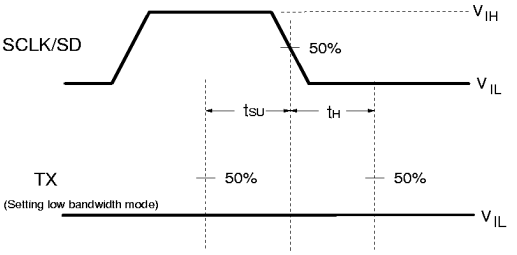


Figure 8. Setting the Receiver to Low BW Mode

The transceiver powers on with the receiver in low bandwidth mode. To enable high bandwidth mode, apply timings as shown in the figure 7, to the SCLK/SD and the TX inputs. Note that the internal LED driver is disabled when SCLK/SD is active and is not enabled until the next rising edge of TX. This ensures that the LED will not be active during bandwidth adjustment. It is recommended that the SCLK/SD pin be connected to GND if bandwidth adjustment, shutdown mode and serial programming are not used.

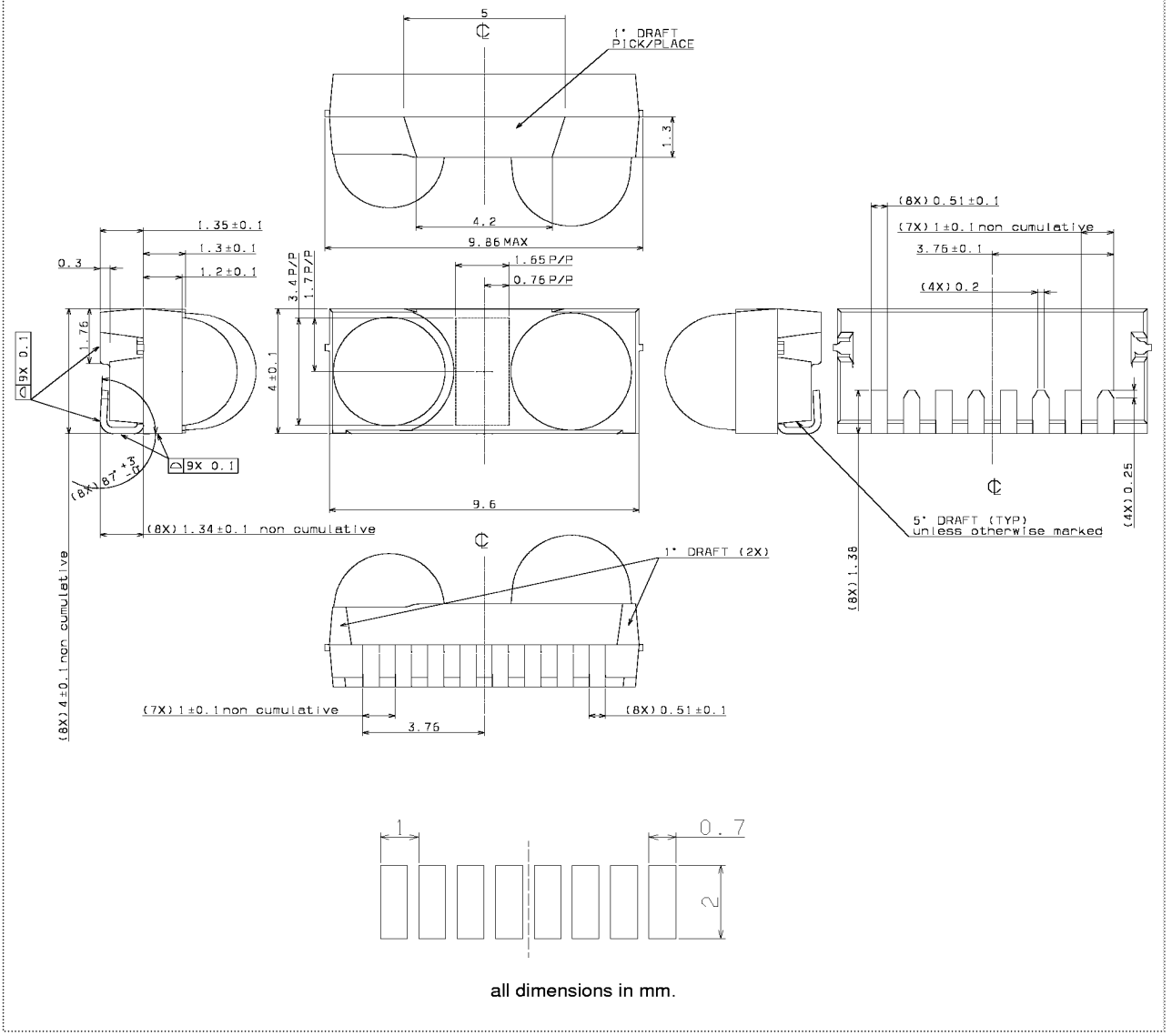
Setting the Receiver to High Bandwidth Mode (see Figure 7)

1. Set the SCLK/SD input to 'logic high'.
2. Set the TX input to 'logic high'. Wait $t_{su} \geq 20$ ns.
3. Set the SCLK/SD to 'logic low'. (This high-to-low transition latches the state of TX, which determines the receiver bandwidth.)
4. After waiting $t_h \geq 20$ ns, set the TX input to 'logic low'. The receiver is in high bandwidth mode within 400 µs of the SCLK/SD rising edge or 20 ns after the SCLK/SD falling edge, whichever occurs later.

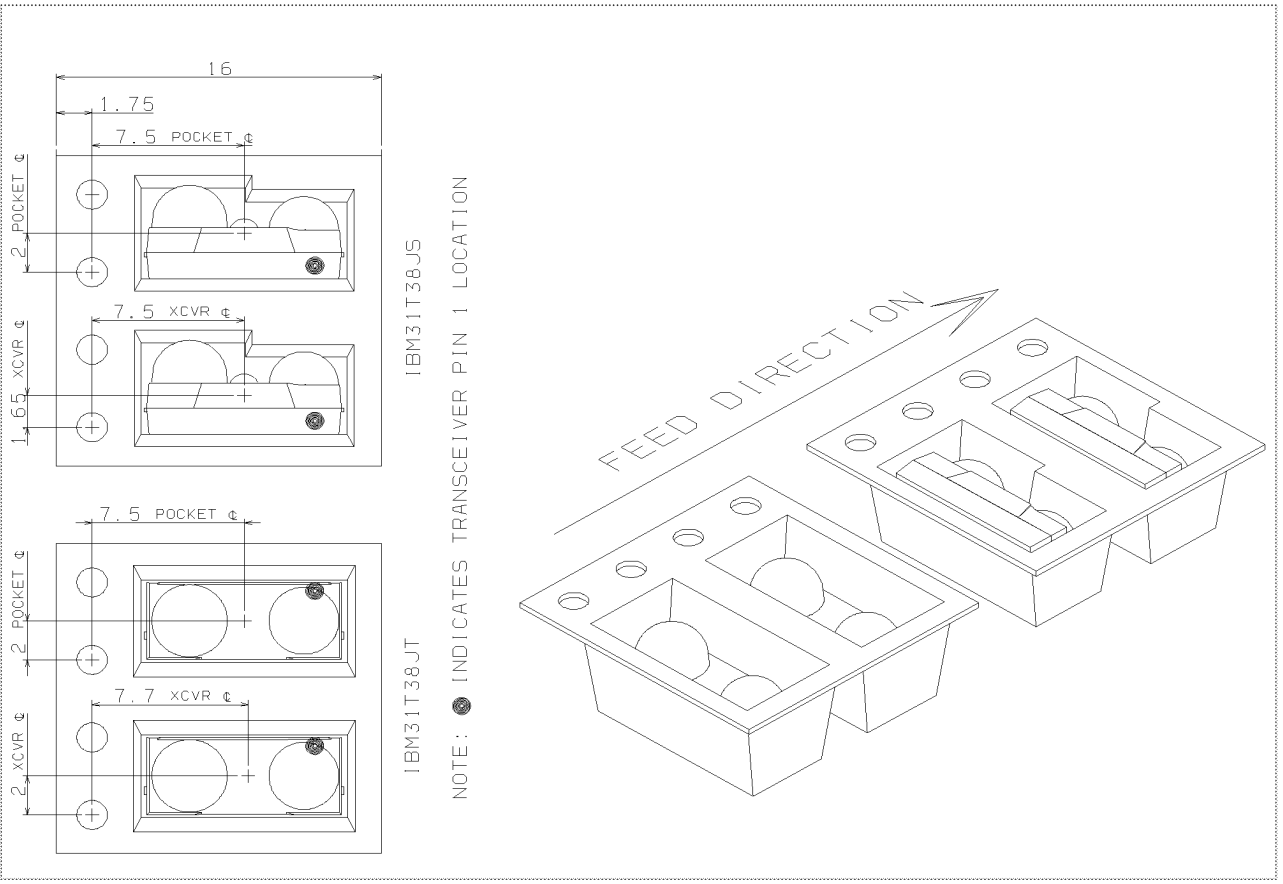
Setting the Receiver to Low Bandwidth Mode (see Figure 8)

1. Set the SCLK/SD input to 'logic high'.
2. Ensure that the TX input is at 'logic low'. Wait $t_{su} \geq 20$ ns.
3. Set the SCLK/SD to 'logic low'. (This high-to-low transition latches the state of TX, which determines the receiver bandwidth.)
4. Ensure that the TX input remains low for $t_h \geq 20$ ns. The receiver is in low bandwidth mode within 400 µs of the SCLK/SD rising edge or 20 ns after the SCLK/SD falling edge, whichever occurs later.

Package Diagram and PCB Pad Placement



Tape and Reel Diagram



Revision Log

Revision	Date	Contents of Modification
00	06/01/98	Initial release.
01	06/24/98	Correction of $\overline{RX}$ pulse width at 9.6 kbit/s.
02	08/28/98	PCB Pad Placement drawing update, Layout update, added 'Tape and Reel' diagram.
03	02/25/99	Post qualification refresh: operating supply voltage range increased and significant updates to optical and electrical characteristics.
04	03/05/99	Clarified instructions for setting receiver bandwidth mode; Min V_{IH} for TX and SCLK/SD pins changed to 2.4V.