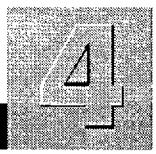

4.0 ELECTRICAL SPECIFICATIONS

4.1 Electrical Connections

This section provides information on electrical connections, absolute maximum ratings, recommended operating conditions, DC characteristics, and AC characteristics. All voltage values in Electrical Specifications are measured with respect to V_{SS} unless otherwise noted.

4.1.1 Power and Ground Connections and Decoupling

Testing and operating the IBM 6x86 CPU requires the use of standard high frequency techniques to reduce parasitic effects. The high clock frequencies used in the IBM 6x86 CPU and its output buffer circuits can cause transient power surges when several output buffers switch output levels simultaneously. These effects can be minimized by filtering the DC power leads with low-inductance decoupling capacitors, using low impedance wiring, and by utilizing all of the V_{CC} and GND pins. The IBM 6x86 CPU contains 296 pins with 53 pins connected to V_{CC} and 53 connected to V_{SS} (ground).

4.1.2 Pull-Up/Pull-Down Resistors

Table 4-1 lists the input pins that are internally connected to pull-up and pull-down resistors. The pull-up resistors are connected to V_{CC} and the pull-down resistors are connected to V_{SS}. When unused, these inputs do not require connection to external pull-up or pull-down resistors. The SUSP# pin is unique in that it is connected to a pull-up resistor only when SUSP# is not asserted.

Table 4-1. Pins Connected to Internal Pull-Up and Pull-Down Resistors

SIGNAL	PIN NO.	RESISTOR
BRDYC#	Y3	20-kΩ pull-up
CLKMUL	Y33	20-kΩ pull-down
QDUMP#	AL7	20-kΩ pull-up
SMI#	AB34	
SUSP#	V34	20-kΩ pull-up (see text)
TCK	M34	20-kΩ pull-up
TDI	N35	
TMS	P34	
TRST#	Q33	
Reserved	J33	
Reserved	W35	
Reserved	Y35	
Reserved	AN35	20-kΩ pull-down

4.1.3 Unused Input Pins

All inputs not used by the system designer and not listed in Table 4-1 should be connected either to ground or to V_{CC}. Connect active-high inputs to ground through a 20 kΩ (± 10%) pull-down resistor and active-low inputs to V_{CC} through a 20 kΩ (± 10%) pull-up resistor to prevent possible spurious operation.

4.1.4 NC and Reserved Pins

Pins designated NC have no internal connections. Pins designated RESV or RESERVED should be left disconnected. Connecting a reserved pin to a pull-up resistor, pull-down resistor, or an active signal could cause unexpected results and possible circuit malfunctions.

4.2 Absolute Maximum Ratings

The following table lists absolute maximum ratings for the IBM 6x86 CPU microprocessors. Stresses beyond those listed under Table 4-2 limits may cause permanent damage to the device. These are stress ratings only and do not imply that operation under any conditions other than those listed under "Recommended Operating Conditions" Table 4-3 (Page 4-3) is possible. Exposure to conditions beyond Table 4-2 may (1) reduce device reliability and (2) result in premature failure even when there is no immediately apparent sign of failure. Prolonged exposure to conditions at or near the absolute maximum ratings may also result in reduced useful life and reliability.

Table 4-2. Absolute Maximum Ratings

PARAMETER	MIN	MAX	UNITS	NOTES
Storage Temperature	-65	150	°C	
Supply Voltage, V_{CC}	-0.5	4.0	V	
Voltage On Any Pin	-0.5	V_{CC} +0.5	V	
Input Clamp Current, I_{IK}		10	mA	Power Applied
Output Clamp Current, I_{OK}		25	mA	Power Applied

4.3 Recommended Operating Conditions

Table 4-3 presents the recommended operating conditions for the IBM 6x86 CPU device.

Table 4-3. Recommended Operating Conditions

PARAMETER	MIN	MAX	UNITS	NOTES
T_C Operating Case Temperature	0	75	°C	Power Applied
V_{CC} =3.3Vnom, Supply Voltage	3.15	3.6	V	
V_{CC} =3.5Vnom, Supply Voltage	3.4	3.6	V	
V_{IH} High-Level Input Voltage	2.0	5.5	V	
V_{IL} Low-Level Input Voltage	-0.3	0.8	V	
I_{OH} High-Level Output Current All outputs except A20-A3 and W/R#		-1.0	mA	$V_O=V_{OH\ (MIN)}$
I_{OL} Low-Level Output Current All outputs except A20-A3 and W/R#		5.0	mA	$V_O=V_{OL\ (MAX)}$

4.4 DC Characteristic

Table 4-4. DC Characteristics (at Recommended Operating Conditions)

PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{OL} Output Low Voltage I_{OL} = 5 mA			0.4	V	
V_{OH} Output High Voltage I_{OH} = -1 mA	2.4			V	
I_I Input Leakage Current For all pins except those listed in Table 4-1.			±15	µA	$0 < V_{IN} < V_{CC}$
I_{IH} Input Leakage Current For all pins with internal pull-downs.			200	µA	V_{IH} = 2.4 V See Table 4-1.
I_{IL} Input Leakage Current For all pins with internal pull-ups.			-400	µA	V_{IL} = 0.45 V See Table 4-1.
I_{CC} 100 MHz		4500	5400	mA	Note 1, 5,6
110 MHz		4800	5800		
120 MHz		5100	6100		
133 MHz		5500	6600		
150 MHz		6000	7000		
I_{CCSM} (Suspend Mode I_{CC})					Note 1, 3, 5
100 MHz		48	80	mA	
110 MHz		50	83		
120 MHz		51	105		
133 MHz		54	115		
150 MHz		60	125		
I_{CCSS} Standby I_{CC} 0 MHz (Suspended/CLK Stopped)		35	55	mA	Note 4,5
C_{IN} Input Capacitance			15	pF	f = 1 MHz, Note 2
C_{OUT} Output Capacitance			20	pF	f = 1 MHz, Note 2
C_{IO} I/O Capacitance			25	pF	f = 1 MHz, Note 2
C_{CLK} CLK Capacitance			15	pF	f = 1 MHz, Note 2

Notes:
1. Frequency (MHz) ratings refer to the internal clock frequency.
2. Not 100% tested.
3. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static except clock and all outputs unloaded (static I_{OUT} = 0 mA).
4. All inputs at 0.4 or V_{CC} - 0.4 (CMOS levels). All inputs held static and all outputs unloaded (static I_{OUT} = 0 mA).
5. Typical, measured at V_{CC} = 3.3 V
6. Max, measured at Vcc=3.6V. Lab Testing on some devices has produced Max current draws of:
   100MHz....6.05A
   110MHz....6.58A
   120MHz....6.95A
   133MHz....7.50A
   150MHz....7.11A

4.5 AC Characteristics

Tables 4-6 through 4-11 (Pages 4-7 through 4-13) list the AC characteristics including output delays, input setup requirements, input hold requirements and output float delays. These measurements are based on the measurement points identified in Figure 4-1 (Page 4-6) and Figure 4-1 (Page 4-6). The rising clock edge reference level V_{REF} and other reference levels are shown in Table 4-5. Input or output signals must cross these levels during testing.

Figure 4-1 shows output delay (A and B) and input setup and hold times (C and D). Input setup and hold times (C and D) are specified minimums, defining the smallest acceptable sampling window a synchronous input signal must be stable for correct operation.

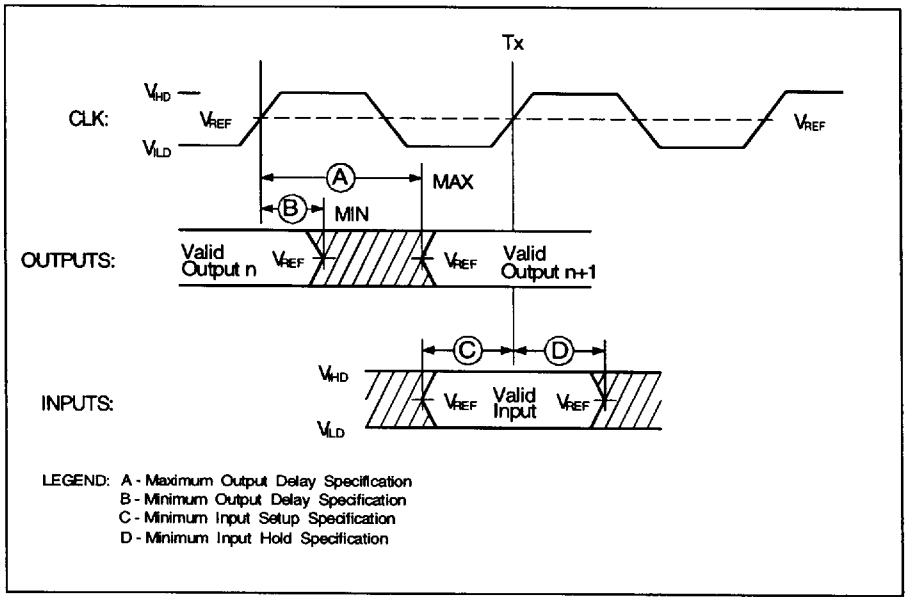

Figure 4-1. Drive Level and Measurement Points for Switching Characterics.

Table 4-5. Drive Level and Measurement Points for Switching Characteristics

SYMBOL	VOLTAGE (Volts)
V_{REF}	1.5
V_{IHD}	2.3
V_{ILD}	0

Note: Refer to Figure 4-1.

Table 4-6. Clock Specifications
T_{CASE} = 0°C to 75°C, See Figure 4-2

SYMBOL	PARAMETER	50-MHz BUS		55-MHz BUS		60-MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	CLK Frequency		50.0		55.0		60.0	MHz
T1	CLK Period	20.0		18.0		16.67		ns
T2	CLK Period Stability		±250		±250		±250	ps
T3	CLK High Time	7.00		4.00		4.00		ns
T4	CLK Low Time	7.00		4.00		4.00		ns
T5	CLK Fall Time	0.15	2.00	0.15	1.50	0.15	1.50	ns
T6	CLK Rise Time	0.15	2.00	0.15	1.50	0.15	1.50	ns

SYMBOL	PARAMETER	66-MHz BUS		75-MHz BUS				UNITS
		MIN	MAX	MIN	MAX			
	CLK Frequency		66.6		75.0			MHz
T1	CLK Period	15.0		13.3				ns
T2	CLK Period Stability		±250		±250			ps
T3	CLK High Time	4.00		4.00				ns
T4	CLK Low Time	4.00		4.00				ns
T5	CLK Fall Time	0.15	1.50	0.15	1.50			ns
T6	CLK Rise Time	0.15	1.50	0.15	1.50			ns

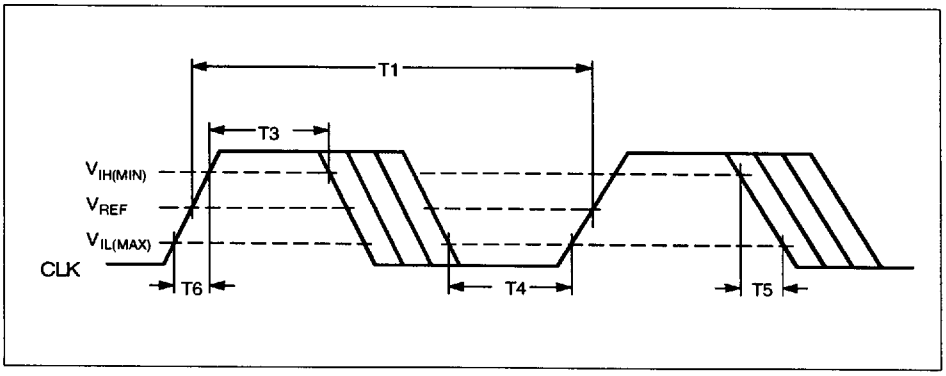

Figure 4-2. CLK Timing and Measurement Points

Table 4-7. Output Valid Delays
CL=50 pF, TCASE =0°C to 75°C, See Figure 4-3

SYMBOL	PARAMETER	50MHz BUS		55MHz BUS		60-MHz BUS		66-MHz BUS		75MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T7a	A31-A3, ADS#, BE7#-BE0#, CACHE#, D/C#, LBA#, LOCK#, PCD, PWT, SCYC, SMIACT#, W/R#	3	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T7b	ADS#, M/IO#	3	12	1.0	7.0	1.0	7.0	1.0	6.0	1.0	6.0	ns
T8	ADSC#	3	12	1.0	7.0	1.0	7.0	1.0	7.0	1.0	7.0	ns
T9	AP	3	12	1.0	8.5	1.0	8.5	1.0	8.5	1.0	8.5	ns
T10	APCHK#, PCHK#, FERR#	3	14	1.0	8.3	1.0	7.0	1.0	7.0	1.0	7.0	ns
T11	D63-D0, DP7-DP0 (Write)	3	12	1.3	8.5	1.3	7.5	1.3	7.5	1.0	7.5	ns
T12a	HIT#	3	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T12b	HITM#,	3	12	1.1	6.0	1.1	6.0	1.1	6.0	1.0	6.0	ns
T13	BREQ, HLDA	3	12	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns
T14	SUSPA#	3	14	1.0	8.0	1.0	8.0	1.0	8.0	1.0	8.0	ns

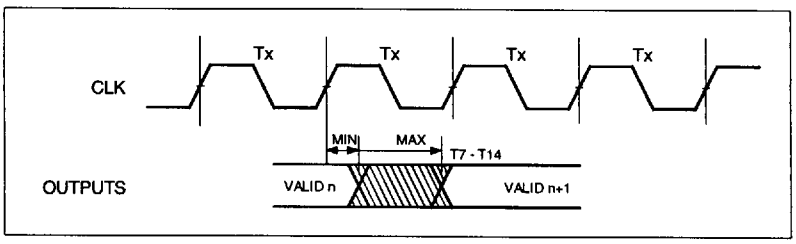

Figure 4-3. Output Valid Delay Timing.

Table 4-8. Output Float Delays
C_L = 50 pF, T_{case} = 0°C to 75°C, See Figure 4-5

SYMBOL	PARAMETER	50MHz BUS		55MHz BUS		60MHz BUS		66MHz BUS		75MHz BUS		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
T15	A31-A3, ADS#, BE7#-BE0#, BREQ, CACHE#, D/C#, LBA#, LOCK#, M/IO#, PCD, PWT, SCYC, SMIACT#, W/R#		16.0		10.0		10.0		10.0		10.0	ns
T16	AP		16.0		10.0		10.0		10.0		10.0	ns
T17	D63-D0, DP7-DP0 (Write)		16.0		10.0		10.0		10.0		10.0	ns

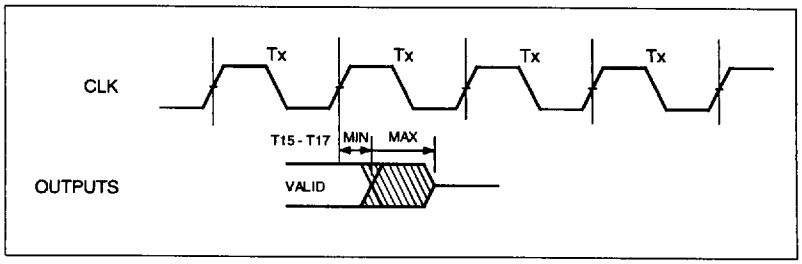

Figure 4-4. Output Float Delay Timing

Table 4-9. Input Setup Times
T_{case} = 0°C to 75°C, See Figure 4-5

SYMBOL	PARAMETER	50MHz BUS	55MHz BUS	60MHz BUS	66MHz BUS	75MHz BUS	UNITS
		MIN	MIN	MIN	MIN	MIN	
T18	A20M#, FLUSH#, IGNNE#, SUSP#	5	5	5	5	3.3	ns
T19	AHOLD, BHOLD, BOFF#, DHOLD, HOLD	5	5	5	5	3.3	ns
T20	BRDY#	5	5	5	5	3.3	ns
T21	BRDYC#	5	5	5	5	3.3	ns
T22a	A31-A3, BE7#-BE0#	4	5	5	5	3.3	ns
T22b	AP	4	5	5	5	4	ns
T22c	D63-D0 (Read), DP7-DP0 (Read)	4	3.8	3	3	3	ns
T23	EADS#, INV	5	5	5	5	3.3	ns
T24	INTR, NMI, RESET, SMI#, WM_RST	5	5	5	5	3.3	ns
T25	EWBE#, KEN#, NA#, WB/WT#	5	4.5	4.5	4.5	3.0	ns
T26	QDUMP#	5	5	5	5	3.3	ns

Table 4-10. Input Hold Times
T_{case} = 0°C to 75°C, See Figure 4-5

SYMBOL	PARAMETER	50MHz BUS	55MHz BUS	60MHz BUS	66MHz BUS	75MHz BUS	UNITS
		MIN	MIN	MIN	MIN	MIN	
T27	A20M#, FLUSH#, IGNNE#, SUSP#	2	1	1	1	1	ns
T28	AHOLD, BHOLD, BOFF#, DHOLD, HOLD	2	1	1	1	1	ns
T29	BRDY#	2	1	1	1	1	ns
T30	BRDYC#	2	1	1	1	1	ns
T31a	A31-A3, AP, BE7#-BE0#	2	1	1	1	1	ns
T31b	D63-D0(Read), DP7-DP0 (Read)	2	2	2	2	2	ns
T32	EADS#, INV	2	1	1	1	1	ns
T33	INTR, NMI, RESET, SMI#, WM_RST	2	1	1	1	1	ns
T34	EWBE#, KEN#, NA#, WB/WT#	2	1	1	1	1	ns
T35	QDUMP#	2	1	1	1	1	ns

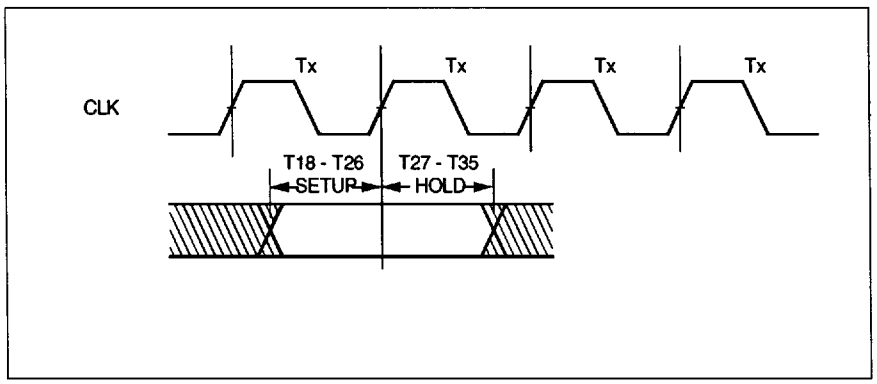

Figure 4-5. Input Setup and Hold Timing

Table 4-11. JTAG AC Specifications

SYMBOL	PARAMETER	ALL BUS FREQUENCIES		UNITS	FIGURE
		MIN	MAX		
	TCK Frequency (MHz)		20	MHz	
T36	TCK Period	50		MHz	4-6
T37	TCK High Time	25		MHz	4-6
T38	TCK Low Time	25		MHz	4-6
T39	TCK Rise Time		5	MHz	4-6
T40	TCK Fall Time		5	MHz	4-6
T41	TDO Valid Delay	3	20	MHz	4-7
T42	Non-test Outputs Valid Delay	3	20	MHz	4-7
T43	TDO Float Delay		25	MHz	4-7
T44	Non-test Outputs Float Delay		25	MHz	4-7
T45	TRST# Pulse Width	40		MHz	4-8
T46	TDI, TMS Setup Time	20		MHz	4-7
T47	Non-test Inputs Setup Time	20		MHz	4-7
T48	TDI, TMS Hold Time	13		MHz	4-7
T49	Non-test Inputs Hold Time	13		MHz	4-7

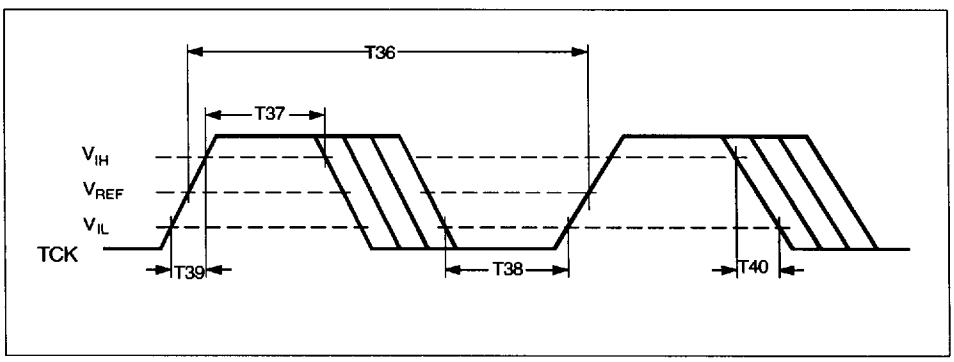

Figure 4-6. TCK Timing and Measurement Points

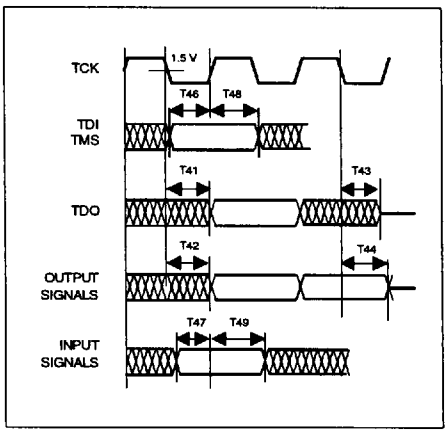

Figure 4-7. JTAG Test Timings

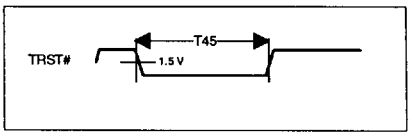

Figure 4-8. Test Reset Timing