ICD2023

PC Motherboard Clock Generator

Industry Standard Single-Chip Oscillator for 486/386/286 Personal Computer Motherboards

1

- 7 Independent Clock Outputs Handle all Clocking Requirements for Personal Computer Motherboards
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Programmable Frequency Range: 10 MHz – 80 MHz with 50% Duty Cycle
- Ideally Suited for PC Desktop and Laptop Computer Applications
- Sophisticated Internal Loop-Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- Battery Input Maintains 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Test Purposes
- 5V Operation
- Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

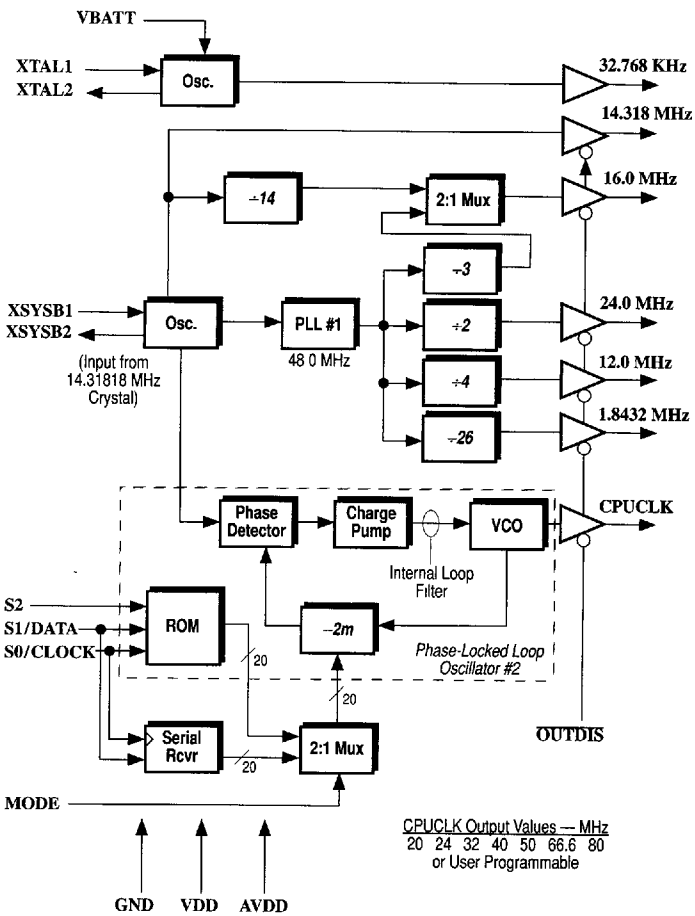

Fig. 1: ICD2023 Block Diagram

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Introduction

A modern personal computer motherboard often requires as many as six different crystal can oscillators. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of the oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2023 PC-AT Motherboard Clock Generator offers 2 oscillators, 2 phase-locked loops and 7 different outputs in a single package. Six of the outputs are of a fixed value while the seventh oscillator is fully user-programmable and may be changed "on the fly" to any desired frequency value between 10 MHz and 80 MHz. The ICD2023 is ideally suited for use in both existing designs (since it requires no support from the motherboard chip set and outputs 7 frequencies concurrently) and new designs which can utilize the programmable nature of this device.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

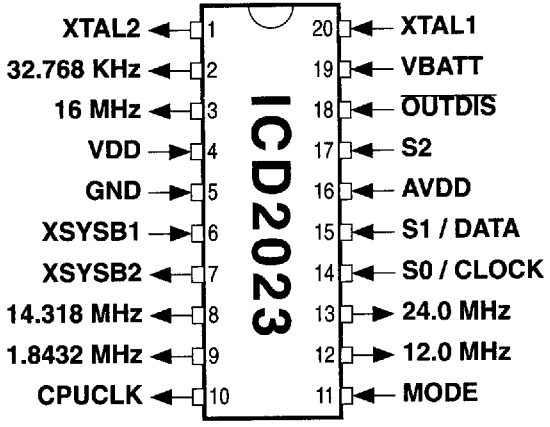

Table 1: Signal Descriptions

Pin #	Signal	Function
1	XTAL2	Oscillator Output to a 32.768 KHz Parallel-Resonant Crystal
2	32.768 KHz	32.768 KHz Output
3	16 MHz	16 MHz Output
4	VDD	+5V to I/O Ring
5	GND	Ground
6	XSYSB1	Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock Signal may be used as input if available.
7	XSYSB2	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)

Table 1: Signal Descriptions (Continued)

Pin #	Signal	Function
8	14.318 MHz	14.31818 MHz Output
9	1.8432 MHz	1.8432 MHz Output
10	CPUCLK	CPUCLK Programmable Oscillator Output (See *Table 3: CPUCLK Output with MODE = 1* on page 9)
11	MODE	MODE=0, CPUCLK is in programmable mode MODE=1, CPUCLK is in selection mode
12	12.0 MHz	12.0 MHz Output
13	24.0 MHz	24.0 MHz Output
14	S0 / CLOCK	MODE=0, S0 is serial clock input line for CPUCLK MODE=1, S0 is select line for CPUCLK (Internal pull-up)
15	S1 / DATA	MODE=0, S1 is serial data input line for CPUCLK MODE=1, S1 is select line for CPUCLK (Internal pull-up)
16	AVDD	+5 volts to Analog Core
17	S2	MODE=0 & S2=1: CPUCLK=(14.31818 MHz) reference frequency MODE=1, S2 is select line for CPUCLK (Internal pull-down)
18	$\overline{\text{OUTDIS}}$	Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up for no-connect if 3-state operation is not needed.)
19	VBATT	+5V for battery backup operation
20	XTAL1	Oscillator input from a 32.768 KHz crystal. For more information on crystal requirements, please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292.

General Considerations

Fixed Frequency Oscillator Operation

The following table describes each output:

Table 2: Fixed Frequency Oscillator Outputs

Output Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error	Notes
Real-Time Clock	32.768 KHz	32.768 KHz	0	Pass-through 32.768 KHz XTAL
System Bus	14.318	14.318	0	Pass-through 14.31818 MHz XTAL
Int. Bus Clock	16.000	15.983	1058	VCO = 47.94295 / 3
Keyboard Clock	12.000	11.987	1058	VCO = 47.94295 / 4
Floppy Disk Clock	24.000	23.975	1058	
Serial Port	1.843	1.844	543	

CPUCLK Programmable Oscillator: Selection Mode

CPUCLK is the programmable oscillator offering two modes of operation. The first mode uses three select lines to select one of 8 different preset frequencies, while the other mode allows the user to program any desired frequency between 10 MHz and 80 MHz. The two different modes are controlled by the MODE signal.

When MODE = 1, the selection lines can be changed to choose different frequencies. When this occurs, PLL #2 section will immediately seek the newly selected frequency as shown in the following table. During the transition period, the CPUCLK output will not glitch.

Table 3: CPUCLK Output with MODE = 1

S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error
0	0	0	20.000	20.0454	2272
0	0	1	24.000	23.9746	1058
0	1	0	32.000	32.0455	1422
0	1	1	40.000	40.0909	2272
1	0	0	50.000	49.9923	154
1	0	1	66.667	66.5962	57
1	1	0	80.000	80.1818	2272
1	1	1	100.000[a]	99.8182	1818

a. Duty cycle specs not guaranteed above 80 MHz

CPUCLK Programmable Oscillator: Serial Mode

When MODE = 0, CPUCLK enters its programmable mode. Signals S0 (clock) and S1 (data) become a serial interface, allowing a 20-bit number to be shifted in. The ICD2023 programmable oscillator (CPUCLK) requires a 20-bit programming word (W). This word contains 4 fields:

Table 4: Programming Word Bit Fields

Field	# of Bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter Value (Q')	6	LSB (Least Significant Bits)

If signal S2=1 and MODE=0, then the reference frequency (14.31818 MHz) is multiplexed to the CPUCLK output. This enables a glitch-free transition to the reference frequency while the VCO stabilizes.

The frequency of the programmable oscillator $f_{(VCO)}$ is determined by these fields as follows:

$$P' = P - 3 \qquad Q' = Q - 2$$

$$f_{(VCO)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

where $f_{(REF)}$ = Reference frequency = 14.31818 MHz.

The value of $f_{(VCO)}$ should be kept between 40 MHz and 80 MHz. Therefore, for output frequencies below 40 MHz, $f_{(VCO)}$ must be multiplied up into the required range. The mux bits allow a post-divide of the higher VCO to bring the output to those desired values below 40 MHz.

Table 5: Mux Bits M_0–M_1

M_1	M_0	Divisor
0	0	16
0	1	4
1	0	2
1	1	1

The M2 mux bit is used to select which one of the two Phase-Locked Loops is to be utilized in the CPUCLK output. Normally, the PLL #2 section (see *Fig. 1: ICD2023 Block Diagram* on page 3) is used. However, if the desired output frequency requires $f_{(VCO)}$ to be set to 48 MHz, then PLL #1 section should be used. This both reduces power consumption (since only one VCO is activated) and eliminates the possibility of jitter which can arise when 2 VCOs of the same frequency beat (heterodyne) against each other.

Table 6: Mux Bit M_2

M_2	CPUCLK
0	PLL #2
1	PLL #1 (48 MHz)

The Index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from the following table. (Note that this table is referenced to the VCO frequency $f_{(VCO)}$, rather than to the desired output frequency.)

Table 7: Index Field (I)

I	$f_{(VCO)}$ MHz
0001	40.0 – 47.5
0010	47.5 – 52.2
0011	52.2 – 56.3
0100	56.3 – 61.9
0101	61.9 – 65.0
0110	65.0 – 68.1
0111	68.1 – 80.0
1111	Turn off VCO

If the desired VCO frequency lies on a boundary in the table — in other words, if it is exactly the upper limit of one entry and the lower limit of the next — then either index value may be used (since both limits are tested), but we recommend using the higher one.

To assist with these calculations, IC DESIGNS provides ***BitCalc*** (Part #ICD/BCALC), a Windows™ program which automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers. For Macintosh or DOS environments, please ask about availability. Please specify disk size (5" or 3") when ordering ***BitCalc***.

Programming Constraints

There are five primary programming constraints the user must be aware of:

$$f_{(REF)} = 14.31818\,MHz$$

$$200KHz \le \frac{f_{(REF)}}{Q} \le 1MHz$$

$$40MHz \le f_{(VCO)} \le 80MHz$$

$$3 \le Q \le 65$$

$$4 \le P \le 130$$

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the ***BitCalc*** program all of these constraints become transparent.

ICD2023 Programming Example

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 40 MHz, double it to 79.0 MHz. Set M2, M1 and M0 to 0, 1 and 0, respectively. Set I to 0111. The result:

$$f_{(VCO)} = 79.0 = (2 \times 14.31818 \times \frac{P}{Q})$$

$$\frac{P}{Q} = 2.7857$$

Several choices of P and Q are available:

Table 8: Possible P & Q values

P	Q	$f_{(VCO)}$	Error (in ppm)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q) = (80,29) as this results in the best accuracy (40 ppm).

Therefore:

$$P' = P - 3 = 80 - 3 = 77 = 1001101 \quad (4dH)$$

$$Q' = Q - 2 = 29 - 2 = 27 = 011011 \quad (1bH)$$

and the full programming word, W, is:

$$W = I, P', M, Q' = 0111, 1001101, 010, 011011 = 01111001101010011011 \quad (79a9bH)$$

A low-to-high transition on S0 is used to shift the programming word W into S1 as a serial bit stream, LSB first. (See the set-up and hold timing specifications elsewhere in this datasheet.) If more than 20 shifts are performed, only the last 20 data bits received will be retained.

Output Frequency Accuracy

The accuracy of the ICD2023 output frequencies depends on the target output frequency. As stated previously, the output frequencies of the ICD2023 are an integral fraction of the input reference frequency:

$$f_{(OUT)} = (2 \times f_{(REF)} \times \frac{P}{Q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2023 normally produces an output frequency within 0.1% of the target frequencies listed. This is more than sufficient to meet standard motherboard requirements. Specifics regarding accuracy are available from the output of the ***BitCalc*** program.

3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state all the clock output lines (except 32.768 KHz). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2023.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1µF multi-layer ceramic capacitor and a 2.2µF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2023 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2023 closest to the device requiring the highest frequency. If the high-frequency clocks must be routed to board extremes, the ICD2031 distributed "satellite" oscillators should be considered.

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is 14.31818 MHz, and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements. Further, all the synthesis VCOs are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCOs and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be acceptable for motherboard designs.

Temperature and Process Sensitivity

Because of its feedback circuitry, the IC DESIGNS is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the IC DESIGNS, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

VBATT

The VBATT input powers the Real-Time Clock Oscillator (RTC). The backup power is typically supplied by a 3V lithium battery; however, any voltage between 2V and 5V is acceptable.

Crystal Operation

The following diagram details the proper way to hook up the two reference crystals. See the IC DESIGNS Application Note titled *Crystal Oscillator Topics* on page 292 for specifics regarding recommended crystals.

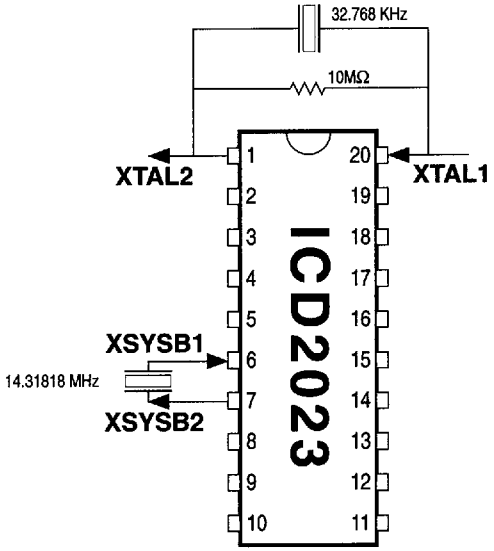

Fig. 3: Crystal Schematic

Ordering Information

Table 9: Order Codes

Part Number	Package Type	Temperature Range	Clock Output Options
ICD2023	S = 20-Pin SOIC	C = Commercial[a]	2 = CPUCLK ROM A, 16 MHz Output

a. 0°C to +70°C

Example: order ICD2023SC–2 for the ICD2023, 20–pin SOIC, commercial temperature range device which utilizes the CPUCLK ROM Option A table of frequency decodes and provides a 16 MHz output on pin 3. Custom CPUCLK ROM decodes are available by special order.

Device Specifications

Electrical Data

Table 10: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD} & AV_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		375	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} & AV_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

Table 11: DC Characteristics

Name	Description	Min	Max	Units	Conditions
V_{BATT}	Backup battery voltage	2.0	5.0	Volts	typ. = 3.0 Volts
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level CMOS output voltage	2.4		Volts	I_{OH} = –4.0 mA
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0 mA
I_{IH}	Input high current		150	µA	$V_{IH} = V_{DD} - 0.5V$
I_{IL}	Input low current		–250	µA	V_{IL} = 0.5V
I_{OZ}	Output leakage current		10	µA	(3-state)
I_{DD}	Power supply current	25	65	mA	
I_{DD-TYP}	Power supply current (typical)		40	mA	CPUCLK = 66 MHz
I_{BATT}	Backup battery current		50	µA	V_{BATT} = 3.0V
$I_{BATT-TYP}$	Backup battery current (typical)		8	µA	C_L = 10pF

Table 12: AC Characteristics

Symbol	Name	Description	Min	Typ	Max	Units
	CPUCLK	Reference Oscillator Output	10		80	MHz
t_1	ref freq	Reference Oscillator nominal value			14.318	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as $t_2 \div t_1$	40%		60%	
t_3	rise time	Rise time for the output oscillators into a 25pF load			3	ns
t_4	fall time	Fall time for the output oscillators into a 25pF load			3	ns
t_5	set-up	Delay required after MODE goes low prior to starting the S0 clock line			0	ns
t_6	cycle time	Minimum cycle time for the S0 clock	200			ns
t_7	set-up	Time required for the data to be valid prior to the rising edge of S0 / CLOCK	10			ns
t_8	hold	Time required for the data to remain valid after the rising edge of S0 / CLOCK	5			ns
t_9	clk unstable	Time CPUCLK oscillator remains valid after MODE signal goes low			0	ns
t_{10}	clk stable	Time required for the CPUCLK oscillator to become valid after last S0 clock			10	msec
t_{11}	clk unstable	Time the output oscillators remain valid after the S0, S1 or S2 select signals change value			0	ns
t_{12}	clk stable	Time required for the output oscillators to become valid after the S0, S1 or S2 select signals change value			10	msec
t_{13}	3-state	Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion			12	ns
t_{14}	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high			12	ns

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 4: Rise and Fall Times

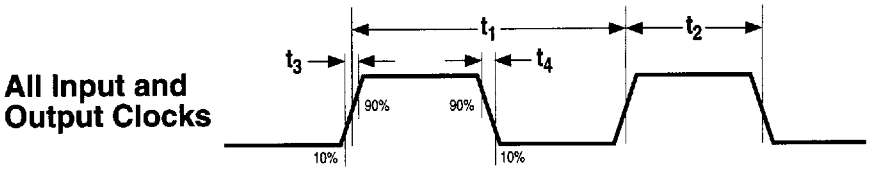

Fig. 5: Serial Programming Timing

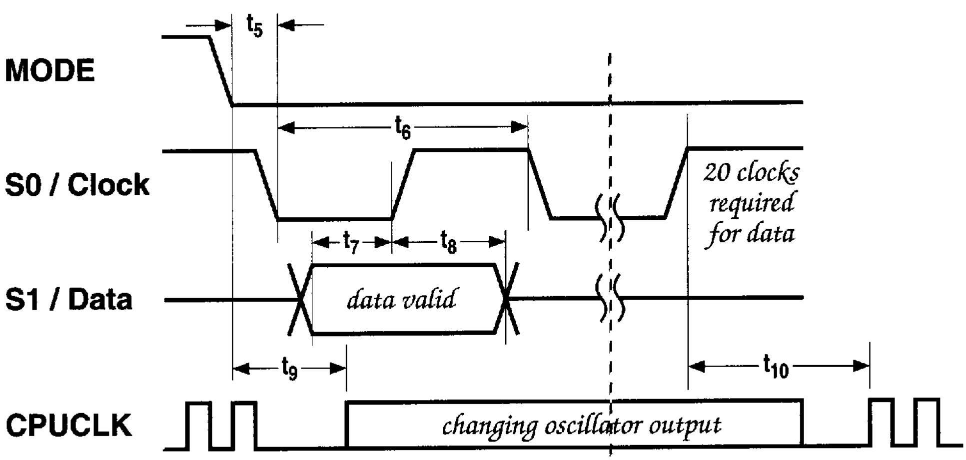

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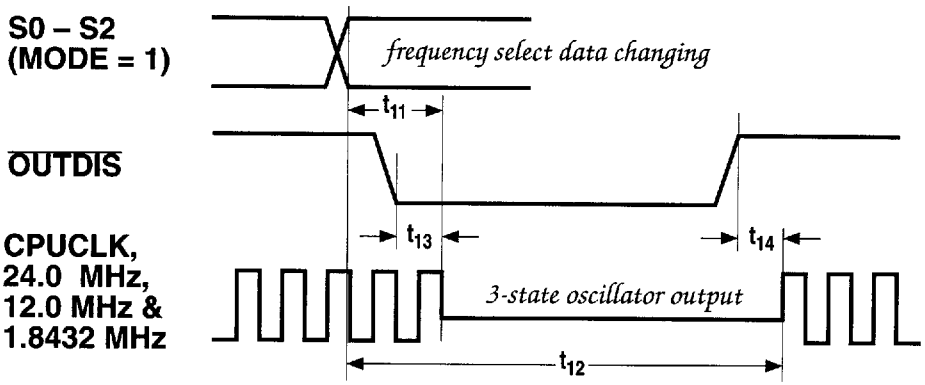
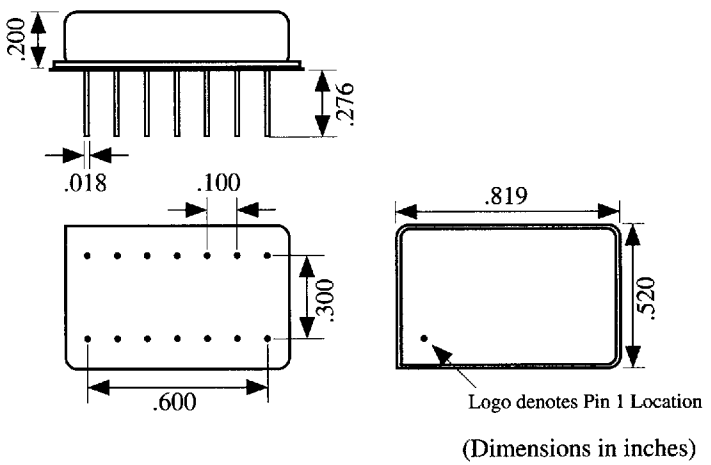
Fig. 6: 3-State Timing



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

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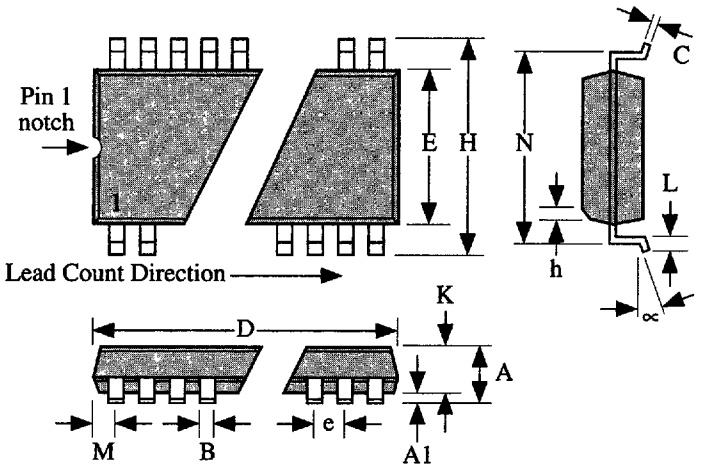
16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

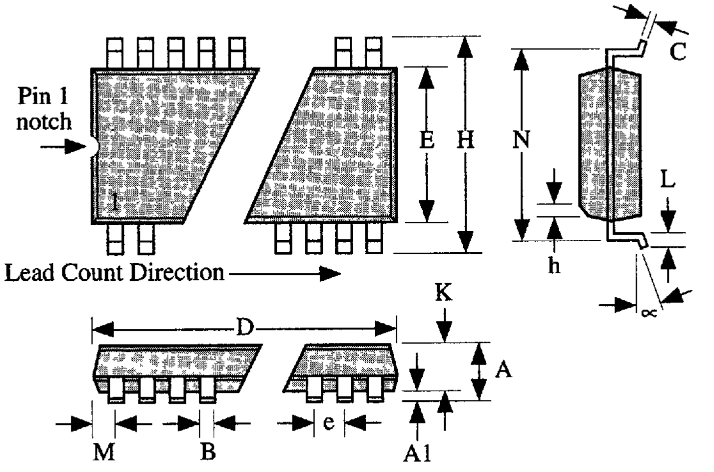


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)