ICD2027

PC Motherboard Clock Generator

Single-Chip Oscillator Ideally Suited for 486/386/286 Laptop/Notebook Computer Applications

1

- 6 Clock Outputs Handle all Clocking Requirements for Personal Computer Motherboards
- Phase-Locked Loop Oscillator Input Derived from Single 14.31818 MHz Crystal
- Frequency Range from 760 KHz – 100 MHz with 50% Duty Cycle
- 2 Power-Down Modes — Hardware Pin and Programmable Software Mode
- Concurrent and Low Skew ÷1 and ÷2 CPUCLK Outputs
- Ideally Suited for PC Desktop, Laptop and Notebook Computer Applications
- Battery Input Maintains 32.768 KHz Clock During Power-Down
- 3-State Oscillator Control Disables Outputs for Test Purposes
- Sophisticated Internal Loop-Filter Requires no External Components
- 5V, Low-Power, High-Speed CMOS Technology
- Available in 20-Pin SOIC Package Configuration

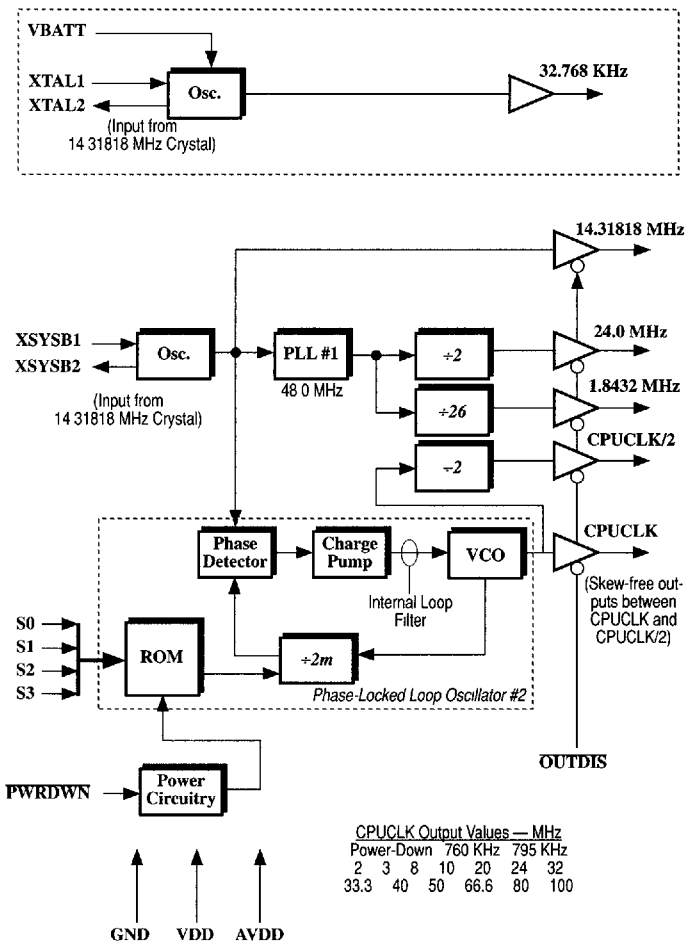

Fig. 1: ICD2027 Block Diagram

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Introduction

A modern personal computer motherboard often requires as many as six different crystal can oscillators per printed circuit board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of the oscillators required to build such multi-function motherboards. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2027 PC Motherboard Clock Generator offers 2 oscillators, 2 phase-locked loops, and 6 different outputs in a single package. Four of the outputs are of a fixed value while the other two may be changed "on the fly" to any one of 16 preset frequency values between 760 KHz and 100 MHz. The ICD2027 is ideally suited for use in new laptop/notebook designs due to its dual power-down modes. The ICD2027 also requires no support from the motherboard chip set and outputs all 6 frequencies concurrently.

Pin & Signal Descriptions

Fig. 2: Pin Descriptions

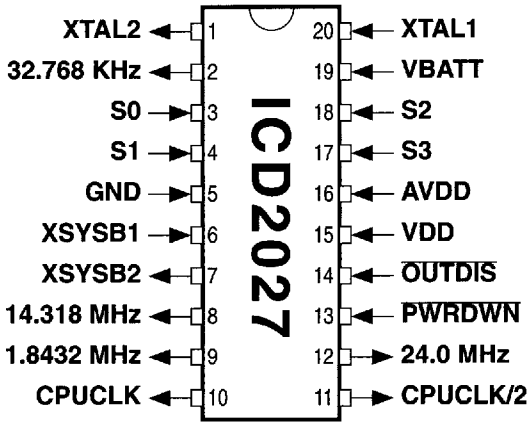


Table 1: Signal Descriptions

Pin #	Signal	Function
1	XTAL2	Oscillator Output to a 32.768 KHz Parallel-Resonant Crystal
2	32.768 KHz	32.768 KHz Output
3	S0	Bit 0 (LSB) of S0–S3, used to select CPUCLK frequency (Internal pull-down)
4	S1	Bit 1 of S0–S3, used to select CPUCLK frequency (Internal pull-down)
5	GND	Ground
6	XSYSB1	Input Reference Oscillator for all Phase-Locked Loops (nominally 14.31818 MHz). An optional PC System Bus Clock Signal may be used as input if available.
7	XSYSB2	Oscillator Output to a reference Series-Resonant Crystal. For higher accuracy, a Parallel-Resonant Crystal may be used. Assume CLOAD ≈ 17pF. For more specifics on crystal requirements please refer to the IC DESIGNS Application Note *Crystal Oscillator Topics* on page 292. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)

Table 1: Signal Descriptions

Pin #	Signal	Function
8	14.318 MHz	14.31818 MHz Output
9	1.8432 MHz	1.8432 MHz Output
10	CPUCLK	CPUCLK Programmable Oscillator Output (See *Table 2: CPUCLK ROM Selection Outputs* on page 44)
11	CPUCLK/2	Half the frequency of CPUCLK. Output is phase-coherent with the CPUCLK output.
12	24.0 MHz	24.0 MHz Output
13	$\overline{\text{PWRDWN}}$	Used to select Power Down mode when signal is pulled low (Pull-down)
14	$\overline{\text{OUTDIS}}$	Output Disable (3-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if 3-state operation not needed.)
15	VDD	+5V to I/O Ring
16	AVDD	+5V to Analog Core. See *Power Feed and Board Layout Issues* on page 281.
17	S3	Bit 3 (MSB) of S0–S3, used to select CPUCLK frequency (Internal pull-down)
18	S2	Bit 2 of S0–S3, used to select CPUCLK frequency (Internal pull-down)
19	VBATT	+2V to +5V used for battery backup operation.
20	XTAL1	Real-Time Clock Input Reference Oscillator (nominal 32.768 KHz).

General Considerations

CPUCLK Oscillator Operation

CPUCLK is the selectable oscillator. It uses 4 select lines to select 1 of 16 different preset frequencies. (Reference Frequency = 14.31818 MHz)

Table 2: CPUCLK ROM Selection Outputs

S3	S2	S1	S0	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error
0	0	0	0	0.7950[a]	$f_{(REF)}$ / 18	0
0	0	0	1	0.7950	$f_{(REF)}$ / 18	0
0	0	1	0	33.3000	33.2981	57
0	0	1	1	0.7600	0.7599	75
0	1	0	0	2.0000	2.0003	167
0	1	0	1	3.0000	2.9968	1057
0	1	1	0	8.0000	8.0013	167
0	1	1	1	10.0000	10.0227	2273
1	0	0	0	20.0000	20.0455	2273
1	0	0	1	24.0000	23.9747	1057
1	0	1	0	32.0000	32.0053	167
1	0	1	1	40.0000	40.0909	2273
1	1	0	0	50.0000	50.0000	0
1	1	0	1	66.6000	66.5962	57
1	1	1	0	80.0000	80.1818	2273
1	1	1	1	100.0000	99.8182	1818

a. Soft Power-Down Mode

NOTE: The select lines have internal pull-downs so that in a system power-down situation, the power-down mode is chosen in the CPUCLK table as the default. Therefore, upon power-up, one of the select lines must be pulled high.

Fixed Frequency Oscillator Operation

The following table describes each output:

Table 3: Fixed Frequency Oscillators

Output Clock Function	Desired Freq. (MHz)	Actual Freq. (MHz)	PPM Error	Notes
Real-Time Clock	32.768 KHz	32.768 KHz	0	Pass-through 32.768 KHz XTAL
System Bus	14.31818	14.31818	0	Pass-through 14.31818 MHz XTAL
Floppy Disk Clock	24.00000	23.97470	1058	
Serial Port	1.84320	1.84420	1058	

Power-Down Operation

There are two power-down modes within the ICD2027. The first is the hardware mode. When Pin 13 is pulled low ($\overline{PWRDWN}$ = 0), the part is immediately forced into its lowest power mode. This shuts down everything but the 32.768 KHz oscillator and its output. All power is now supplied by the VBATT input. For minimum power consumption in power-down mode, all select lines should be set low and $\overline{OUTDIS}$ should be set high.

The second mode is a programmable soft power-down mode. This mode shuts down the two phase-locked loops and all outputs except for the CPUCLK output, which runs at 795 KHz — a frequency sufficient to refresh dynamic RAMs.

Table 4: Soft Power-Down Mode (S0–S3 = 0000)

Output Signal	Status
32.768 KHz	32.768 KHz
CPUCLK	795.00 KHz
CPUCLK/2	(shutdown)
14.318 MHz	(shutdown)
1.8432 MHz	(shutdown)
24.000 MHz	(shutdown)

3-State Output Operation

The $\overline{\text{OUTDIS}}$ signal, when pulled low, will 3-state all the clock output lines (except 32.768 KHz). This supports wired-or connections between external clock lines, and allows for procedures such as automated testing where the clock must be disabled. The $\overline{\text{OUTDIS}}$ signal contains an internal pull-up; it can be left unconnected if 3-state operation is not required.

Skew-Free ÷2 on CPUCLK/2

The CPUCLK/2 output is available concurrently as a ÷2 of the desired CPUCLK output. The ÷2 output is also closely matched in order to minimize the phase differences between the two outputs. Typical phase coherence is less than 1 ns of skew between the two outputs, with 2 ns guaranteed worst case.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at frequencies above 50 MHz. When designing with this device, it is best to locate the ICD2027 closest to the device requiring the highest frequency.

A full power and ground plane layout should be employed both under and around the IC package. The analog power pin (AVDD) should be bypassed to ground with a 0.1μF multi-layer ceramic capacitor and a 2.2μF/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22Ω resistor placed between the power supply and the AVDD pin can help to filter noisy supply lines. Refer to IC DESIGNS Application Notes *Power Feed and Board Layout Issues* on page 281 and *Minimizing Radio Frequency Emissions* on page 285 for more details and for illustrative schematics.

The designer should also avoid routing any of the output traces of the ICD2027 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency of 14.31818 MHz goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output fre-

quency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

VBATT

The VBATT input powers the Real-Time Clock Oscillator (RTC). The backup power is typically a 3V lithium battery; however, any voltage between +2V and +5V is acceptable.

Crystal Operation

The following diagram details the proper way to hook up the two reference crystals. See the IC DESIGNS Application Note titled *Crystal Oscillator Topics* on page 292 for specifics regarding recommended crystals.

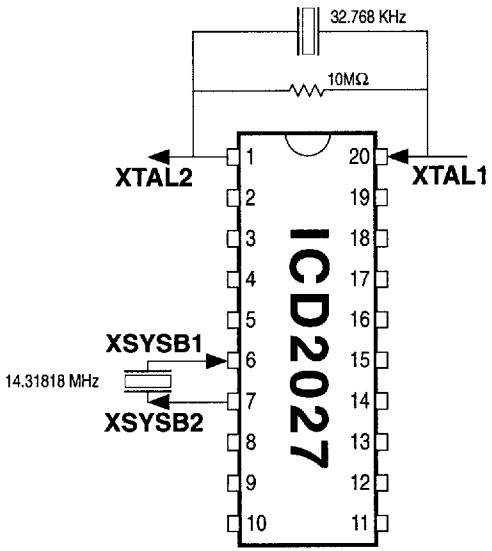


Fig. 3: Crystal Schematic

Ordering Information

Table 5: Order Codes

Part Number	Package Type	Temperature Range	CPUCLK ROM Option
ICD2027	S = 20-Pin SOIC DIP	C = Commercial[a]	1

a. 0°C to +70°C

Example: order ICD2027SC–1 for the ICD2027, 20-pin plastic SOIC, commercial temperature range device which uses the standard CPUCLK ROM Option 1 table of frequency decodes. Custom CPUCLK ROM decodes are available by special order.

Device Specifications

Electrical Data

Table 6: Absolute Maximum Ratings

Name	Description	Min	Max	Units
V_{DD} & AV_{DD}	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input voltage with respect to GND	–0.5	V_{DD} + 0.5	Volts
T_{STOR}	Storage temperature	–65	+150	°C
T_{SOL}	Max soldering temperature (10 sec)		+260	°C
T_J	Junction temperature		+125	°C
P_{DISS}	Power dissipation		375	mWatts

NOTE: Above the Maximum Ratings, the useful life may be impaired. For user guidelines, not tested.

OPERATING RANGE: V_{DD} & AV_{DD} = +5V ±5%; 0°C ≤ $T_{AMBIENT}$ ≤ 70°C
(This applies to all specifications below.)

Table 7: DC Characteristics

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level CMOS output voltage	2.4		Volts	I_{OH} = –4.0 mA
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0 mA
V_{BATT}	Backup battery voltage	2.0	5.0	Volts	
I_{IH}	Input high current		150	µA	V_{IH} = 5.25V
I_{IL}	Input low current		–250	µA	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µA	(3-state)
I_{DD}	Power supply current	25	65	mA	
I_{DD-PD}	Soft power-down current		7.5	mA	
I_{BATT}	Backup battery current		15	µA	typ. = 5 µA

Table 8: AC Characteristics

Symbol	Name	Description	Min	Typ	Max	Units
t_1	ref freq	Reference Oscillator nominal value			14.318	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as $t_2 \div t_1$	40%		60%	
t_3	rise time	Rise time for the output oscillators into a 25pF load			3	ns
t_4	fall time	Fall time for the output oscillators into a 25pF load			3	ns
t_5	3-state	Time for the output oscillators to go into 3-state mode after $\overline{\text{OUTDIS}}$ signal assertion			12	ns
t_6	clk valid	Time for the output oscillators to recover from 3-state mode after $\overline{\text{OUTDIS}}$ signal goes high			12	ns
t_7	CPUCLK/2 skew	Skew delay between the CPUCLK and the CPUCLK/2 outputs		1	2	ns
$t_{(REF)}$	reference period	$1 \div f_{(REF)}$		69.8		ns
t_{freq1}	freq1 output	Old frequency output				
t_{freq2}	freq2 output	New frequency output				
t_A	$f_{(REF)}$ mux time	Time clock output remains high while output muxes to reference frequency	$\frac{t_{(REF)}}{2}$		$3\frac{t_{(REF)}}{2}$	ns
t_B	t_{freq2} mux time	Time clock output remains high while output muxes to new frequency value	$\frac{t_{freq2}}{2}$		$3\frac{t_{freq2}}{2}$	ns
t_{MUXREF}		Time for VCO to settle between changes		6.2		msec

NOTE: Input capacitance is typically 10pF, except for the crystal pads.

Timing Diagrams

Fig. 4: Rise and Fall Times

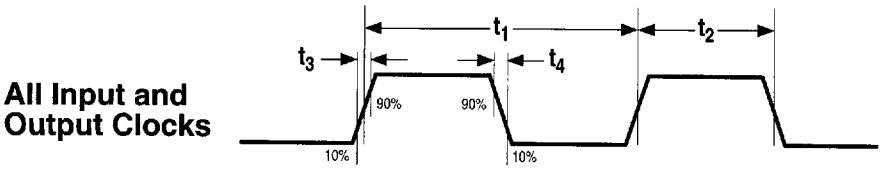


Fig. 5: 3-StateTiming

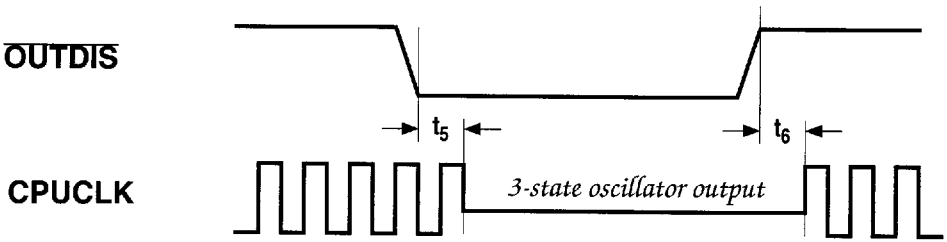


Fig. 6: CPUCLK Skew

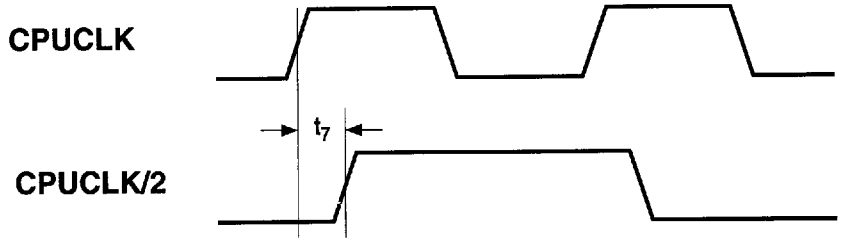
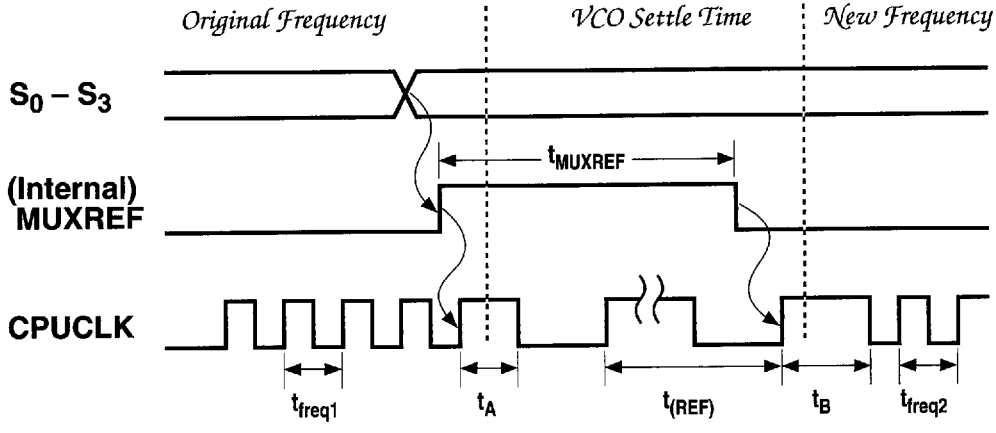


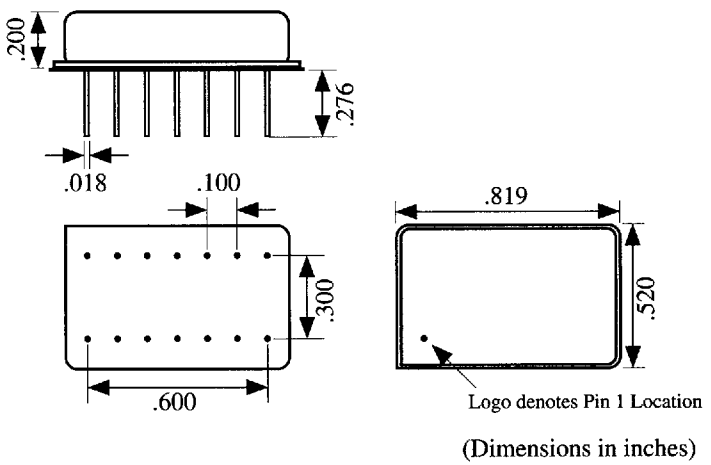
Fig. 7: Selection Timing



14-Pin Packages

Table 1: 14-Pin Metal Can Outline

Package (Lead Count = 14)



(Dimensions in inches)

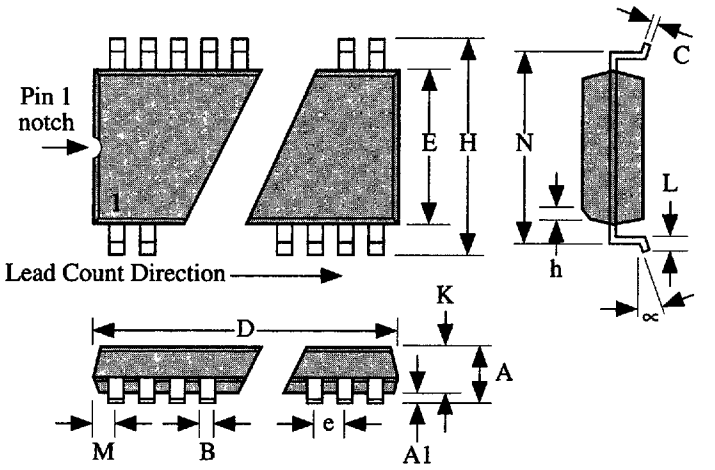
8

16-Pin Packages

Table 2: 16-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 16)

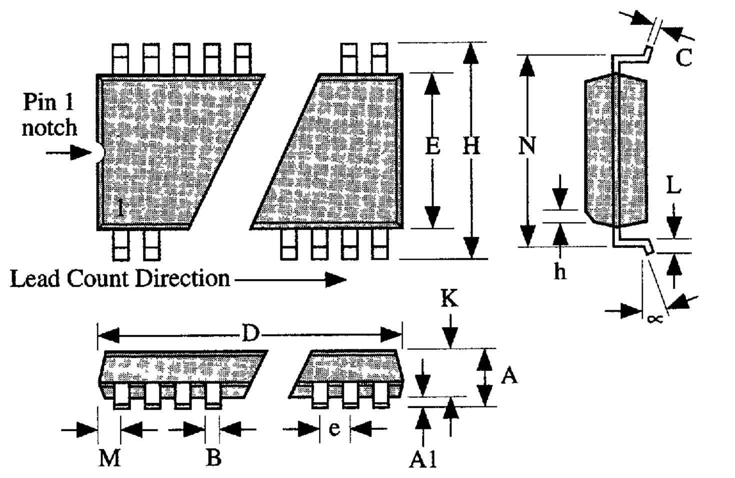


20-Pin Packages

Table 3: 20-Pin SOIC Outline

Symbol	MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.505	.512
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

Package (Lead Count = 20)



(Dimensions in inches)