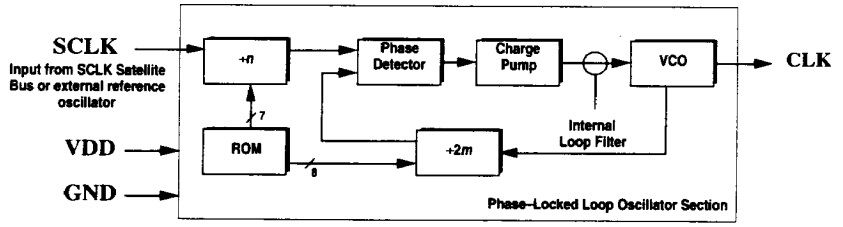
ICD2031A

Satellite Oscillator

Fixed-Frequency Oscillator Replaces Traditional Can Oscillators in Distributed High-Performance System Designs

- **Single Fixed-Frequency Oscillators Ranging from 1 MHz – 87 MHz with 50% Duty Cycle**
- **Generates Synthesized High-Frequency from Low-Frequency "SCLK" 1.0 MHz Reference Clock**
- **"Point-of-Use" Concept Reduces Overall System EMI/RFI Emissions for a Noise-Free High-Frequency Environment**
- **Distributed Synchronous Clocking Helps Reduce Timing Related Design Problems**
- **8–Pin "Mini-SOIC" or 8–Pin DIP Packaging Achieves Minimum Footprint for Space-Critical Applications**
- **5 Volt CMOS Technology can Drive 60 pf Load**
- **Meets or Exceeds Traditional Can Oscillator Specifications in High-Performance Systems**

ICD2031A Satellite Oscillator Block Diagram

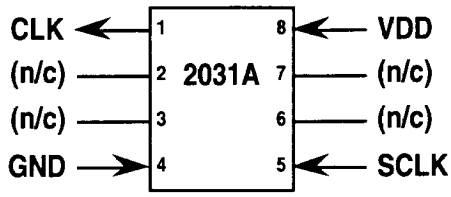


General

The ICD2031A is a unique new type of oscillator device. Though conceptually simple, its implications for system design are profound.

At a minimum, the part replaces a hybrid can-type oscillator with a device which is both smaller in size and less expensive in cost. But the device further offers the ability to synchronize its clock to all other clocks in the system. This capability opens the door to new design techniques never before obtainable with conventional PC board system clocking schemes.

Pin Descriptions



Signal Descriptions

Signal	Pin Number	Signal Function
GND	4	Ground
SCLK	5	SCLK (Satellite Clock) Reference Oscillator Input (1 MHz)
CLK	1	Clock Oscillator Output
VDD	8	+5 Volts

A Perspective on the Problems in High Speed Clocking

As PC boards and bus interfaces run at higher and higher clock frequencies, the problem of how to handle high-frequency clocks pervades the design process. Today's high performance system designs face the following problems:

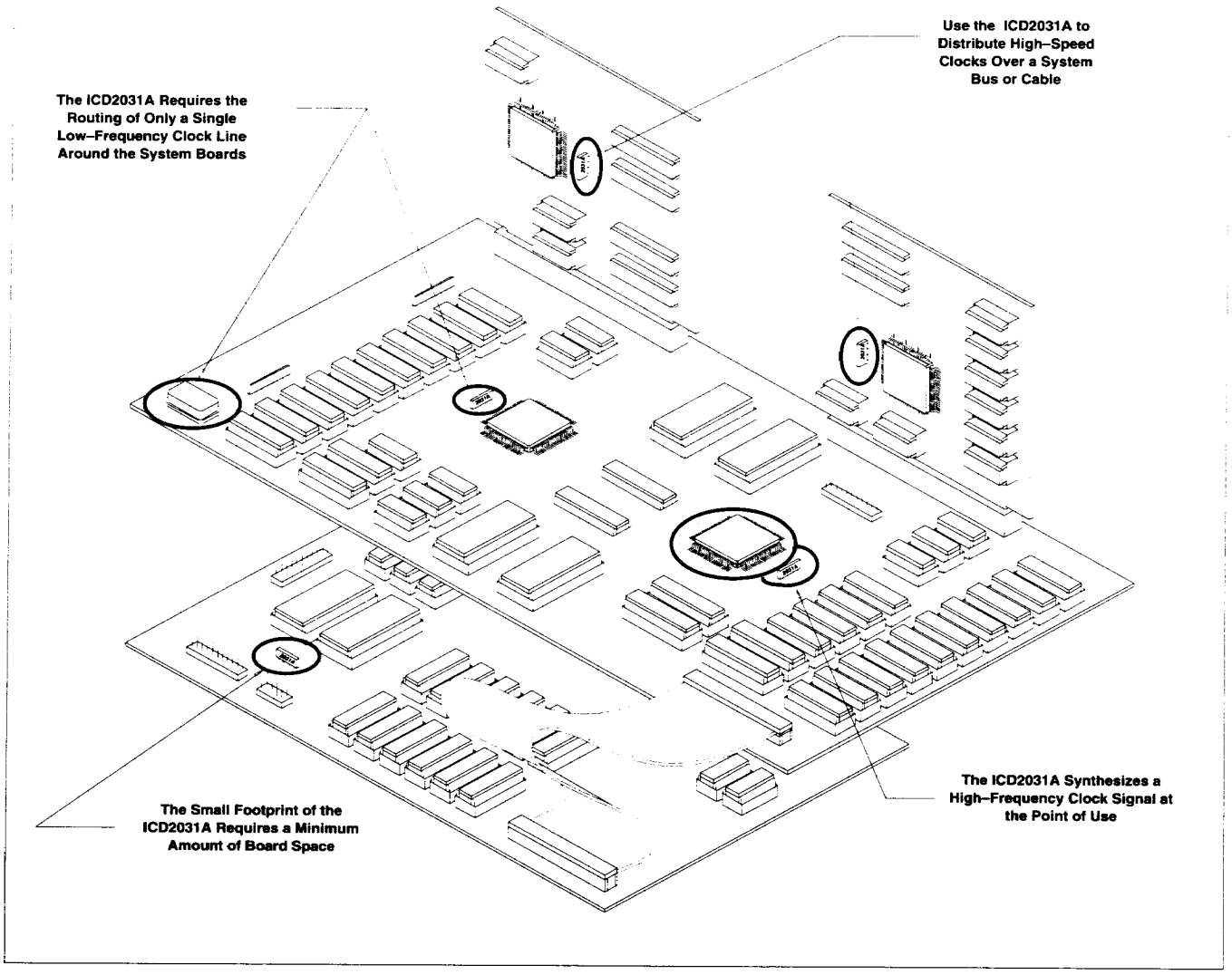
- **Increasing Speeds & Proliferation of Clocks on PC Boards** — Clock rates of greater than 50 MHz are now routine. With these greater clock rates comes a much greater demand on the part of the engineer and the layout designer to manage "transmission-line" effects. While a typical PC board once contained only a single VLSI part such as a microprocessor, most designs now include a large number of such components which are actually customized synchronous processors. Each of these devices typically requires a high-frequency clock as an input. A single high-frequency clock per PC board is no longer sufficient; today a modern PC board may require five or more such clocks.

- **System Noise & Routing Problems** — Maintaining a synchronous high-frequency signal (particularly at 60 MHz or above) across a large PC board can become a routing nightmare. Inductively coupled noise from adjacent signal sources significantly reduces system performance. The long traces involved are susceptible to crosstalk, stray capacitance, and long lead delays. Such constraints place a large burden on a single can oscillator as it tries to supply numerous devices over long distances. A large load manifests itself as delay, worsening slew rates for transitions and reducing the DC levels of the clock signals.

- **Skew Problems** — An 80 MHz clock has a 12.5 ns cycle time. In a perfect medium there is a delay of 1 ns per 9 inches. Through a copper trace across a large PC board, or through connectors and onto peripheral boards, can mean adding many nanoseconds of delay to a signal. A few nanoseconds to a 12 ns clock means a 25% deviation in the phase of the clock.

- **Multiple Crystal Can Oscillator Problems** — The traditional approach of placing a can oscillator next to each component in need of a clock signal is not feasible when several components spread widely apart all require high-frequency timing. The PC board footprint of multiple crystal cans, and the associated acquisition cost, preclude this approach for both area and cost-sensitive applications. If the clocks must be synchronous, the crystal cans are ruled out entirely. There is no way to guarantee the phase relationship or exact frequency between two crystal oscillators of the same value.

- **FCC Certification** — As clock rates climb, there is an associated increase in high-energy EMI/RFI radiation. This radiation must be restrained in order to comply with FCC rules. At the same time, the rules are getting tighter. Faster clocks and tighter restrictions present mutually exclusive design agendas.



The Satellite Oscillator Concept

The ICD2031A alleviates most of the problems associated with high-frequency clocks. As the block diagram on the first page shows, the heart of the ICD2031A is a proprietary frequency generator. This generator synthesizes a unique and inherently stable frequency output from an input reference frequency.

Satellite Distributed Clocking

Instead of using a single central clock generator to handle all clocks, the ICD2031A allows the engineer to distribute the required clocks to the point of need. Long routing traces now must handle only low-frequency signals (the SCLK clock). Each device gets its own clean, unloaded high-frequency clock. And if the part requires the same frequency as another part somewhere else in the system (and not even necessarily on the same board), those two signals will be synchronized with each other.

SCLK

The Satellite BUS (SCLK) is the low-frequency (1 MHz) reference clock which is routed throughout the system, including the primary PC board and any peripheral boards. This signal can also be routed through cables. From this reference signal, the high-frequency clocks are generated. All satellite oscillators are synchronized to the SCLK.

Reduced Noise Generation and EMI/RFI Emissions

The high-frequency signals only exist next to their recipient component devices. This keeps high frequency traces to a minimum, with their lengths measured in tenths of inches. Since each component has its own dedicated clock driver, a clean, unloaded noise-free signal is guaranteed. And since these traces are short, the subsequent radiation of spurious high-energy harmonics is significantly reduced.

Reduced Routing Problems

With the ICD2031A, the "transmission-line" aspect of clock trace routing on the PC board is reduced to the well understood problem of routing a low-frequency clock (1 MHz) around the board.

Reduced Cost

The ICD2031A uses standard CMOS processing and packaging technology. Since no labor-intensive hybrid manufacturing process is involved, the traditional semiconductor cost curves apply over the life of the product. The cost of this technology is therefore less than the metal can oscillators being replaced.

Reduced Package Size

The ICD2031A comes in two different packaging configurations: an 8–pin SOIC for surface mount applications offering the best footprint currently achievable for a fixed-frequency oscillator; and an 8–pin DIP for thru-hole applications.

Circuit Description

The ICD2031A uses a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency, (1 MHz from the SCLK input), goes into a "divide-by-n" block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

Layout & Power Conditioning Considerations

A clean power supply is important, particularly at the higher frequencies. For best results, use either a +12V supply through a +5V Zener diode or a 3–pin +5V voltage regulator. If a +12V supply is not available, a low-pass filter consisting of a capacitor and a 22Ω resistor is recommended.

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1µf multi-layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

Refer to IC DESIGNS Application Note "*Power Feed and Board Layout Issues*" for more details and illustrative schematics.

Minimized Parasitics

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. All the synthesis VCO's are separated from their digital logic. Separate ground buses for the analog and digital circuitry are used. The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce.

Low Sensitivity To Temperature and Process Variations

Because of its feedback circuitry, the ICD2031A is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO.

Skew, Loading & Phase-Coherence Issues

The specifications for rise time, fall time, clock skew and device-to-device skews are all load-dependent and threshold-dependent.

The basic output pad supports 3 ns rise and fall times per 25 pf load.

To guarantee optimum phase coherence between multiple ICD2031A devices, loads must be matched. If the loads are dissimilar, the following equations will help determine the amount of skew which will result between the two parts:

CMOS Thresholds (2.5V)	—>	0.5ns / 8pf load difference
TTL Thresholds (1.5V)	—>	0.3ns / 8pf load difference

Selecting Output Value

Any integer value multiplier in the range 1–87 may be chosen. At manufacturing time, the desired multiplier is "blown" into an internal fuse-link PROM.

A few common multiplier values are stocked and available for sampling. Custom frequency values must be special-ordered. There is no extra charge for a custom frequency; however, there is a minimum ordering quantity. Please consult your local IC DESIGNS sales representative (or the factory) for the available stock multipliers or the current custom ordering requirements.

Ordering Information

Part Number	Package Type	Temperature Range	Desired Output Frequency
ICD2031A	P = 8–Pin Plastic DIP	C = Commercial (0°C – +70°C)	-X = X MHz (1 ≤ X ≤ 87)
	C = 8–Pin Ceramic DIP		
	S = 8–Pin SOIC		

NOTE: Minimum quantities apply for custom frequencies.

Example: order *ICD2031ASC–66* for the 66MHZ ICD2031A commercial temperature range device packaged in an 8–pin SOIC.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VCC + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		125	mWatts

DC Characteristics

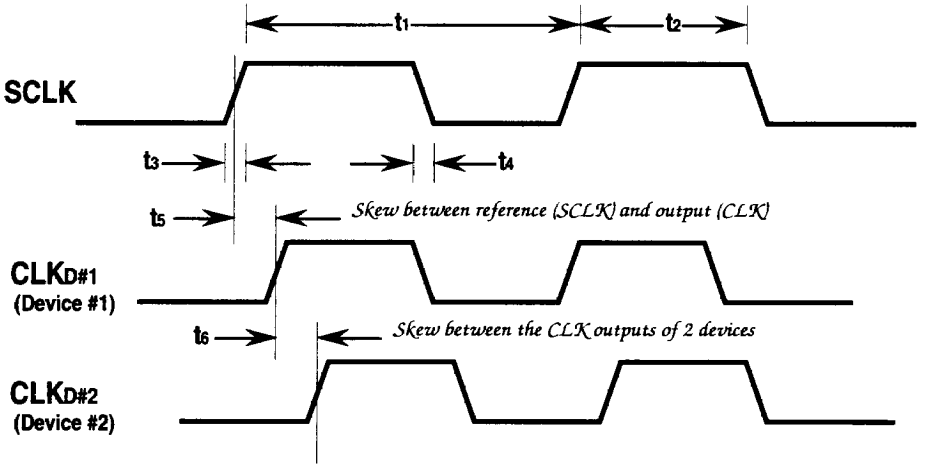
VDD = +5V ±10%
0°C ≤ T_{CASE} ≤ +70°C

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level output voltage	2.4		Volts	I_{OH} = –4.0 ma
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 4.0 ma
I_{IH}	Input high current		2.5	µa	V_{IH} = 4.6 v
I_{IL}	Input low current		–500	µa	V_{IL} = 0.4 v
I_{OL}	Output leakage current		2.5	µa	
I_{CC}	Power supply current	3	15	ma	
C_{IN}	Input Capacitance		10	pf	
C_{LD}	Maximum Load Capacitance		60	pf	

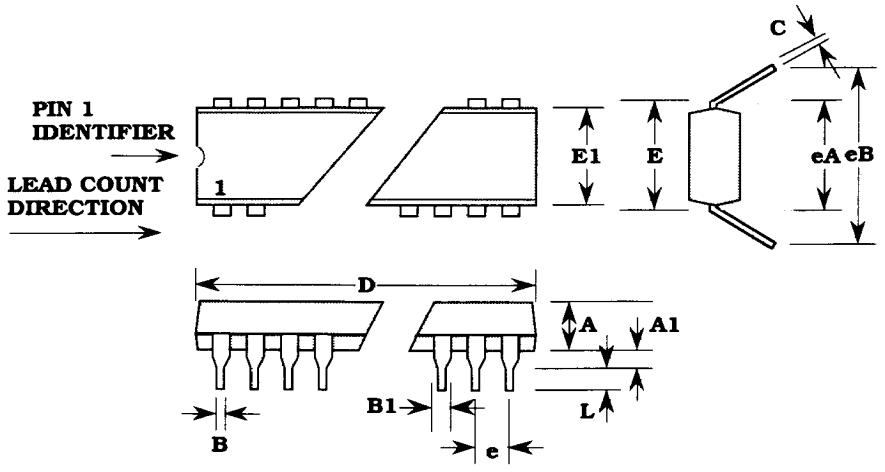
AC Characteristics

VDD = +5V ±10%
0°C ≤ T_{CASE} ≤ +70°C)

Symbol	Name	Description	Min	Max	Units
t_1	SCLK freq	SCLK Satellite Clock Reference Oscillator		1	MHz
t_2	SCLK duty cycle	Duty cycle for the input reference SCLK defined as t_2/t_1	25%	75%	
t_2	CLK duty cycle	Duty cycle for the oscillator output CLK defined as t_2/t_1	45%	55%	
t_3	rise time	Rise time for the output oscillator into a 25 pf load		3	ns
t_4	fall time	Fall time for the output oscillator into a 25 pf load		3	ns
t_5	CLK skew	Skew delay between the SCLK input and the CLK output	–1	1	ns
t_6	$CLK_{D\#1}$ to $CLK_{D\#2}$ skew	Skew delay between the CLK outputs of Device #1 and Device #2	–1	1	ns
	clk stable	Time required for the output oscillator to become valid after Power-Up	0.1	15	msec
	max clk	Maximum CLK output frequency		87	MHz

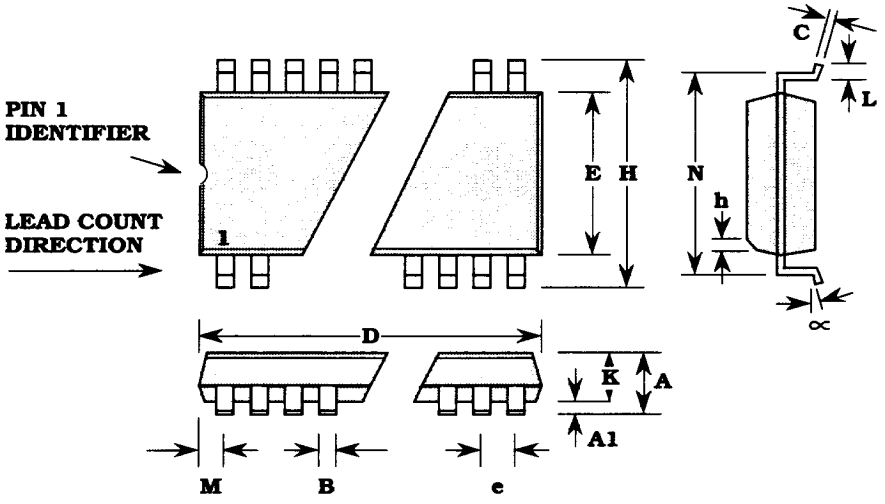


Packaging Information



PDIP Outline		
	Lead Count 8	
SYMBOL	MIN	MAX
A	.155	.160
A1	.015	–
B	.018	.022
B1	.050	.070
C	.008	.012
D	.348	.390
E	.290	.310
E1	.220	.270
e	.100	TYP
eA	.290	—
eB	—	.310
L	.100	—

(Dimensions in Inches)



SOIC Outline		
	Lead Count 8	
SYMBOL	MIN	MAX
A	.053	.069
A1	.004	.009
B	.014	.019
C	.010	REF
D	.188	.196
E	.150	.158
e	.050	TYP
H	.228	.244
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.049	.060
M		
N	.148	.184

(Dimensions in Inches)

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