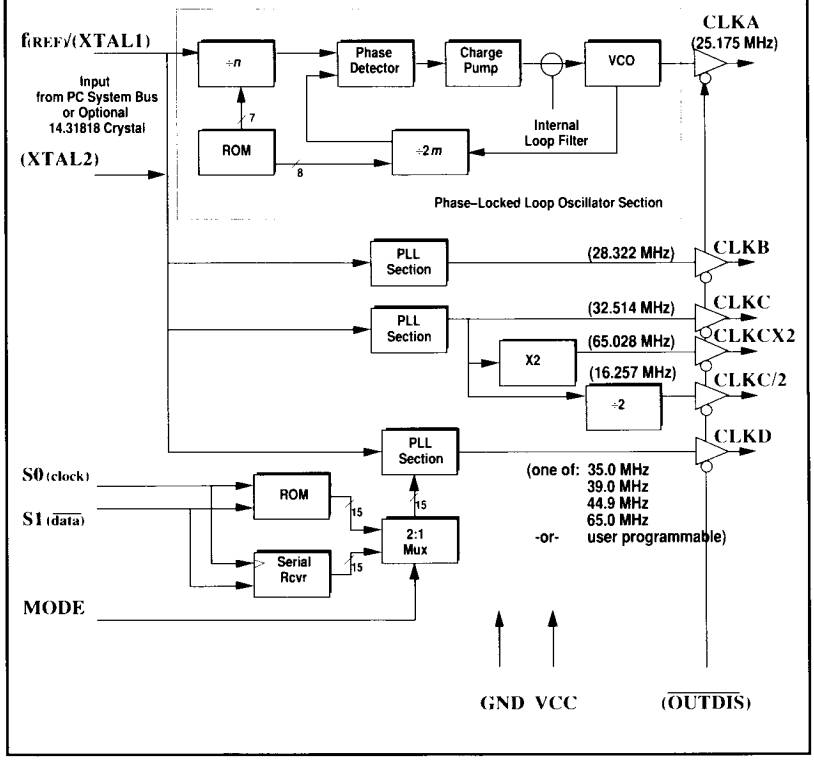
ICD2041

Quad Programmable Clock Generator

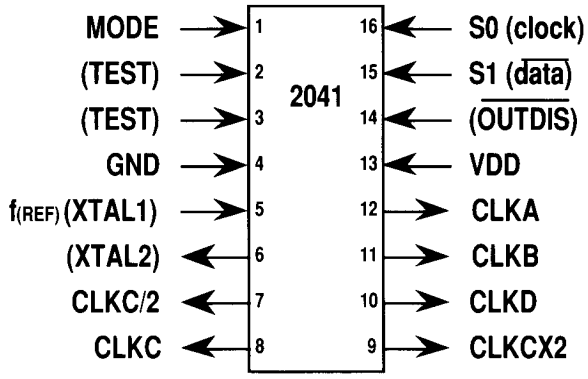
Single–Chip Quad Oscillator for Personal Computer Graphic Boards Replaces as many as 6 Standard Components

- **4 Independent Clock Outputs**
- **Phase–Locked Loop Oscillator Input Derived from PC System Bus or from Single 14.31818 MHz Crystal**
- **Programmable Frequency Range from 5MHz – 80MHz with 50% Duty Cycle**
- **Ideally Suited for VGA/EGA, Super VGA, and 8514 Graphic Applications**
- **Sophisticated Internal Loop–Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **Tri–State Oscillator Control Disables Outputs for Test Purposes**
- **"Change–on–the–Fly" Frequency Selection Supports most Popular VGA/8514 Chip Sets**
- **5–Volt Operation**
- **Low–Power, High–Speed 1.25µ CMOS Technology**
- **Available in 16–Pin DIP or Surface Mount Package Configuration**

ICD2041 Quad–Programmable VGA Clock Generator Block Diagram



Pin Descriptions



Signal Descriptions

Signal	Pin Number	Signal Function
MODE	1	MODE=0 then CLKD is in programmable mode. (S0 & S1 become serial data lines.) MODE=1 then CLKD is in selection mode. (Determined by select lines S0 & S1.)
TEST	2,3	For factory test only. Tie lines to VCC.
GND	4	Ground
$f_{(REF)}$/(XTAL1)	5	Input Reference Oscillator (nominally 14.31818 MHz derived from PC system bus). An optional crystal may be used as input if the reference signal is not available.
(XTAL2)	6	Optional Oscillator output to a 14.31818 MHz Series – Resonant Crystal if the PC System Bus Clock Signal is not available.
CLKC/2	7	16.257 MHz Output
CLKC	8	32.514 MHz Output
CLKCX2	9	65.028 MHz Output
CLKD	10	Programmable Oscillator D Output (See table of values below.)
CLKB	11	28.322 MHz Output
CLKA	12	25.175 MHz Output
VDD	13	+5 Volt
OUTDIS–	14	Output Disable (Tri–State Output Enable) when signal is pulled low (Internal pull–up allows no–connect if tri–state is not required.)
S1 (data–)	15	MODE=0, S1 is serial data input line for CLKD MODE=1, S1 is select line for CLKD
S0 (clock)	16	MODE=0, S0 is serial clock input line for CLKD MODE=1, S0 is select line for CLKD

General

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of the oscillators required to build such multi–function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2041 Quad–Programmable Clock Generator offers four different oscillators in a single package. Three of the oscillators are of a fixed value while the fourth oscillator is fully user–programmable and may be changed 'on–the–fly'. To program the part, a 15–bit word is shifted in which defines the desired frequency value from 5MHz to 80MHz. The ICD2041 is ideally suited for use in existing designs since it requires no support from the graphics chip set and outputs 4 concurrent frequencies. It is also appropriate for those unique applications where a dynamically programmable oscillator is desirable.

Non–Programmable Oscillator Operation (CLKA, CLKB, CLKC)

The following table describes each oscillator:

Oscillator	Frequencies Available (MHz)
CLKA	25.175
CLKB	28.322
CLKC	16.257, 32.514, 65.028

CLKC employs a unique frequency modification circuit in order to generate multiple outputs from the same base frequency (32.514 MHz). All three of these outputs are available concurrently.

Programmable Oscillator Operation (CLKD)

CLKD is the programmable oscillator offering two modes of operation. The first mode uses two select lines to select one of 4 different preset frequencies, while the other mode allows the user to program any desired frequency. The two different modes are controlled by the MODE signal.

CLKD with MODE = 1 Frequency (MHz)			
S1	**S0**	**CLKD ROM Option 1**	**CLKD ROM Option 2**
0	0	35.0	44.0
0	1	39.0	36.0
1	0	44.9	30.0
1	1	65.0	80.0

[Note: 80MHz operation is only available in the ICD2041B speed selected part.]

When MODE = 0, Oscillator D enters its programmable mode. Signals S0 (clock) and S1 (data–) become a serial interface, allowing a 15–bit number to be shifted in. The procedure to determine the proper number is outlined in the Application Note "Determining the Proper Code for a Given Output Frequency" and its associated BASIC program, both of which are available from IC DESIGNS.

Tri–State Output Operation

The OUTDIS– signal, when pulled low, will tri–state all the clock output lines. This supports "wired–or" connections between external clock lines (ex: the Feature Connector external clock), and allows for procedures such as automated testing where the clock must be disabled. The OUTDIS– signal contains an internal pull–up but should be tied to VCC if not used.

Optional External Crystal

Normal operation requires a nominal 14.31818 MHz reference signal which comes from the PC system bus. In modern PC designs, this signal is stable enough for use with the ICD2041. For those cases where a stable, noise–free system clock cannot be guaranteed, the ICD2041 includes a built–in oscillator which can serve as the reference source. If this mode is desired, an external series–resonant 14.31818 MHz crystal should be connected between the XTAL1 and XTAL2 pins.

No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2041.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher dot clock frequencies above 50MHz.

A full power and ground plane layout should be employed both under and around the IC package. The power pin should be bypassed to ground with a 0.1µf multi–layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin.

The designer should also avoid routing any of the output traces of the ICD2041 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2041 closest to the device requiring the highest frequency. If the high–frequency clocks must be routed to board extremes, the ICD2031 distributed 'satellite' oscillators should be considered.

Circuit Description

Each oscillator block is a classical phase–locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 Mhz (as derived from the PC system bus), and goes into a "divide–by–n" block. The resultant signal becomes the reference frequency for the phase–locked loop circuitry.

The phase–locked loop is a feedback system which phase matches the reference signal and the variable 'synthesized' signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately 'lock–on' to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal 'loop filter' provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

The parts use center pins to deliver power and ground to the die instead of the more conventional corner pins. The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground–bounce and output crosstalk.

Stability and "Bit–Jitter"

The long–term frequency stability of the IC DESIGNS phase–locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short–term stability (also called "bit–jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of "bit–jitter". The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low–gain VCO's and sufficient loop filtering are design elements specifically included to minimize this "bit–jitter". The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2041 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures that the loop filter will track the same process variations as does the VCO. With the ICD2041, no manufacturing "tweaks" to external filter components are required as is the case with external "de–coupled" filters.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VCC	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VCC + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		125	mWatts

DC Characteristics

VCC = +5V ±10%

$0°C \leq T_{CASE} \leq +70°C$

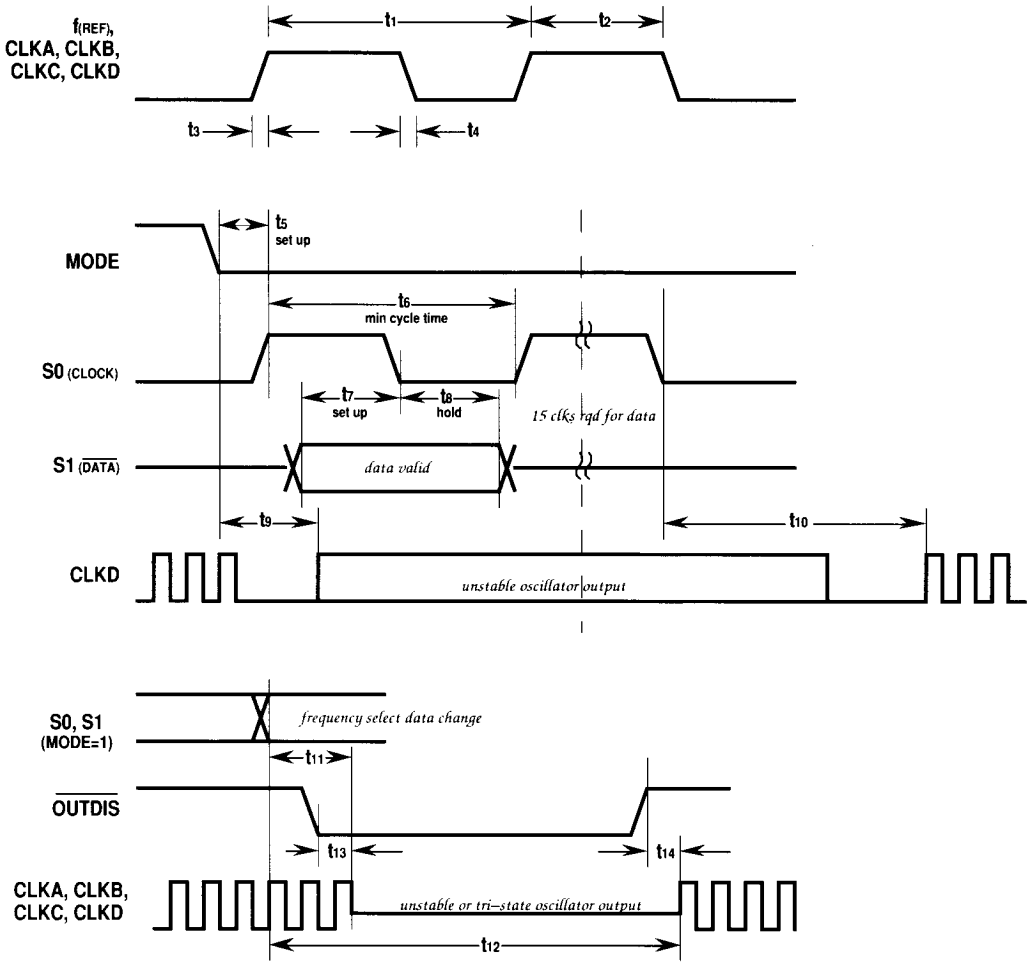
Name	Description	Min	Max	Units	Conditions
V_{IH}	High–level input voltage	2.0		Volts	
V_{IL}	Low–level input voltage		0.8	Volts	
V_{OH}	High–level output voltage	2.4		Volts	I_{OH} = -4.0 ma
V_{OL}	Low–level output voltage		0.4	Volts	I_{OL} = 4.0 ma
I_{IH}	Input high current		2.5	µa	V_{IH} = 4.6 v
I_{IL}	Input low current		-500	µa	V_{IL} = 0.4 v
I_{OL}	Output leakage current		2.5	µa	
I_{CC}	Power supply current		25	ma	
C_{IN}	Input Capacitance		10	pf	

AC Characteristics

VCC = +5V ±10%

$0°C \leq T_{CASE} \leq +70°C$

Symbol	Name	Description	Min	Max	Units
t_1	ref freq	Reference Oscillator nominal value		14.31818	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as t_2/t_1	45%	55%	
t_3	rise time	Rise time for the output oscillators into a 25pf load		3	ns
t_4	fall time	Fall time for the output oscillators into a 25pf load		3	ns
t_5	set–up	Delay required after MODE goes low prior to starting the S0 clock line		0	ns
t_6	cycle time	Minimum cycle time for the S0 clock	500		ns
t_7	set–up	Time required for the data to be valid prior to the falling edge of S0 (clock)	250		ns
t_8	hold	Time required for the data to remain valid after the falling edge of S0 (clock)	250		ns
t_9	clk unstable	Time CLKD oscillator remains valid after MODE signal goes low		0	ns
t_{10}	clk stable	Time required for the CLKD oscillator to become valid last S0 clock	0.1	5	msec
t_{11}	clk unstable	Time the output oscillators remain valid after the S0 or S1 select signals change value		0	ns
t_{12}	clk stable	Time required for the output oscillators to become valid after the S0 or S1 select signals change value	0.1	5	msec
t_{13}	tri–state	Time for the output oscillators to go into tri–state mode after OUTDIS– signal assertion		12	ns
t_{14}	clk valid	Time for the output oscillators to recover from tri–state mode after OUTDIS– signal goes high		12	ns



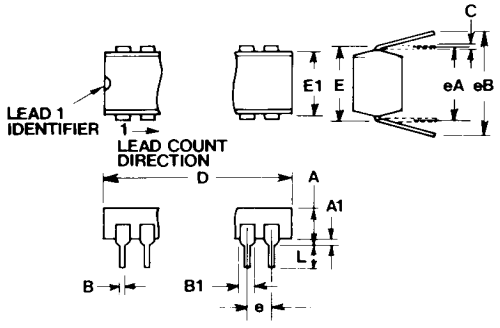
Ordering Information

Part Number	Speed Designation	Package Type	Temperature Range	CLKD ROM Option
ICD2041	A – 65MHz	P – 16–Pin Plastic DIP	C – Commercial (0°C – +70°C)	1
	B – 80MHz	C – 16–Pin Ceramic DIP		2
		S – 16–Pin SOIC		

Example: order *ICD2041APC–1* for the 65MHZ ICD2041, 16–pin plastic DIP, commercial temperature range device which utilizes CLKD ROM Option 1 table of decodes.

Packaging Information

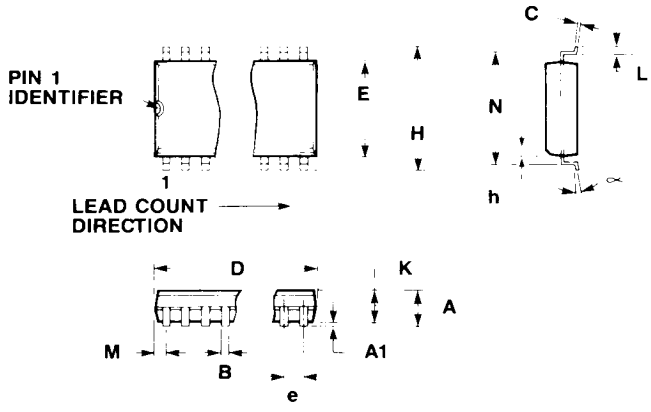
PDIP Outline



SYMBOL	LEAD COUNT 16 MIN	MAX
A	.195	.200
A1	.015	–
B	.015	.020
B1	.050	.070
C	.008	.012
D	.745	.790
E	.290	.310
E1	.220	.280
e	.100	TYP
eA	.290	–
eB	–	.310
L	.100	–

(Dimensions in Inches)

SOIC Outline



SYMBOL	LEAD COUNT 16 MIN	MAX
A	.099	.104
A1	.004	.009
B	.014	.019
C	.010	REF
D	.405	.410
E	.294	.299
e	.050	TYP
H	.402	.419
h	.025 x	45°
L	.030	.040
∝	0°	8°
K	.088	.098
M	.020	.030
N	.335	.351

(Dimensions in Inches)

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