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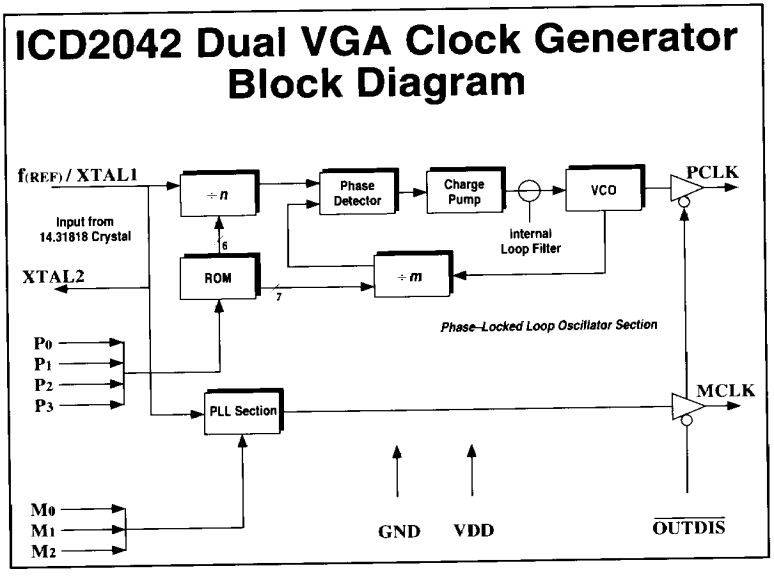
ICD2042

Dual VGA Clock Generator

Single-Chip Dual Oscillator for Personal Computer Graphic Boards Handles Frequency Requirements of Popular VGA/8514 Chip Sets.

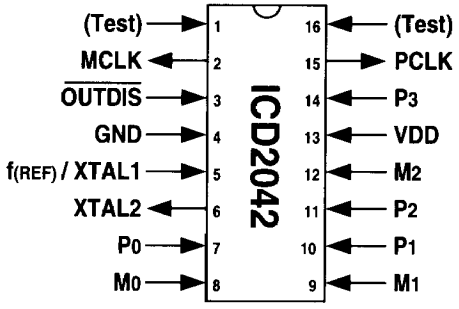
- 2 Independent Clock Outputs — Handles Separate Pixel Clock and Memory Clock
- Phase-Locked Loop Oscillator Input Derived from PC System Bus or from Single 14.31818 MHz Crystal
- Ideally Suited for VGA, Super VGA, and 8514 Graphic Applications
- Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters
- Tri-State Oscillator Control Disables Outputs for Test Purposes
- "Change-on-the-Fly" Frequency Selection Supports Most Popular VGA/8514 Chip Sets
- 5–Volt Operation
- Low-Power, High-Speed 1.25µ CMOS Technology
- Available in 16–Pin DIP or SOIC Package

ICD2042 Dual VGA Clock Generator Block Diagram



NOTE: For new designs, use the ICD2042A

Pin Descriptions



Signal Descriptions

Signal	Pin #	Signal Function
(Test)	1, 16	For factory test only. No connection.
MCLK	2	Memory Clock Oscillator Output (see Memory Clock Selection Table)
OUTDIS–	3	Output Disable (Tri-State Output Enable) when signal is pulled low. (Internal pull-up allows no-connect if tri-state operation not needed).
GND	4	Ground
$f_{(REF)}$ / XTAL1	5	Input Reference Oscillator (nominally 14.31818 MHz.) A crystal may be used if a reference oscillator is not available.
XTAL2	6	Optional Oscillator Output to a 14.31818 MHz Series-Resonant Crystal
P_0	7	Input Pixel Clock Selection Signal
M_0	8	Input Memory Clock Selection Signal
M_1	9	Input Memory Clock Selection Signal
P_1	10	Input Pixel Clock Selection Signal
P_2	11	Input Pixel Clock Selection Signal
M_2	12	Input Memory Clock Selection Signal
VDD	13	+5 volts
P_3	14	Input Pixel Clock Selection Signal
PCLK	15	Pixel Clock Oscillator Output (see Pixel Clock Selection Table)

General

The proliferation of video standards, support for various monitors, increasing screen resolutions, and different memory speeds present in the DOS graphics community often require as many as six different crystal can oscillators per PC board. A new family of frequency synthesis parts from IC DESIGNS replaces the large number of these oscillators required to build such multi-function graphic boards as EGA, VGA, Super VGA, and 8514. These parts synthesize all the required frequencies in a single monolithic device, thus lowering manufacturing costs and significantly reducing the printed circuit board space required.

The ICD2042 Dual VGA Clock Generator supports new designs using the newer graphic chip sets which generate output frequency select information. The ICD2042 features two independent clock outputs for the pixel clock and the memory clock which are chosen via select lines. Additional features include tri-stateable outputs and direct support for popular graphics chip set selection decodes.

Output Frequency Accuracy

The accuracy of the ICD2042 output frequencies depends on the target output frequencies. The tables within this document contain target frequencies which differ from the actual frequencies produced by the clock synthesizer.

As stated previously, the output frequencies of the ICD2042 are an integral fraction of the input (reference) frequency:

$$f_{(OUT)} = (2 * f_{(REF)} * \frac{p}{q})$$

Only certain output frequencies are possible for a particular reference frequency. However, the ICD 2042 always produces an output frequency within 0.1% of the target frequencies listed, which is more than sufficient to meet standard display requirements. [Actual values are available from the factory.]

Tri-State Output Operation

The OUTDIS– signal, when pulled low, will tri-state both the MCLK and the PCLK output lines. This supports wired-or connections between external clock lines (ex: the Feature Connector external clock) and allows for procedures such as automated testing, where the clock must be disabled. The OUTDIS– signal contains an internal pull-up but should be tied to VCC if not used.

External Reference Crystal

Normal operation requires a nominal 14.31818 MHz reference signal. The ICD2042 includes a built-in oscillator which can serve as the reference source. An external series-resonant 14.31818 MHz crystal should be connected between the XTAL1 and XTAL2 pins.

Pixel and Memory Clock Oscillator Selection

The output frequency values of the pixel and memory clock oscillators are selected by the pixel and memory clock selection inputs: P_0–P_3 and M_0–M_1, respectively. This feature allows the ICD2042 to support different video configurations.

At any time during operation the selection lines can be changed to select a different frequency. When this occurs, the internal phase-locked loop will immediately seek the newly selected frequency. During the transistion period, the clock output will not glitch and will settle to the new frequency.

Normally, the MCLK select lines are hard-wired during manufacturing to match the desired memory speed. As long as the transitional period of changing frequency is acceptable to the system, a different memory clock frequency output may be generated by changing the MCLK select lines of the ICD2042.

The selection tables for the different pixel and memory clock ROM decode options are shown below:

Pixel Clock ROM Decode Options (MHz)

P_3	P_2	P_1	P_0	Word	2042–1B	2042–5	2042–7	2042–13	2042–14
0	0	0	0	0	80.000	25.175	57.283	25.175	80.000
0	0	0	1	1	65.000	28.322	31.334	28.322	65.000
0	0	1	0	2	65.000	36.000	30.240	65.000	65.000
0	0	1	1	3	32.514	44.900	75.000	44.900	32.514
0	1	0	0	4	25.175	31.320	50.350	28.322	25.175
0	1	0	1	5	28.332	28.322	56.664	36.000	28.332
0	1	1	0	6	36.000	40.000	72.000	40.000	36.000
0	1	1	1	7	40.000	65.000	80.000	36.000	40.000
1	0	0	0	8	50.350	25.175	100.000	25.175	50.350
1	0	0	1	9	44.900	44.900	89.800	28.322	44.900
1	0	1	0	10	65.000	65.000	65.000	78.000	65.000
1	0	1	1	11	36.000	80.000	40.000	65.000	36.000
1	1	0	0	12	25.175	31.320	50.000	63.000	25.175
1	1	0	1	13	28.332	40.000	57.283	72.000	28.332
1	1	1	0	14	57.273	74.160	31.334	40.000	57.273
1	1	1	1	15	40.000	34.900	30.240	50.000	40.000

Memory Clock ROM Decode Options (MHz)

M_2	M_1	M_0	Word	2042–1B	2042–5	2042–7	2042–13	2042–14
0	0	0	0	48.0	32.3	40.0	48.0	48.0
0	0	1	1	39.8	35.8	41.0	39.8	39.8
0	1	0	2	29.8	39.8	41.5	66.0	66.0
0	1	1	3	24.8	45.0	42.0	50.0	50.0
1	0	0	4	28.0	28.2	42.5	56.644	56.644
1	0	1	5	32.0	42.5	43.0	32.0	32.0
1	1	0	6	44.0	38.0	44.0	44.0	44.0
1	1	1	7	35.8	48.0	48.0	39.8	39.8

NOTE: Custom Frequency Tables for the ICD2042 are no longer accepted. For designs requiring Custom Frequency Tables, please refer to the ICD0242A Datasheet.

PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher pixel clock frequencies above 50MHz.

A full power and ground plane layout should be employed both under and around the IC package. It is important that the ground plane be nearly continuous with a minimum of cuts, holes, or breaks. Both analog and digital ground pins should go directly to this plane.

To produce an output of high spectral purity, additional supply noise precautions might be required, particularly in noisy environments. The power bus should be bypassed to ground with a 0.1µf multi-layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22 ohm resistor placed between the power supply and the IC can help to filter noisy supply lines. This method works quite well, but it has one drawback which must be allowed for, namely that there will be a frequency-dependent voltage drop across the resistor. Deriving power from the +12V supply is also effective. Drop the supply thru 180 ohms to a 5.1V zener diode (1N5231B) to ground.

The designer should also avoid routing the two output traces of the ICD2042 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2042 closest to the device requiring the highest frequency. For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues.*

Circuit Description

Each oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 Mhz (as derived from the PC system bus) and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable "synthesized" signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

Minimized Parasitic Problems

All of the IC DESIGNS families of frequency synthesis components have been optimized to reduce internal noise and crosstalk problems. To minimize adjacency problems, all the synthesis blocks are physically separated into discrete elements with their output oscillator pins placed on separate sides of the package. Further, all the synthesis VCO's are separated from their digital logic. Finally, separate ground buses for the analog and digital circuitry are used.

The parts use center pins to deliver power and ground to the die instead of the more conventional corner pins. The package leadframes are optimized for the lowest possible inductance from the supply pin on the package to the die within, and results in minimized supply noise problems such as ground-bounce and output crosstalk.

Stability and "Bit-Jitter"

The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2042 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2042, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

Ordering Information

Part Number	Package Type	Temperature Range	Pixel Clock ROM Option
ICD2042	P = 16–Pin Plastic DIP	C – Commercial (0°C – +70°C)	–1B
	C = 16–Pin Ceramic DIP		–5
	S = 16–Pin SOIC		–7
			–13
			–14

Example: order *ICD2042PC–1B* for the ICD2042, 16–pin plastic DIP, commercial temperature range device which utilizes the Pixel/Memory Clock ROM Option 1B table of frequency decodes.

Electrical Data

Maximum Ratings

Name	Description	Min	Max	Units
VDD	Supply voltage relative to GND	–0.5	7.0	Volts
V_{IN}	Input Voltage with respect to GND	–0.5	VCC + 0.5	Volts
T_{OPER}	Operating Temperature	0	+70	°C
T_{STOR}	Storage Temperature	–65	+150	°C
T_{SOL}	Max Soldering Temperature (10 sec)		+260	°C
T_J	Junction Temperature		+125	°C
P_{DISS}	Power Dissipation		350	mWatts

DC Characteristics

VDD = +5V ±5%
0°C ≤ T_{CASE} ≤ +70°C

Name	Description	Min	Max	Units	Conditions
V_{IH}	High-level input voltage	2.0		Volts	
V_{IL}	Low-level input voltage		0.8	Volts	
V_{OH}	High-level output voltage	2.4		Volts	I_{OH} = –2.0ma
V_{OL}	Low-level output voltage		0.4	Volts	I_{OL} = 2.0ma
I_{IH}	Input high current		100	µa	V_{IH} = 5.25V
I_{IL}	Input low current		–250	µa	V_{IL} = 0V
I_{OZ}	Output leakage current		10	µa	(tri-state)
I_{DD}	Power supply current		50	ma	(@ hi freq)
C_{IN}	Input Capacitance		10	pf	

AC Characteristics

VDD = +5V ±5%
0°C ≤ T_{CASE} ≤ +70°C)

Symbol	Name	Description	Min	Max	Units
t_1	ref freq	Reference Oscillator nominal value		14.31818	MHz
t_2	duty cycle	Duty cycle for the output oscillators defined as t_2/t_1	40%	50%	(@ hi freq)
t_3	rise time	Rise time for the output oscillators into a 25pf load		3	ns
t_4	fall time	Fall time for the output oscillators into a 25pf load		3	ns
t_5	clk unstable	Time the output oscillators remain valid after P_{0-3} or M_{0-2} select signals change value		0	ns
t_6	clk stable	Time required for the output oscillators to become valid after P_{0-3} or M_{0-2} select signals change value		10	msec
t_7	tri-state	Time for the output oscillators to go into tri-state mode after OUTDIS– signal assertion		12	ns
t_8	clk valid	Time for the output oscillators to recover from tri-state mode after OUTDIS– signal goes high		12	ns