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# ICD2047

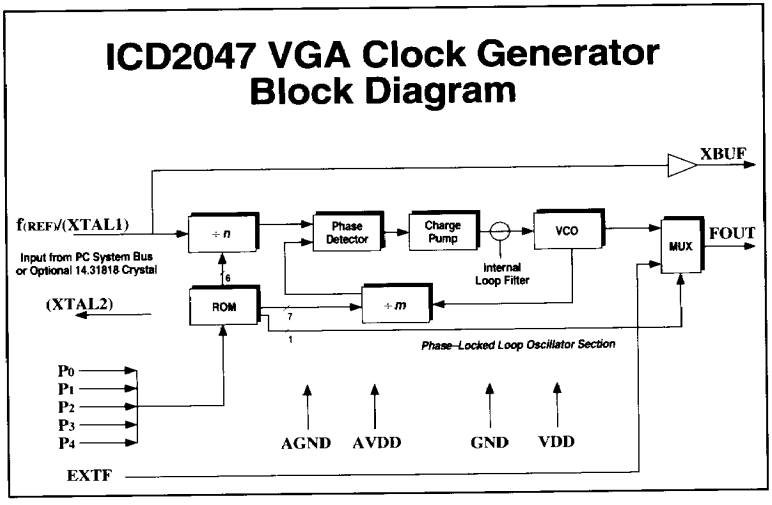
## VGA Clock Generator



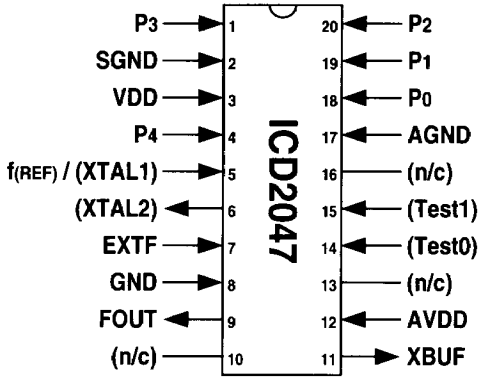
**Single-Chip Oscillator for Personal Computer Graphic Boards Handles Frequency Requirements of Popular VGA/8514 Chip Sets.**

- **Output Handles all Pixel Clock Requirements for Common Personal Computer Graphic Chip Sets**
- **Phase-Locked Loop Oscillator Input Derived from PC System Bus or from Single 14.31818 MHz Crystal**
- **Ideally Suited for VGA, Super VGA, and 8514 Graphic Applications**
- **Sophisticated Internal Loop Filter Requires no External Components or Manufacturing "Tweaks" as Commonly Required with External Filters**
- **"Change-on-the-Fly" Frequency Selection Supports Most Popular VGA/8514 Chip Sets**
- **5–Volt Operation**
- **Low-Power, High-Speed 1.25µ CMOS Technology**
- **Available in 20–Pin DIP or SOIC Package Configuration**

### ICD2047 VGA Clock Generator Block Diagram



## Pin Descriptions



## Signal Descriptions



| Signal | Pin # | Signal Function |
|---|---|---|
| $P_3$ | 1 | Frequency Selection Signal Input, Bit 3. TTL Compatible. |
| SGND | 2 | For factory test only. Tie line to GND, or leave floating. |
| VDD | 3 | +5 volts to I/O Ring |
| $P_4$ | 4 | Frequency Selection Signal Input, Bit 4 (MSB). TTL Compatible. |
| $f_{(REF)}$/(XTAL1) | 5 | Input Reference Oscillator. (nominally 14.31818 MHz derived from PC system bus.) An optional crystal may be used as input if the reference signal is not available. |
| (XTAL2) | 6 | Optional Oscillator output to a 14.31818 MHz Series-Resonant Crystal if the PC System Bus Clock Signal is not available |
| EXTF | 7 | Externally generated frequency input |
| GND | 8 | Digital Ground |
| FOUT | 9 | Clock Oscillator Output. TTL compatible. (see Clock Selection Table) |
| (n/c) | 10, 13, 16 | No connection |
| XBUF | 11 | Buffered Crystal Output. TTL compatible. |
| AVDD | 12 | +5 volts to Analog Core. See notes on power supply conditioning. |
| (Test0)<br>(Test1) | 14<br>15 | For factory test only. Tie to VDD, or leave floating.<br>Do not tie to GND. |
| AGND | 17 | Analog Ground |
| $P_0$ | 18 | Frequency Selection Signal Input, Bit 0 (LSB). TTL Compatible |
| $P_1$ | 19 | Frequency Selection Signal Input, Bit 1. TTL Compatible |
| $P_2$ | 20 | Frequency Selection Signal Input, Bit 2. TTL Compatible |

## General

The ICD2047 VGA Clock Generator is a monolithic CMOS integrated circuit which can generate any one of 32 different video pixel clock frequencies for use with EGA, VGA, Super VGA, and 8514 graphic boards. In addition, the ICD2047 can multiplex an externally generated signal source into the output path.

## FOUT Clock Oscillator Selection

The output frequency value of the clock oscillator is selected by the five clock selection inputs: $P_0$, $P_1$, $P_2$, $P_3$, and $P_4$. This feature allows the ICD2047 to support different video configurations. At any time during operation the selection lines can be changed to select a different frequency. The output will settle to the new frequency value after a short transition period.

The selection table for the different pixel clock ROM decode options is shown on the facing page.

## External Frequency Option

In addition to pre-programmed frequencies provided via the clock ROM Option Tables, some ICD2047 devices can multiplex an optional external frequency, EXTF (pin 7), through the FOUT signal (pin 9). This is controlled by the presence of an *EXTF* entry in one or more ROM Option Table locations. For these versions of the ICD2047, there are some special PC board layout considerations to observe whenever this feature is not used.

When changing frequencies or switching the output, the ICD2047 always prevents fractional clock cycles (which could mis-clock other devices) from occurring at the output. Because this fractional cycle protection requires a continuous pulse train as input, A CLOCK MUST ALWAYS BE PRESENT ON PIN 7, especially during power-up. Therefore, if the PC board does NOT use the pin 7 input, connect pin 7 to pin 6 via a jumper to supply the necessary pulse train.

## Use with Specific Manufacturer's Chip Sets

The ICD2047 is designed to be directly compatible with most of the commercially available graphic chip sets. Please call for applications information on the use of this device with a particular graphics chip set, or for specific frequency decodes for the newer VGA chip sets.

## Optional Reference Crystal

Normal operation requires a nominal 14.31818 MHz reference signal which comes from the PC system bus. In modern PC designs, this signal is stable enough for use with the ICD2047. For those cases where a stable, noise-free system clock cannot be guaranteed, the ICD2047 includes a built-in oscillator which can serve as the reference source. If this mode is desired, an external series-resonant 14.31818 MHz crystal should be connected between the XTAL1 and XTAL2 pins.

## No External Components Required

Under normal conditions no external components are required for proper operation of any of the internal circuitry of the ICD2047.

## Pixel Clock ROM Options Selection Table (MHz)

| $P_4$ | $P_3$ | $P_2$ | $P_1$ | $P_0$ | Word |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 0 | 2 |
| 0 | 0 | 0 | 1 | 1 | 3 |
| 0 | 0 | 1 | 0 | 0 | 4 |
| 0 | 0 | 1 | 0 | 1 | 5 |
| 0 | 0 | 1 | 1 | 0 | 6 |
| 0 | 0 | 1 | 1 | 1 | 7 |
| 0 | 1 | 0 | 0 | 0 | 8 |
| 0 | 1 | 0 | 0 | 1 | 9 |
| 0 | 1 | 0 | 1 | 0 | 10 |
| 0 | 1 | 0 | 1 | 1 | 11 |
| 0 | 1 | 1 | 0 | 0 | 12 |
| 0 | 1 | 1 | 0 | 1 | 13 |
| 0 | 1 | 1 | 1 | 0 | 14 |
| 0 | 1 | 1 | 1 | 1 | 15 |
| 1 | 0 | 0 | 0 | 0 | 16 |
| 1 | 0 | 0 | 0 | 1 | 17 |
| 1 | 0 | 0 | 1 | 0 | 18 |
| 1 | 0 | 0 | 1 | 1 | 19 |
| 1 | 0 | 1 | 0 | 0 | 20 |
| 1 | 0 | 1 | 0 | 1 | 21 |
| 1 | 0 | 1 | 1 | 0 | 22 |
| 1 | 0 | 1 | 1 | 1 | 23 |
| 1 | 1 | 0 | 0 | 0 | 24 |
| 1 | 1 | 0 | 0 | 1 | 25 |
| 1 | 1 | 0 | 1 | 0 | 26 |
| 1 | 1 | 0 | 1 | 1 | 27 |
| 1 | 1 | 1 | 0 | 0 | 28 |
| 1 | 1 | 1 | 0 | 1 | 29 |
| 1 | 1 | 1 | 1 | 0 | 30 |
| 1 | 1 | 1 | 1 | 1 | 31 |

| 2047–20 Headland Tech | 2047–24 Tseng Labs | 2047–30 Cirrus Logic | 2047–35 Tseng Labs | 2047–57 Tseng Labs | 2047–73 NCR | 2047–83 Tseng Labs |
|---|---|---|---|---|---|---|
| 25.175 | 25.175 | 14.318 | 25.175 | 25.175 | 14.318 | 25.175 |
| 28.332 | 28.322 | 16.257 | 28.322 | 28.322 | 16.257 | 28.322 |
| 40.000 | 32.514 | EXTF | 32.500 | 32.514 | EXTF | 36.500 |
| 32.500 | 36.000 | 32.514 | 36.000 | EXTF | 32.514 | 44.900 |
| 50.350 | 40.000 | 25.175 | 40.000 | 40.000 | 25.175 | 59.000 |
| 65.000 | 44.900 | 28.332 | 44.900 | 44.900 | 28.322 | 62.000 |
| 38.000 | 65.000 | 24.000 | 65.028 | 50.000 | 24.000 | 40.000 |
| 44.900 | 84.000 | 40.000 | 84.000 | 62.000 | 40.000 | 47.500 |
| 25.175 | 25.175 | 14.318 | 25.175 | 25.175 | 25.175 | 25.175 |
| 28.332 | 28.322 | 16.257 | 28.322 | 28.322 | 28.322 | 28.322 |
| 80.000 | 40.000 | EXTF | 32.500 | 32.514 | 36.000 | 73.000 |
| 32.500 | 44.900 | 36.000 | 36.000 | 36.000 | 65.000 | 44.900 |
| 50.350 | 32.514 | 25.175 | 40.000 | EXTF | 44.900 | 59.000 |
| 65.000 | 28.322 | 28.332 | 56.000 | 44.900 | 50.000 | 64.000 |
| 76.000 | 36.000 | 24.000 | 44.900 | 50.000 | 56.000 | 40.500 |
| 44.900 | 65.000 | 40.000 | 65.028 | 65.000 | 75.000 | 47.500 |
| 25.175 | 25.175 | 14.318 | 25.175 | 25.175 | 25.175 | 50.350 |
| 44.900 | 28.322 | 65.000 | 28.322 | 28.322 | 28.322 | 56.644 |
| 28.322 | 32.514 | EXTF | 32.500 | 32.514 | 40.000 | 75.800 |
| 38.000 | 36.000 | 36.000 | 36.000 | 36.000 | 65.000 | 45.500 |
| 40.000 | 40.000 | 25.175 | 40.000 | 40.000 | 44.900 | 59.000 |
| 46.000 | 44.900 | 28.332 | 65.028 | 44.900 | 50.000 | 64.000 |
| 48.000 | 56.000 | 24.000 | 44.900 | 50.000 | 56.000 | 80.000 |
| 60.000 | 65.000 | 40.000 | 56.000 | 62.000 | 75.000 | 95.000 |
| 65.000 | 25.175 | 44.900 | 25.175 | 25.175 | 25.175 | 50.350 |
| 72.000 | 28.322 | 50.350 | 28.322 | 28.322 | 28.322 | 56.644 |
| 74.000 | 32.514 | 16.257 | 32.500 | 32.514 | EXTF | 75.800 |
| 76.000 | 40.000 | 32.514 | 40.000 | 36.000 | EXTF | 45.500 |
| 78.000 | 44.900 | 56.644 | 36.000 | 40.000 | 60.000 | 59.000 |
| 80.000 | 60.000 | 20.000 | 44.900 | 44.900 | 80.000 | 64.000 |
| 100.000 | 80.000 | 50.000 | 80.000 | 50.000 | EXTF | 40.500 |
| 110.000 | 84.000 | 80.000 | 84.000 | 65.000 | EXTF | 47.500 |

**NOTE:** There are more ROM tables available, plus specific parts for Macintosh users. Custom ROMs are also available for a nominal fee. Please contact IC DESIGNS for details.

## PC Board Routing Issues

Traditionally, having multiple crystals has allowed the designer to locate them in those places on the board where they are needed. Using a monolithic circuit puts some constraints on the PC board layout to accommodate a single source of all clocks, particularly at the higher pixel clock frequencies above 50MHz.

A full power and ground plane layout should be employed both under and around the IC package. It is important that the ground plane be nearly continuous with a minimum of cuts, holes, or breaks. Both analog and digital ground pins should go directly to this plane.

To produce an output of high spectral purity, additional supply noise precautions might be required, particularly in noisy environments. The power bus should be bypassed to ground with a 0.1µf multi-layer ceramic capacitor and a 2.2µf/10V tantalum capacitor wired in parallel. Both capacitors should be placed within 0.15" of the power pin. A 22 ohm resistor placed between the analog power supply pin (AVDD) and the IC can help to filter noisy supply lines. In extreme situations, deriving power from the +12V supply has been effective. Drop the supply thru 180 ohms to a 5.1V zener diode (1N5231B) to ground.

The designer should also avoid routing the two output traces of the ICD2047 in close parallel proximity. Large routing lengths and large fanouts add capacitance to output drivers. Capacitance affects the rise and fall times of the outputs. Large fanouts should therefore be buffered, particularly for the highest frequencies.

When designing with this device, it is best to locate the ICD2047 closest to the device requiring the highest frequency. If the high-frequency clocks must be routed to board extremes, the ICD2031 distributed 'satellite' oscillators should be considered.

For more details concerning layout and power considerations, please see the IC DESIGNS Application Note *Power Feed and Board Layout Issues*.

## Circuit Description

The oscillator block is a classical phase-locked loop connected as shown in the diagram on the first page. The external input frequency $f_{(REF)}$ is typically 14.31818 MHz (as derived from the PC system bus) and goes into a divide-by-n block. The resultant signal becomes the reference frequency for the phase-locked loop circuitry.

The phase-locked loop is a feedback system which phase matches the reference signal and the variable 'synthesized' signal. The system averages zero phase error between the negative edges arriving at the phase detector. The phase error at the charge pump tells the VCO to either go faster or slower as required. The greater the change in control voltage, the greater the change in the VCO's output frequency. This up and down movement of the variable frequency will ultimately lock on to the reference frequency, resulting in an output oscillation as stable as the input reference. An internal loop filter provides stability and damping.

## Minimized Parasitic Problems

The ICD2047 has been optimized to reduce internal noise and crosstalk problems. The VCO is separated from its digital logic, and separate supply buses for the analog and digital circuitry are used.

## Stability and "Bit-Jitter"



The long-term frequency stability of the IC DESIGNS phase-locked loop frequency synthesis components is good due to the nature of the feedback mechanism employed internally in the design. As a result, stability of the devices is affected more by the accuracy of the external reference source than by the internal frequency synthesis circuits.

Short-term stability (also called "bit-jitter") is a manifestation of the frequency synthesis process. The IC DESIGNS frequency synthesis parts have been designed with an emphasis on reduction of bit-jitter. The primary cause of this phenomenon is the "dance" of the VCO as it strives to maintain lock. Low-gain VCO's and sufficient loop filtering are design elements specifically included to minimize bit-jitter. The IC DESIGNS families of frequency synthesis components are all guaranteed to operate at a jitter rate low enough to be visually unnoticeable in the graphics display.

## Temperature and Process Sensitivity

Because of its feedback circuitry, the ICD2047 is inherently stable over temperature and manufacturing process variations. Incorporating the loop filter internal to the chip assures the loop filter will track the same process variations as does the VCO. With the ICD2047, no manufacturing "tweaks" to external filter components are required as is the case with external de-coupled filters.

## Ordering information

| Part Number | Package Type | Temperature Range | Clock ROM Option |
|---|---|---|---|
| ICD2047 | P = 20–Pin Plastic DIP | C = Commercial (0°C – +70°C) | –20 |
| | C = 20–Pin Ceramic DIP | | –24 |
| | S = 20–Pin SOIC | | –30 |
| | | | –35 |
| | | | –57 |
| | | | –73 |
| | | | –83 |

Example: order *ICD2047PC-30* for a 20–pin plastic DIP, commercial temperature range device which utilizes the *–30* Clock ROM Decode Option. Check with the factory for other Clock ROM Decode Options available but not shown.

# Electrical Data

## Maximum Ratings

| Name | Description | Min | Max | Units |
|---|---|---|---|---|
| VDD | Supply voltage relative to GND | –0.5 | 7.0 | Volts |
| $V_{IN}$ | Input Voltage with respect to GND | –0.5 | VDD + 0.5 | Volts |
| $T_{OPER}$ | Operating Temperature | 0 | +70 | °C |
| $T_{STOR}$ | Storage Temperature | –65 | +150 | °C |
| $T_{SOL}$ | Max Soldering Temperature (10 sec) | | +260 | °C |
| $T_J$ | Junction Temperature | | +125 | °C |
| $P_{DISS}$ | Power Dissipation | | 375 | mWatts |

## DC Characteristics

VDD = +5V ±5%
0°C ≤ $T_{CASE}$ ≤ +70°C

| Name | Description | Min | Max | Units | Conditions |
|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | 2.0 | | Volts | |
| $V_{IL}$ | Low-level input voltage | | 0.8 | Volts | |
| $V_{OH}$ | High-level output voltage | 2.4 | | Volts | $I_{OH}$ = –4.0ma |
| $V_{OL}$ | Low-level output voltage | | 0.4 | Volts | $I_{OL}$ = 4.0ma |
| $I_{IH}$ | Input high current | | 100 | µa | $V_{IH}$ = 5.25V |
| $I_{IL}$ | Input low current | | –250 | µa | $V_{IL}$ = 0V |
| $I_{DD}$ | Power supply current | | 25 | ma | |
| $C_{IN}$ | Input Capacitance | | 10 | pf | |

## AC Characteristics

VDD = +5V ±5%
0°C ≤ $T_{CASE}$ ≤ +70°C)

| Symbol | Name | Description | Min | Max | Units |
|---|---|---|---|---|---|
| $t_1$ | ref freq | Reference Oscillator nominal value | | 14.31818 | MHz |
| $t_2$ | duty cycle | Duty cycle for the output oscillators defined as $t_2/t_1$ | 45% | 55% | |
| $t_3$ | rise time | Rise time for the output oscillators into a 25pf load | | 3 | ns |
| $t_4$ | fall time | Fall time for the output oscillators into a 25pf load | | 3 | ns |
| $t_5$ | clk unstable | Time the output oscillators remain valid after the $P_{0-4}$ select signals change value | | 0 | ns |
| $t_6$ | clk stable | Time required for the output oscillators to become valid after $P_{0-4}$ select signals change value | 0.1 | 15 | msec |