Features

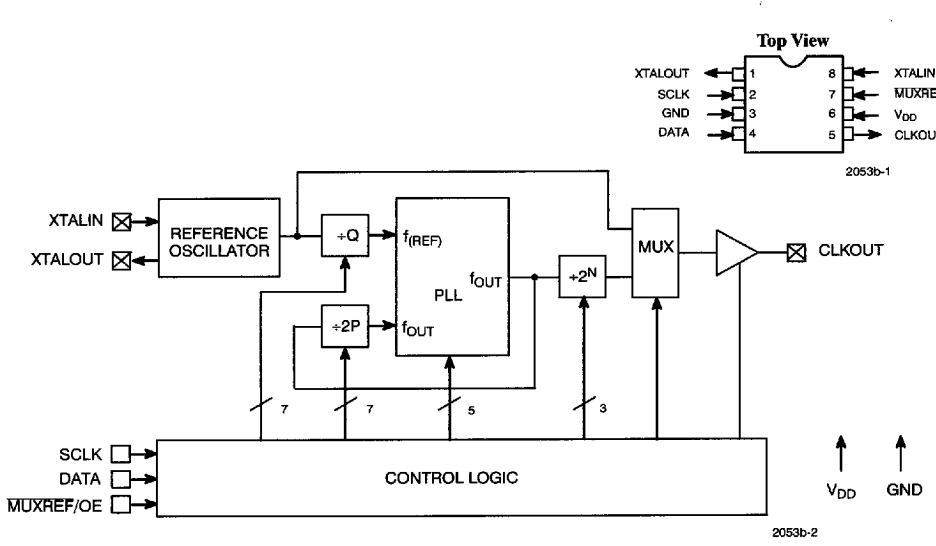
- **Clock outputs ranging from 391 kHz to 100 MHz (TTL levels) or 90 MHz (CMOS levels)**
- **2-wire serial interface facilitates programmable output frequency**
- **Phase-Locked Loop oscillator input derived from external reference clock (1 MHz to 25 MHz) or External Crystal (2 MHz to 24 MHz)**
- **Three-State output control disables output for test purposes**
- **Sophisticated internal loop filter requires no external components or manufacturing tweaks as commonly required with external filters**
- **Low power consumption makes device ideal for power- and space-critical applications**
- **8-pin 150-mil packaging achieves minimum footprint for space-critical applications**
- **5V operation**
- **High-speed CMOS technology**

Functional Description

The ICD2053B Programmable Clock Generator offers a fully user-programmable phase-locked loop in a single 8-pin package. The output may be changed "on the fly" to any desired frequency value between 391 kHz and 100 MHz (90 MHz at CMOS levels). The ICD2053B is ideally suited for any design in which package size, power, and/or frequency programmability are important design issues.

The ability to dynamically change the output frequency adds a whole new degree of freedom for the designer. Some examples of the uses for this device include: laptop computers, in which slowing the speed of operation can mean less power consumption; graphics board dot clocks to allow dynamic synchronization of different brands of monitors or display formats; on-board test strategies where the ability to skew a system's desired frequency (e.g., ±10%) allows worst-case evaluation.

Logic Block Diagram



Pin Configuration

Pin Summary

Name	Number	Description
XTALOUT[1, 2]	1	Reference crystal feedback
SCLK	2	Serial clock input line for programming purposes
GND	3	Ground
DATA	4	Serial data input line for programming purposes
CLKOUT	5	Programmable clock output
V_{DD}	6	+5 volts
MUXREF/OE	7	If bit 3 (Pin 7 Usage) in the Control register is set to 1, this input pin controls the multiplexed reference frequency function. The operation is defined in *Table 1* If bit 3 (Pin 7 Usage) in the Control Register is set to 0, this input pin controls the three-state output function. The operation is defined in *Table 1* On power-up, pin 7 implements the OE function. An internal pull-up allows pin to be not-connected.
XTALIN[1, 2]	8	Reference crystal input or external reference input ($f_{(REF)}$)

ICD2053B Registers

The ICD2053B contains two registers, Control and Program.

These registers are written using a protocol which uses a Protocol word = 011110 to distinguish Control register data from Program register data. This Protocol word is recognized by the four sequential 1s; therefore, all other data sent must have a 0 bit stuffed in after each sequence of three sequential 1s (whether originally followed by a 1 or a 0). This is called bit-stuffing.

Please see the example under "Program Register Example" and the "Frequency Modification Procedure" section. Following is a bit-stuffing example (read right to left, LSB to MSB):

To send this programming data: 1111 0111 1110 111111
Transmit this serial bit stream: 10111 00111 01110 01110111

All serial words are shifted in bit-serially starting with the LSB. A low-to-high transition on SCLK is used to shift data. Whenever the Protocol word is detected, the preceding 8 bits are transferred into the Control register. The control command is then immediately executed.

Control Register

The Control register is used to control the non-frequency setting aspects of the ICD2053B. It is an 8-bit register, which is defined as shown in *Figure 1* and *Table 1*.

At power-up, the Control register is loaded with 0000 0100. This means that the MUXREF Control field is set to 1, forcing the CLKOUT to equal the reference frequency. Additionally, the other fields in the Control register specify that the Program register is disabled from loading, and the internal three-state is disabled.

7	6	5	4	3	2	1	0
0 (Reserved)	0 (Reserved)	Duty Cycle Adjust (Set to 1)	0 (Reserved)	Pin 7 Usage	MUXREF Control	OE Control	Enable Program Word

Figure 1. Control Register

Notes:
1. For best accuracy, use a parallel-resonant crystal.
2. Assume $C_{LOAD} \approx 17$ pF.

Table 1. Control Register

Bit	Definition
RESERVED	For future use. Set to 0.
Duty Cycle Adjust	Set to 1 to reduce duty cycle by approximately 0.7 ns. Normally set to 1.
Pin 7 Usage	Definition of whether pin 7 is $\overline{\text{MUXREF}}$ or OE input pin 0 = Pin 7 is OE input (default) 1 = Pin 7 is $\overline{\text{MUXREF}}$ input
MUXREF Control	Allows internal control of MUXREF. If enabled, this feature automatically multiplexes the reference frequency to the CLKOUT output. This is used to change output glitch-free to new frequencies. 0 = CLKOUT is VCO frequency 1 = CLKOUT is $f_{(REF)}$ (default)
OE Control	Forces the CLKOUT output into a three-state mode 0 = CLKOUT is VCO frequency or $f_{(REF)}$ (default)(depending on current MUXREF state) 1 = CLKOUT is three-stated
Enable Program Word	Enable Program word loading into Program register. When enabled, the Program word may be shifted in. This permits changing the Control register without disturbing Program register data. 0 = Program register is disabled from loading (default) 1 = Program register is enabled to receive data

Program Register

The Program register can be loaded with a 22-bit programming word, the fields of which are defined in *Table 2.*

Table 2. Program Register

Field	# of Bits	Notes
P Counter value (P')	7	MSB (Most Significant Bits)
Duty Cycle Adjust Up (D)	1	Set to logic 1 to increase duty cycle by approx. 0.7 ns. Normally set to 1.
Mux (M)	3	
Q Counter value (Q')	7	
Index (I)	4	LSB (Least Significant Bits)

The VCO frequency, $f_{(VCO)}$, is determined by the following relation:

$f_{(VCO)} = (2 * f_{(REF)} * P/Q)$

where $P' = P - 3$

$Q' = Q - 2$

$f_{(REF)}$ = Reference frequency (1 MHz to 25 MHz)

The value of $f_{(VCO)}$ must remain between 50 MHz and 150 MHz. Therefore, for output frequencies below 50 MHz, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO Divisor is selected by setting the values of the Mux field (M) as follows:

Mux Field (M)

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The index field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 3.* (Note that this table is referenced to the VCO frequency $f_{(VCO)}$ rather than to the desired output frequency and that only the MSB is significant.)

Table 3. Index Field (I)

I	$f_{(VCO)}$ @ 5V
0000	50 to 80 MHz
1000	80 to 150 MHz

To assist with these calculations, Cypress/IC Designs provides the BITCALC program. BITCALC is a Windows™ program for the IBM PC which automatically generates the appropriate programming word from the user's reference input and desired output frequencies.

VCO Programming Constraints

There are seven primary programming constraints the user must be aware of:

Table 4. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	50 MHz	150 MHz
divisor	1	128
f_{OUT}	50 MHz/128	100 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability and factors affecting the loop equation. The factors are listed for completeness sake; however, by using the above-mentioned BITCALC program, these constraints become transparent.

PROGRAM Register Example

The following is an example of the calculations BITCALC performs:

Derive the proper programming word for a 39.5 MHz output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz < 50 MHz, double it to 79.0 MHz. Set M to 001 to post divide by 2. Set I to 1000. The result:

$f_{(VCO)} = 79.0 = (2 * 14.31818 * {}^{P}/_{Q})$

${}^{P}/_{Q} = 2.7587$

Several choices of P and Q are available for this example:

P	Q	$f_{(VCO)}$	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9969	419

Normally, one would choose (P,Q) = (80,29) for the best accuracy (40 PPM). However, we will choose (P,Q) = (91,33) as it illustrates bit stuffing.

Therefore:

P' = P − 3 = 91 − 3 = 88 = 1011000
Q' = Q − 2 = 33 − 2 = 31 = 0011111

The programming word, W, is generated by first creating the non-bit-stuffed word W' by concatenating P'=1011000, D=1, M=001, Q'=0011111, I=1000, and then bit-stuffing.

W' = 1011000 1 001 001 0011111 1000
W = 10110001001000111011000

Zeros were stuffed in two places in this example.

Output Frequency Accuracy

The accuracy of the ICD2053B output frequency depends on the target output frequency and reference frequency. As stated previously, the output frequency of the ICD2053B is mathematically related to the input reference frequency:

$f_{(OUT)} = (2 * f_{(REF)} * {}^{P}/_{Q}) \div 2^{n}$, n = 0...7.

Only certain output frequencies are possible for a particular reference frequency. However, the ICD2053B generally produces an output frequency within 0.1% of the desired output frequency. Specifics regarding accuracy (in ppm) are given for any desired output frequency in the BITCALC program output.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
Input Voltage ..... −0.5V to V_{DD}+0.5
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Max. Soldering Temperature (10 sec) ..... +260°C
Junction Temperature ..... +125°C

Note:
3. Static sensitive <2000V.

Frequency Modification Procedure

When changing to a new frequency, there is a period of time during which the output signal will be in transition and could jump in frequency, or glitch due to changes in the post divider. For applications in which it is critical that the output clock not glitch and always maintain some known value, the MUXREF feature in the Control register should be used. MUXREF causes the reference clock to be multiplexed, glitch-free, to the output clock. The output will remain at this fixed frequency while the VCO seeks its new programmed value.

The procedure for programming the ICD2053B to an initial or new frequency is as follows:

1. Load the Control register to enable MUXREF and enable loading of the Program register. This will set the output to the reference frequency. The transition is guaranteed to be glitch-free. (See timing specifications.) Note that the Protocol Word must precede the Control register data. Also note that all data is shifted in LSB (Least Significant Bit) first.

   Control word = 0 1 1 1 1 0 (Protocol Word) 0 0 0 0 X 1 0 1 ← LSB (Control Reg. Data)

   The state of the Pin 7 Usage bit is defined by the user, and so is denoted as X.
2. Shift in the desired output frequency value computed via a 22-bit data word (as defined above), plus any bit-stuffs (as defined above). Remember to bit-stuff a 0 after any three sequential 1s.
3. Load the Control register to enable MUXREF and disable loading of the Program register. This loads the Program word bits into the Program register and keeps the output set to the reference frequency while the new frequency settles.

   Control word = 0 1 1 1 1 0 (Protocol Word) 0 0 0 0 X 1 0 0 (Control Reg. Data)
4. Wait for VCO to settle in the new state (10 ms to within 0.1% of the new frequency).
5. Load the Control register to enable new frequency output. The transition is guaranteed to be glitch-free. (See the timing specifications.)

   Control word = 0 1 1 1 1 0 (Protocol Word) 0 0 0 0 X 0 0 0 (Control Reg. Data)

Package Power Dissipation ..... 400 mW
Static Discharge Voltage ..... Class 1[3] (per MIL-STD-883, Method 3015)

Operating Range

Range	Ambient Temperature	V_{DD}
Commercial	0°C to +70°C	5V ± 10%

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage	4.5	5.5	V
T_A	Ambient Operating Temperature	0	70	°C
C_L	Load Capacitance		25	pF

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{OH}	HIGH-level Output Voltage	I_{OH} = 4.0 mA	2.4		V
V_{OL}	LOW-level Output Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	HIGH-level Input Voltage	Except XTALIN pins	2.0		V
V_{IL}	LOW-level Input Voltage	Except XTALIN pins		0.8	V
V_{IH}	HIGH-level Reference Input Voltage, when DC coupled[4]	XTALIN pin only	$V_{DD}-0.8$		V
V_{IL}	LOW-level Reference Input Voltage, when DC coupled[4]	XTALIN pin only		0.8	V
I_{IH}	Input HIGH Current	V_{IN} = 5.0V, except SCLK		100	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, except SCLK		−250	µA
I_{IH}	Input HIGH Current	V_{IN} = 5.0V, SCLK only		250	µA
I_{IL}	Input LOW Current	V_{IN} = 0.5V, SCLK only		−100	µA
I_{OZ}	Output Leakage Current	Three-state		10	µA
I_{DD}	Power Supply Current	$V_{DD}=V_{DD}$ max., 100 MHz, $V_{IN}=V_{DD}$ or 0V	13	50	mA

Capacitance

Parameter	Description	Max.	Unit
C_{IN}	Input Capacitance, except XTALIN pin	10	pF
C_{IN}	Input Capacitance, XTALIN pin	34	pF

Switching Characteristics Over the Operating Range

Parameter	Name	Description		Min.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value[4]		1	25	MHz
$t_{(REF)}$	Reference Clock Period	$t_{(REF)} = 1/f_{(REF)}$		40	1000	ns
t_1	Reference Clock HIGH Time	Input pulse width HIGH for reference. Measured at $V_{DD}/2$, DC coupled.[4]		16		ns
t_2	Output Period	CLKOUT period (frequency), TTL levels		10 (100 MHz)	2560 (391 kHz)	ns
		CLKOUT period (frequency), CMOS levels		11.1 (90 MHz)	2560 (391 kHz)	
t_3	Output Duty Cycle (t_0/t_2)	Duty cycle of CLKOUT measured at 1.4V (TTL) threshold	$f_{(OUT)}$ < 50 MHz AND post-divide ≥ 2	45%	55%	
			$f_{(OUT)}$ > 50 MHz OR post-divide = 1	40%	60%	
		Duty cycle of CLKOUT measured at $V_{DD}/2$ (CMOS) threshold	post-divide ≥ 2	45%	55%	
			post-divide = 1	40%	60%	
t_4	Rise Time	Rise time for the clock output into a 25 pF load	TTL 0.4V to 2.4V		3	ns
			CMOS, 0.1V_{DD} to 0.9V_{DD}		6	

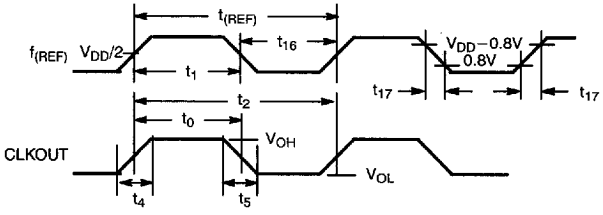
Note:
4. See *Externally Driven Crystal Oscillator* Application Note. For AC coupling, use an input duty cycle near 50%.

Switching Characteristics Over the Operating Range (continued)

Parameter	Name	Description		Min.	Max.	Unit
t_5	Fall Time	Fall time for the clock output into a 25 pF load	TTL 0.4V to 2.4V		3	ns
			CMOS, 0.1V_{DD} to 0.9V_{DD}		6	
t_6	SCLK Cycle Time	Minimum cycle time for the SCLK clock		2 * $t_{(REF)}$		ns
t_7	Clock Valid	Time required for the CLKOUT oscillator to become valid after last SCLK clock[5]		$t_{(REF)}$	3 * $t_{(REF)}$ + 25	ns
t_8	Serial Data Set-up	Time required for the data to be valid prior to the rising edge of SCLK		15		ns
t_9	Hold	Time required for the data to remain valid after the rising edge of SCLK		0		ns
t_{10}	Delay, MUXREF[6] Asserted to CLKOUT HIGH	Time for CLKOUT to go HIGH after assertion of MUXREF[6]		0	t_{old} + 25	ns
t_{11}	Transition, $f_{(OLD)}$ to $f_{(REF)}$	Delay of first falling edge of $f_{(REF)}$ signal at output		t_{13}	$t_{(REF)}$ + 25	ns
t_{12}	Reference Output High Time	Output during MUXREF[6], reference DC coupled		t_{16} − 10	t_{16} + 10	ns
t_{13}	Reference Output Low Time	Output during MUXREF[6], reference DC coupled		t_1 − 10	t_1 + 10	ns
t_{14}	Transition, $f_{(REF)}$ to $f_{(NEW)}$	Time for CLKOUT to go HIGH after release of MUXREF[6]		0	$t_{(REF)}$ + 25	ns
t_{15}	Transition, MUXREF[6] released to CLKOUT LOW	Delay of first falling edge of $f_{(NEW)}$ signal at output		t_{new}/2	t_{new} * 3/2 + 25	ns
t_{16}	Reference Clock Low Time	Input pulse width low for reference. Measured at V_{DD}/2, DC coupled[4]		18		ns
t_{17}	Reference Input Rise/Fall	Rise/fall time for DC coupled reference input[4]			$t_{(REF)}$/10	ns
t_{18}	Output Enable Delay	Delay from Output Enable HIGH to Output Valid		0	20	ns
t_{19}	Output Disable Delay	Delay from Output Enable LOW to Output Floating		0	20	ns
t_{old}	Original Period	Output period before reprogramming, $1/f_{(OLD)}$				
t_{new}	New Period	Output period after reprogramming, $1/f_{(NEW)}$				
t_{lock}	VCO Lock Time	Time for VCO to lock onto new $f_{(VCO)}$ within 0.1%			10	msec

Switching Waveforms

Rise and Fall Times



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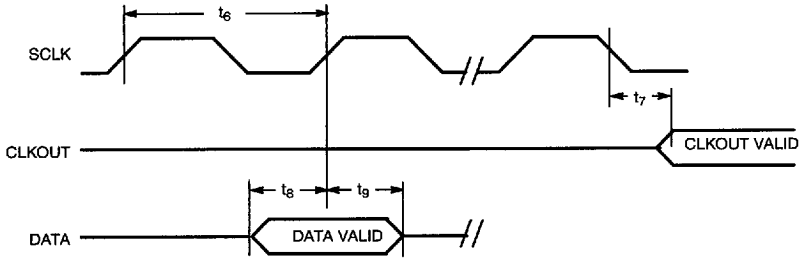
Notes:
5. This is the time for the serial word shifted in to take effect, including the Control Word output enable bit. The VCO stabilization time is separate.
6. Pin or internal bit.

Switching Waveforms (continued)

Serial Programming Timing



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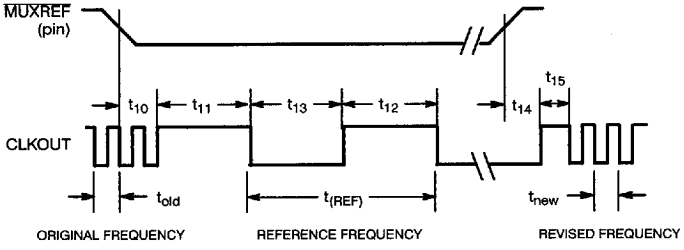
MUXREF Timing[7]



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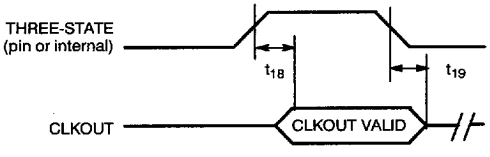
Three-State Timing



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Ordering Information

Ordering Code	Package Name	Package Type	Operating Range
ICD2053B	S8	8-Pin (150-Mil) SOIC	Commercial[8]

Notes:
7. Identical behavior is exhibited when the internal MUXREF bit in the Control register is HIGH.
8. 0°C to +70°C

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