Integrated Circuit Systems, Inc.

ICS1561

T-52-33-49

Differential Output Video Dot Clock Generator

Features

- High frequency operation for extended video modes - up to 180 MHz
- Compatible with Brooktree high performance RAMDACs™
- Low Cost - Eliminates need for multiple ECL crystal clock oscillators in video display subsystems
- Strobed /Transparent frequency select options
- Mask-programmable frequencies
- Fast acquisition of selected frequencies, strobed or non-strobed
- Advanced PLL for low phase-jitter
- Dynamic control of VCO sensitivity providing optimized loop gain over entire frequency range
- Small footprint - 20 pin DIP or SO

Applications

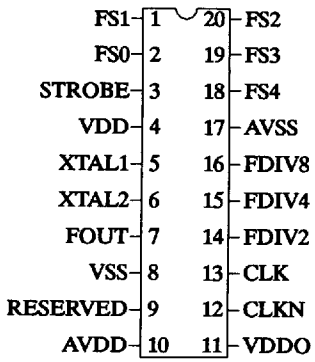
- Workstations
- High resolution MACII displays
- EGA - VGA - Super VGA video adapters
- 8514A - TMS 34010 - TMS 34020

B

Description

The ICS1561 Dot Clock Generator is an integrated circuit capable of generating up to 32 video dot clock frequencies for use with high performance video display systems. Utilizing CMOS technology to implement all linear, digital and memory functions, the ICS1561 provides a low power, small footprint, low cost solution to the generation of video dot clocks. Output frequencies are compatible with VGA, EGA, MCGA, CGA, MDA, as well as the higher frequencies needed for advanced applications in desktop publishing and workstation graphics. Provision is made via a single level custom mask to implement customer specific frequency sets. Phase-locked loop circuitry permits rapid glitch-free transitions between clock frequencies. The ICS1561 provides positive ECL outputs compatible with RAMDAC™ clock and clock* inputs. TTL compatible clocks at 1, 1/2, 1/4, and 1/8 the primary clock frequency facilitate the interfacing of video DRAM to the system.

Pin Configuration

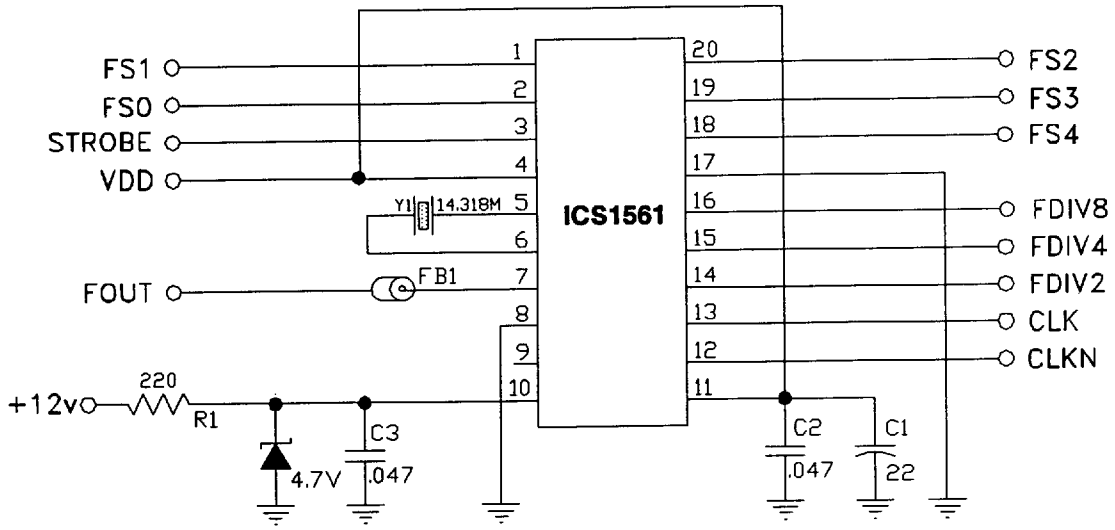


Top View

Ordering Information
ICS1561NXXX (DIP Package)
ICS1561MXXX (SO Package)
(XXX = Pattern number)

ICS1561

Connection Diagram

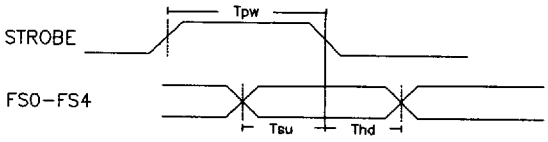


Circuit and Application Options

Digital Inputs

FS0 (2), FS1 (1), FS2 (20), FS3(19), and FS4(18) are the TTL compatible frequency select inputs for the binary code corresponding to the frequency desired. **STROBE (3)**, when high, allows new data into the frequency select latches; and, when low, prevents address changes. The internal power-on-clear signal will force an initial frequency code corresponding to an all zeros input state.

ICS tailors the upper frequency limits of the **ICS1561** to satisfy the frequency requirements of the application. This prevents frequency excursions of the dot clock beyond the capabilities of the graphics chipset.



Applications

Layout Considerations

Utilizing the **ICS1561** in video graphics applications is simple, but does require precautions in board layout if satisfactory jitter-free performance is to be realized. A low series inductance bypass capacitor of .047μF should be utilized between digital Vss (8) and V_{DD} (4). AVss (17) should be connected to ground at the card edge connector, and care should be exercised in ensuring that components not related to the **ICS1561** do not use this ground. In applications utilizing a multi-layer board, both AVss and Vss should be directly connected to the ground plane. In a 5 Volt only system, AV_{DD} should be isolated from V_{DD} with a 100 Ω resistor and should be decoupled with a 2.2μF tantalum capacitor in parallel with a .047μF ceramic capacitor. The .047μF ceramic should be physically close to AV_{DD} as is practical, to ensure low lead inductances between AV_{DD} and AVss. A 4.7 Volt zener diode and an appropriate dropping resistor to power the analog circuitry may be used instead of the 2.2 μF tantalum capacitor. This should be connected to the +12 volt supply, and will provide improved noise rejection and require less board space. The .047 μF capacitor should still be utilized to provide high frequency bypassing. **CLK and CLKN connections to the RAMDAC™ should follow good ECL interconnection practice. Terminating resistors should be as close as possible to the RAMDAC™.**

Pin Functions

Pin Name	Pin Number	Description
FS0	2	- Frequency select input, TTL compatible (LSB)
FS1	1	- Frequency select input, TTL compatible
FS2	20	- Frequency select input, TTL compatible
FS3	19	- Frequency select input, TTL compatible
FS4	18	- Frequency select input, TTL compatible (MSB)
STROBE	3	- Negative edge clock for select inputs, TTL compatible
F_{OUT}	7	- Clock output, TTL compatible
XTAL1	5	- Crystal Interface / Ext. oscillator input
XTAL2	6	- Crystal Interface
V_{DD}	4	- 5 Volt power pin
AV_{DD}	10	- Analog V_{DD} input
V_{SS}	8	- Digital ground
AVss	17	- Analog ground
Phaseout	9	- Phase comparator output
CLOCK	13	- Clock output, positive ECL
CLOCKN	12	- Complementary clock output, positive ECL
F_{DIV2}	14	- Clock/2 output, TTL compatible
F_{DIV4}	15	- Clock/4 output, TTL compatible
F_{DIV8}	16	- Clock/8 output, TTL compatible
V_{DD0}	11	- Output stage V_{DD} supply pin

ICS1561

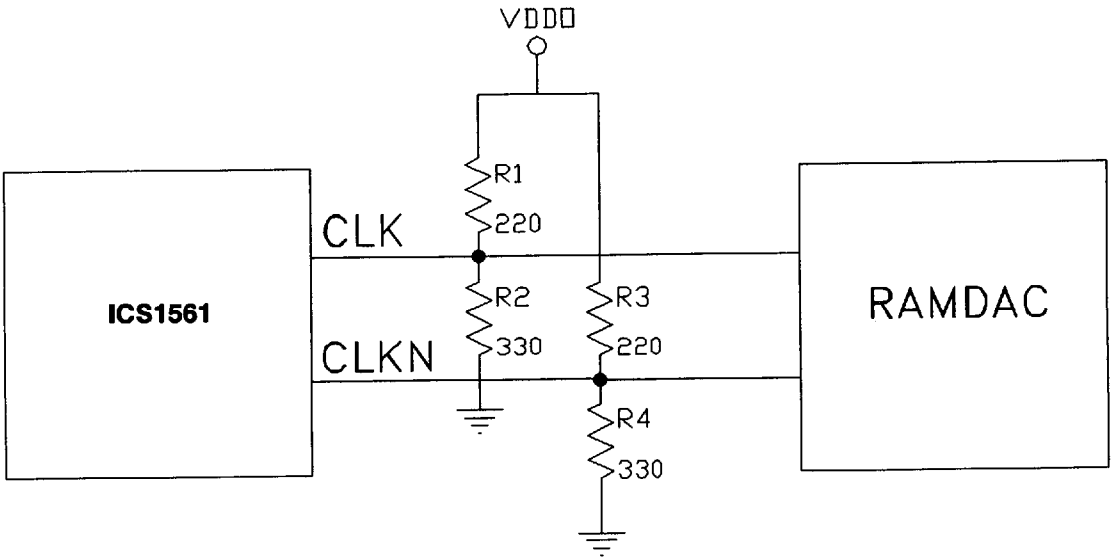
Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate series resonant crystal should be connected between **XTAL1 (5)** and **XTAL2 (6)**. In IBM™-compatible applications this will typically be a 14.31818 MHz crystal, but crystals between 5MHz and 25 MHz may be used. Maintain short lead lengths between the crystal and the **ICS1561**. In some applications, it may be desirable to utilize the bus clock. To do this, connect the clock through a .047uF capacitor to **XTAL1 (5)** and keep the lead length of the capacitor to XTAL1 (5) to a minimum to reduce noise susceptibility. This input is internally biased at $V_{DD/2}$. Since TTL compatible clocks typically exhibit a V_{OH} of 3.5V, capacitively coupling the input restores noise immunity. The **ICS1561** is not sensitive to the duty cycle of the bus clock; however, the quality of this signal varies considerably with different motherboard designs. As the quality of the bus clock is typically outside the control of the graphics adapter card manufacturer, it is suggested that this signal be buffered on the graphics adapter board. **XTAL2 (6)** must be left open in this configuration.

Output Circuit Considerations

The **CLK** and **CLKN** outputs are each connected to the drains of P-Channel MOSFET devices. The source of each of these devices is connected to V_{DDO}. Typical on resistance of each device is 15 Ohms. Typically, these outputs will drive the clock and clock* of a RAMDAC™ device. The inputs of the RAMDAC™ should have a 220 ohm resistor connected to +5V and a 330 ohm resistor connected to ground as physically close to the RAMDAC as practical.

Typical Output Configuration



NOTE: RAMDAC is a trademark of Brooktree Corporation.

Absolute Maximum Ratings

Ambient Temperature under bias ..... T_o ..... 0 °C to 70 °C
Supply Voltage ..... V_{DD} ..... -0.5V to +7V
Input Voltage ..... V_{IN} ..... -0.5V to V_{DD} +0.5V
Output Voltage ..... V_{OUT} ..... -0.5V to V_{DD} +0.5V
Clamp Diode Current ..... V_{IK} & I_{OK} .... +/-30mA
Output Current per Pin ..... I_{OUT} ..... +/-50mA
Storage Temperature ..... T_S ..... -85 °C to +150 °C
Power Dissipation ..... P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than the maximum rated voltages. For proper operation it is recommended that V_{IN} and V_{OUT} be constrained to $>= V_{SS}$ and $<= V_{DD}$.

B

DC Characteristics (Power Supply Voltage 4.75- 5.25 Volts)

SYMBOL	PARAMETER	MIN	MAX	UNITS	CONDITIONS
V_{IL}	Input Low Voltage	V_{SS}	0.8	V	V_{DD} = 5V
V_{IH}	Input High Voltage	2.0	V_{DD}	V	VDD = 5V
I_{IH}	Input Leakage Current	-	10	u A	V_{in} = V_{DD}
V_{OL}	Output Low Voltage	-	0.4	V	I_{OL} = 8.0 mA
V_{OH}	Output High Voltage	2.4	-	V	I_{OH} = 4.0 mA
I_{DD}	Supply Current	-	30	mA	V_{DD} = 5V
R_{UP}	Internal Pullup Resistors	25	100	K ohms	V_{DD} = 5V
C_{in}	Input Pin Capacitance	-	8	pF	F_C = 1 MHz
C_{out}	Output Pin Capacitance	-	12	pF	F_C = 1 MHz

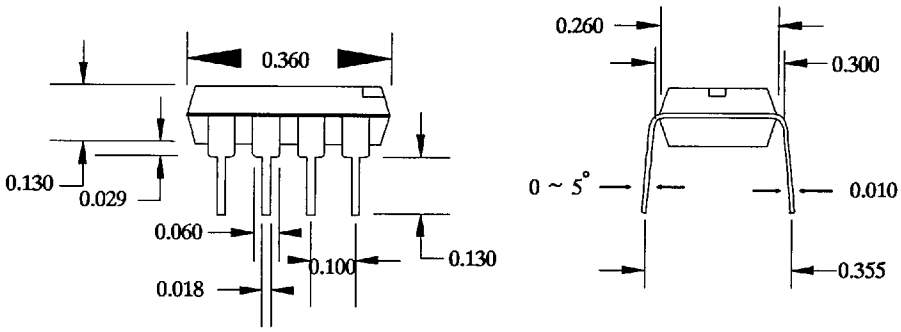
AC Timing Characteristics

The following notes apply to all of the parameters presented in this section:
1. REFCLK = 14.318 MHz
2. All units are in nanoseconds (ns).
3. Rise and fall time is between 0.8 and 2.0 VDC for TTL I/O.
4. Output pin loading = 25pF.
5. Duty cycle is measured at 1.4V for TTL I/O.

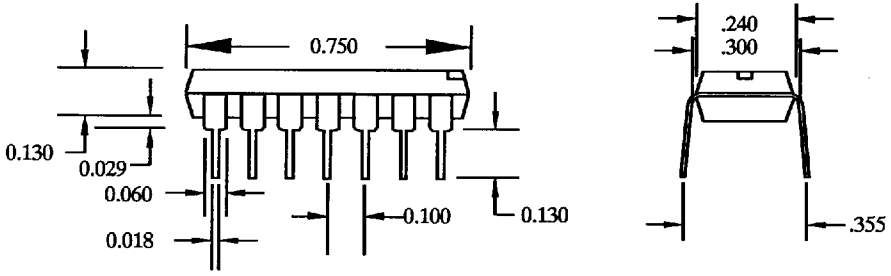
SYMBOL	PARAMETER	MIN	MAX	NOTES
	Strobe Timing			
T_{strobe}	Strobe Pulse Width	20	-	
T_{su}	Setup Time Data to Enable	20	-	
T_{hd}	Hold Time Data to Enable	10	-	
	Reference Input Clock			
Tr	Rise Time	-	10	
Tf	Fall Time	-	10	
	CLK and CLK Timings			
Tr	Rise Time	-	3	ns
Tf	Fall Time	-	3	Duty Cycle 40% min. to 60% max.
-	Frequency Error		0.5	%
-	Maximum Frequency		180	MHz

T-90-20

DIP Packages



8 Pin DIP Package



14 Pin DIP Package

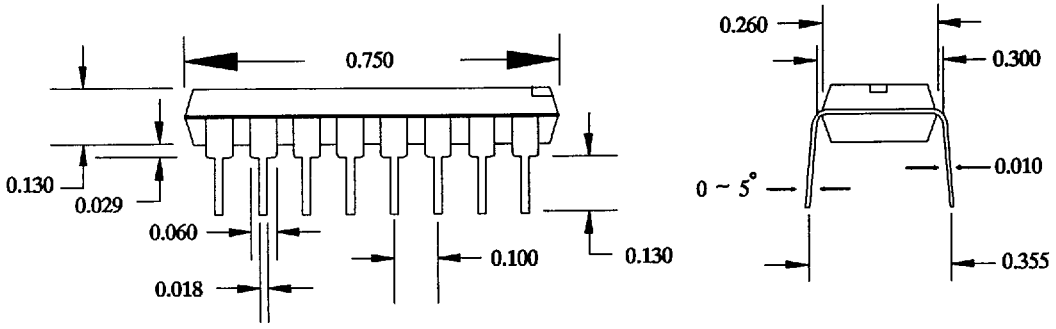
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

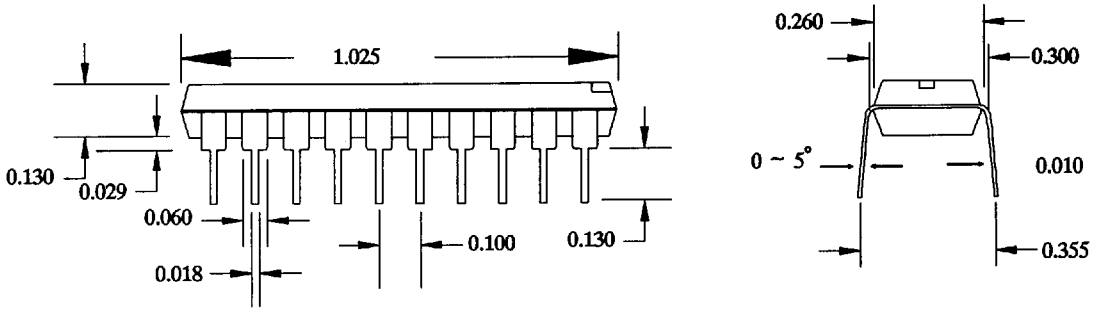
Example: ICSXXXXN

H

DIP Packages



16 Pin DIP Package



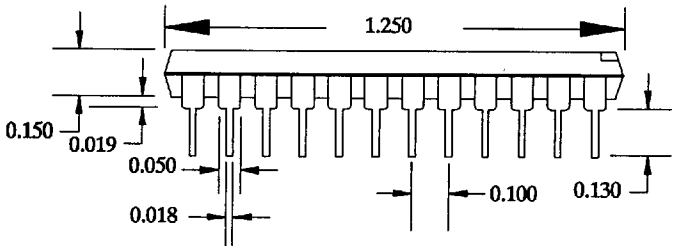
20 Pin DIP Package

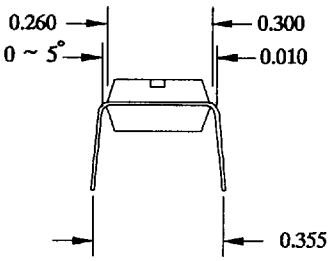
Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

DIP Packages





24 Pin DIP Package

Ordering Information:

All ICS devices in DIP packages carry an "N" designation. See individual data sheets for more specific information.

Example: ICSXXXXN

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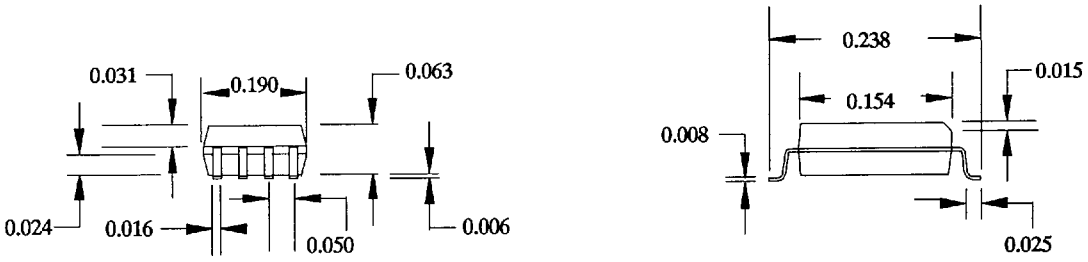
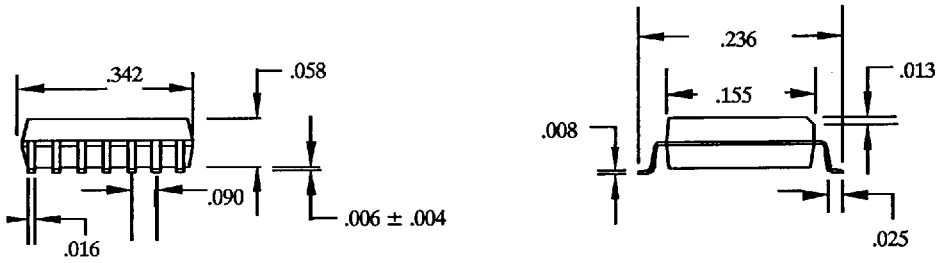
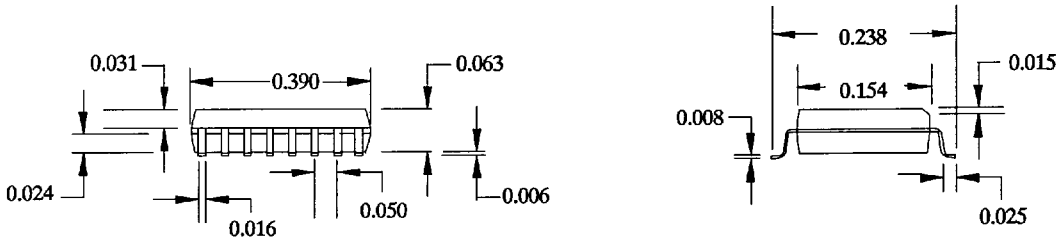
SO Packages



8 Pin SO Package



14 Pin SO Package



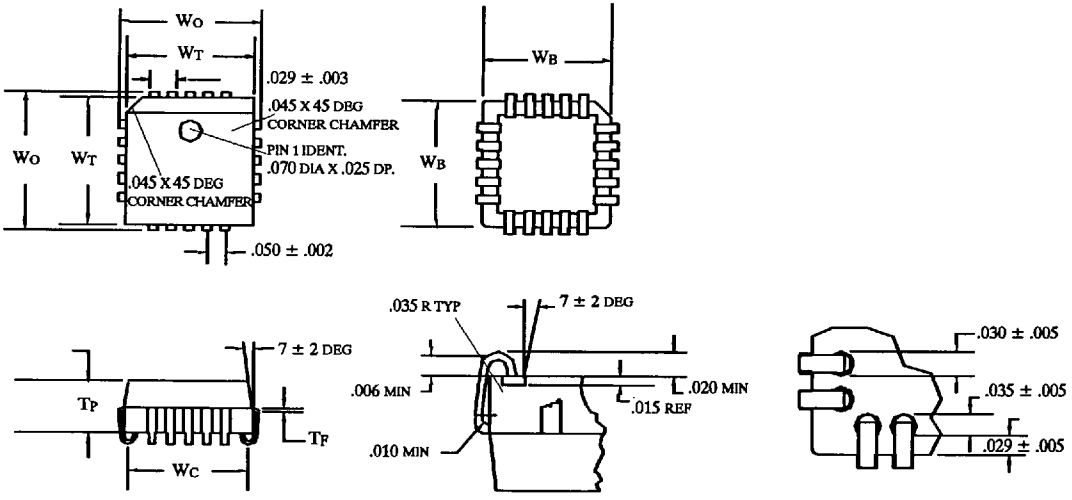
16 Pin SO Package

Ordering Information:

All ICS devices in SO packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM

PLCC Packages



LEAD COUNT	FRAME THICKNESS T_F +/-.0003	PKG. THICKNESS T_P +/-.004	PKG. WIDTH TOP W_T +/-.004	PKG. WIDTH BOTTOM W_B +/-.066	OVERALL PKG. WIDTH W_O +/-.005	CONTACT WIDTH W_O +.010/-.030
20L	0.010	0.152	0.350	0.323	0.390	0.320
28L	0.010	0.152	0.450	0.423	0.490	0.420
44L	0.010	0.152	0.650	0.623	0.690	0.620
52L	0.010	0.152	0.750	0.723	0.790	0.720
68L	0.008	0.150	0.950	0.923	0.990	0.920
84L	0.008	0.150	1.160	1.123	1.190	1.120

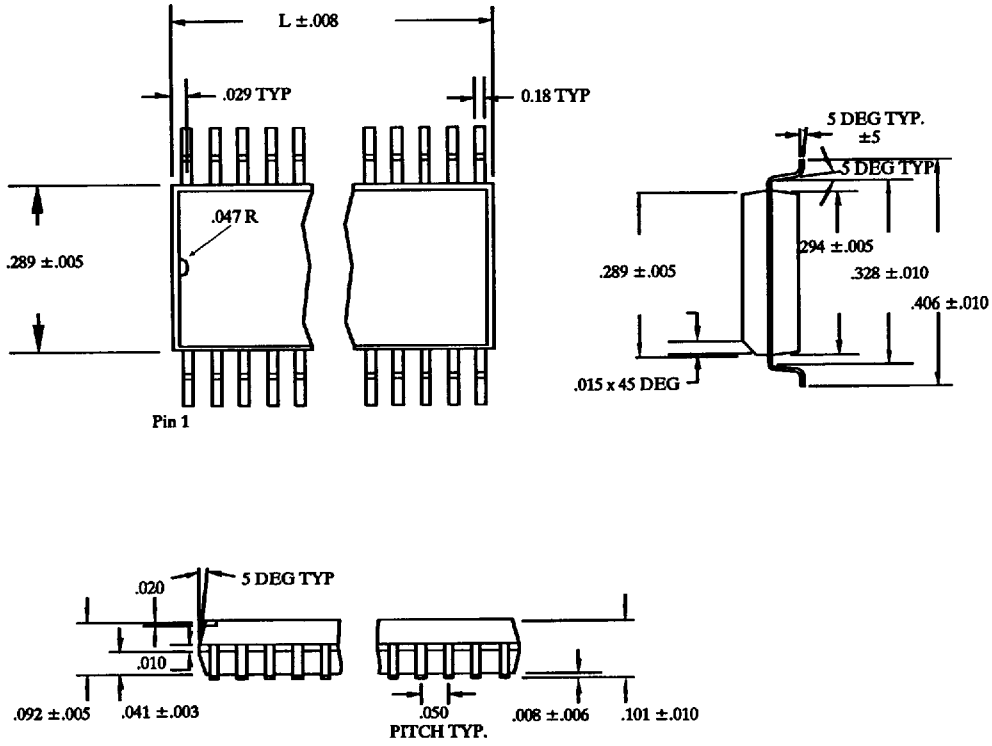
Ordering Information:

All ICS devices in PLCC packages carry a "V" designation. See individual data sheets for more specific information.

Example: ICSXXXXV

H

SOIC Packages



SOIC Packages (wide body)

LEAD COUNT	14L	16L	18L	20L	24L	28L	32L
DIMENSION L	.354	.404	.454	.504	.604	.704	.704

Ordering Information:

All ICS devices in SOIC packages carry an "M" designation. See individual data sheets for more specific information.

Example: ICSXXXXM