Integrated Circuit Systems, Inc.

# ICS2102

# Sound Blaster™ Compatible Mixer

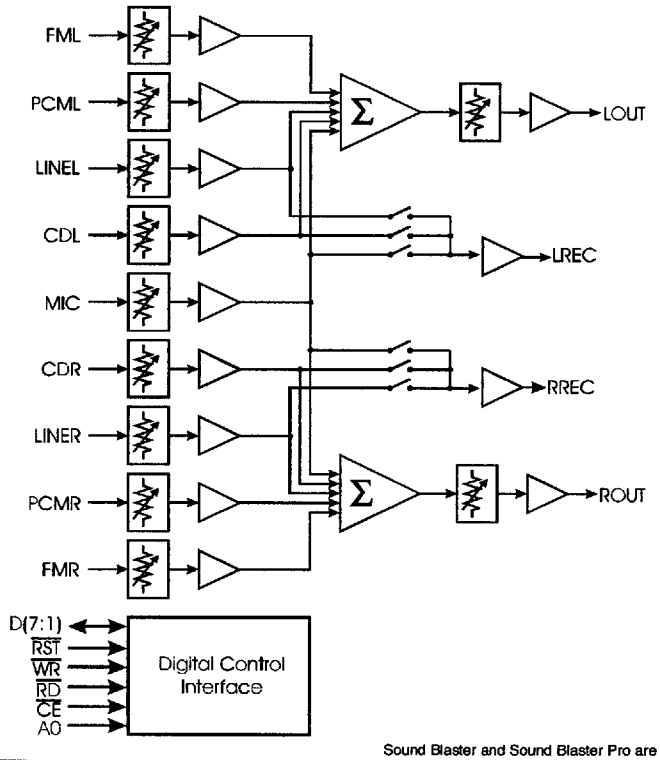
## General Description

The **ICS2102** is a CMOS integrated circuit that provides mixing of 4 stereo and 1 monaural audio signals as well as master volume control. These functions are digitally controlled through Sound Blaster compatible mixer registers, an 8 bit parallel interface. The monaural microphone input has 4 levels of attenuation. The remaining 8 input channels have 8 levels of attenuation. The four stereo channels and one monaural channel are summed to form a composite signal before global volume controls are added. The master volume may be programmed with one of 8 levels of attenuation. This component performs all the necessary audio mixing for a product that is compatible with Sound Blaster Pro.™

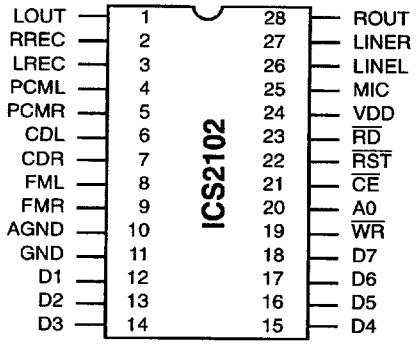
## Features

- 4 channel stereo and 1 monaural mixing
- 8 levels of independent channel input attenuation control, except microphone (4 levels)
- 8 level master volume control
- 5V CMOS process
- 28-pin SOIC package

## Block Diagram



## Pin Configuration




**28-Pin SOIC**

## Pin Descriptions

| PIN NUMBER | PIN NAME | TYPE | DESCRIPTION |
|---|---|---|---|
| 4 | PCML | Analog input | Left PCM input channel. |
| 5 | PCMR | Analog input | Right PCM input channel. |
| 8 | FML | Analog input | Left FM input channel. |
| 9 | FMR | Analog input | Right FM input channel. |
| 6 | CDL | Analog input | Left CD input channel. |
| 7 | CDR | Analog input | Right CD input channel. |
| 26 | LINEL | Analog input | Left line input channel. |
| 27 | LINER | Analog input | Right line input channel. |
| 25 | MIC | Analog input | Microphone input channel. |
| 19 | $\overline{WR}$ | Digital input | Write Enable. |
| 23 | $\overline{RD}$ | Digital input | Read Enable. |
| 21 | $\overline{CE}$ | Digital input | Chip Enable. |
| 22 | RST | Digital input | Hardware Reset. |
| 20 | A0 | Digital input | Address bit 0. |
| 12 | D1 | Digital input | Data bit 1. |
| 13 | D2 | Digital input | Data bit 2. |
| 14 | D3 | Digital input | Data bit 3. |
| 15 | D4 | Digital input | Data bit 4. |
| 16 | D5 | Digital input | Data bit 5. |
| 17 | D6 | Digital input | Data bit 6. |
| 18 | D7 | Digital input | Data bit 7. |
| 1 | LOUT | Analog output | Left audio output. |
| 28 | ROUT | Analog output | Right audio output. |
| 3 | LREC | Analog output | Left record output. |
| 2 | RREC | Analog output | Right record output. |
| 11 | DGND | Power | Digital ground. |
| 10 | AGND | Power | Analog ground. |
| 24 | $V_{DD}$ | Power | Positive supply voltage. |

## Pin Descriptions

**xL, xR**: Left and right channel inputs. These pins are used as the four pairs of inputs for the audio signals to be attenuated and then mixed. The signals applied to these pins should not exceed the supply voltage.

**MIC**: Microphone input. This analog signal is first attenuated and then routed to both left and right channels. It is the only mono input routed to both channels.

**LOUT, ROUT**: Audio output left and right. These pins are connected to buffer amplifiers that are in turn driven from the volume control. This output should be used to drive the amplifier section of the final sound reproduction system.

**LREC, RREC**: A second set of audio outputs used for recording one of three inputs: LINE, CD or MIC. The Input Selection Register determines which source is connected to the LREC and RREC outputs.

**VDD**: Digital and Analog supply. This pin supplies the analog section and digital interface of the mixer and should not be greater than 5V above the analog ground (AGND).

**AGND**: Analog ground. This pin is used as the negative supply of the analog section.

**DGND**: Digital ground. This pin is used as a reference for the digital section of the mixer. The potential at this pin should be externally tied to the chasis ground on the board where AGND is also connected.

**A0**: Address bit 0. This pin, when driven low, determines that the incoming data is an index. When high, the incoming data is data to set the register indicated on the previous data transfer.

**$\overline{WR}$**: Write Pulse (Low Active). The write line is pulsed low while the chip enable line is a low. A 7 bit data load will occur using data pins 1 to 7.

**$\overline{RD}$**: Read Pulse (Low Active). The read line is pulsed low while the chip enable line is low. A 7 bit data read will occur using data pins 1 to 7.

**$\overline{CE}$**: Chip Enable (Low Active). This line should be pulsed low in order to initiate a transfer of control information to the digital control section. If this line and the write line are low, a byte transfer will occur.

**$\overline{RST}$**: Hardware Reset (Low Active). This line resets the default setting of the mixer. The application circuit will use the inverted version of the PC reset line.

**D1-7**: Data bits 1-7: These lines are used for parallel transfers to the digital control section. A parallel transfer occurs when bot the chip enable ($\overline{CE}$) and write pulse ($\overline{WR}$) or read pulse ($\overline{RD}$) lines are low. D0 (LSB), not having any impact on both index (address) decoding or actual data, has been omitted.

## Registers

*Overview*

Communication to each internal register of the mixer requires that two byte transfers are completed. The first byte must contain the index (or address) of the register which is to be loaded. The second byte should contain the data that is to be written. The external address line A0 is used to discriminate between an index write and a data write. If the A0 is set to a logic 0, it is identified as an index transfer and if it is set to a logic 1, then the transfer is identified as data. The data transfer is valid only when /CE pin is pulsed low. In this manner an 8 bit bus with multiple uses can be shared for communication.

## Register Maps

*Address Transfer Definitions*

An address transfer is one in which A0 bit is set to a logic 0, whatever the base address might be. The decode of this address is as follows:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | **Accessed Register** (Hex) |
|---|---|---|---|---|---|---|---|
| Mixer Data Reset | | | | | | | 00/01 |
| Left PCM Input | | | X/1 | Right PCM Input | | | 04/05 |
| | | X/0 | X/1 | X/0 | MIC Input | | 0A/0B |
| | | X/0 | X/1 | X/0 | Input Sel. | | 0C/0D |
| L. Master Volume | | | X/1 | R. Master Volume | | | 22/23 |
| Left FM Input | | | X/1 | Right FM Input | | | 26/27 |
| Left CD Input | | | X/1 | Right CD Input | | | 28/29 |
| Left Line Input | | | X/1 | Right Line Input | | | 2E/2F |

X/1=Ignored on write operations, read back as 1.
X/0=Ignored on write operations, read back as 0.

*Ghost Address Definitions*

Some of the actual registers described on the previous page are duplicated by partial decoding. Omitting certain address bits for decoding, the decode is as follows:

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | Accessed Register (Hex) |
|---|---|---|---|---|---|---|---|
| L. Master V. Ghost | | | X/1 | R. Master V. Ghost | | | 02/03 |
| Left FM Ghost | | | X/1 | "Right" FM Ghost | | | 06/07 |
| Left CD Ghost | | | X/1 | "Right" CD Ghost | | | 08/09 |

*Channel Control Register (except Microphone input)*

| D3/D7 | D2/D6 | D1/D5 | D4 | Function |
|---|---|---|---|---|
| 0 | 0 | 0 | X/1 | Mute this channel |
| 0 | 0 | 1 | X/1 | 28dB attenuation |
| 0 | 1 | 0 | X/1 | 21.5dB attenuation |
| 0 | 1 | 1 | X/1 | 16dB attenuation |
| 1 | 0 | 0 | X/1 | 11dB attenuation |
| 1 | 0 | 1 | X/1 | 7dB attenuation |
| 1 | 1 | 0 | X/1 | 3.3dB attenuation |
| 1 | 1 | 1 | X/1 | 0dB attenuation |

There are 5 control registers in the **ICS2102**. The higher 3 bits of each nibble register selects the desired level of attenuation for that channel. The lowest level of attenuation (or highest volume) corresponds to a setting of all 1s for the attenuation field. Attenuation steps increase at varying dB per step until 28dB is reached with a register value in the attenuation field of 001x. The final step does not simply add an additional 6dB attenuation but acts as a mute function by completely killing the input.

The only exception to this is the Microphone input attenuation control that uses D[2-1] for the 8 levels.

*Microphone Input Control Register*

| D2 | D1 | Function |
|---|---|---|
| 0 | 0 | Mute this channel (Default) |
| 0 | 1 | 19dB attenuation |
| 1 | 0 | 11dB attenuation |
| 1 | 1 | 6dB attenuation |

*Input Selection Register*

| D2 | D1 | Function |
|---|---|---|
| 0 | 0 | Microphone (Default) |
| 0 | 1 | CD Input |
| 1 | 0 | Microphone |
| 1 | 1 | Line-In |

*Default Settings*

The default values are set when the part is powered on. The same default values are also set when a hardware reset (low active, pin $\overline{RST}$) occurs. When reset by writing to 00 index (Data Reset register), the **ICS2102** sets the input attenuations of the FM, PCM inputs and the master volume to 99h, while all others are muted (00h). The recording selector switch connects the microphone input to the recording path.

## Register Descriptions

*Reset Register (Index 00)*

When the PC writes any value to this register, the mixer will reset, and all registers will return to their default values. The reset occurs with a write to this register. The default values will load once the data is also written.

*PCM Volume Register (Index 04)*

The PC uses this register to set the PCM input attenuation level. This register can also be programmed by writing to the lower nibble of index register 24h. When programmed in this way, the lower nibble written will set both the left and right PCM volumes. The default value for this register is 99h.

*MIC Input Attenuation Register (Index 0A)*

The recording volume of the microphone input is set through this register. The setting of the levels is described in a previous table. The default value for this register is 00h.

*Input Selector for Recording (Index 0C)*

The recording of a single channel is defined through the selection described in the previous table.

*Master Volume Register (Index 22)*

The PC uses this register to set the overall volume level. This register can also be programmed via the lower nibble of index register 02h. When programmed this way, the nibble written will set both the left and right master volumes. The default value for this register is 99h.

*FM Volume Register (Index 26)*

The PC uses this register to set the FM input attenuation level. This register can also be programmed by writing to the lower nibble of index register 06h. When programmed this way, the lower nibble will set both the left and right FM volume settings. The default value for this register is 99h.

*CD Volume Register (Index 28)*

The PC uses this register to set the CD input attenuation level. This register can also be programmed by writing to the lower nibble of index register 08h. When programmed this way, the lower nibble will set both the left and right CD volume settings. The default value for this register is 00h.

*Line In Volume Register (Index 2E)*

The PC uses this register to set the line-in input attenuation level. The default value for this register is 00h.

## Ghost Registers

*Master Volume Ghost Register (Index 02)*

When this register is written, the lower nibble (bits 3-0) are written to both the left and right Master volume settings at index register 22h. The default value for this register is 99h.

*FM Volume Ghost Register (Index 06)*

When this register is written, the lower nibble (bits 3-0) are written to both the left and right FM volume settings at index register 26h. The default value for this register is 99h.

*CD Volume Ghost Register (Index 08)*

When this register is written, the lower nibble (bits 3-0) are written to both the left and right CD volume settings at index register 28h. The default value for this register is 00h.

## Absolute Maximum Ratings

All voltages measured with respect to ground potential node where AGND and DGND are connected.

$T_A$=0°C to 70°C unless otherwise noted.

| PARAMETER | SYMBOL | TEST CONDITIONS | LIMIT | UNIT |
|---|---|---|---|---|
| Positive Supply Voltage | $V_{DD}$ | $V_{DD}$ | -0.3 to +7.0 | V |
| Digital Input Voltage | $V_{IN}$ | All digital inputs | -0.3 to $V_{DD}$+0.3 | V |
| Analog Input Voltage | $V_{INA}$ | All analog inputs | $V_{SS}$-0.3 to $V_{DD}$+0.3 | V |
| Storage Temperature | $T_{stg}$ | | -25 to 120 | °C |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

## Recommended Operating Conditions

$T_A$=0°C to 70°C unless otherwise noted

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Positive Supply Voltage | $V_{DD}$ | $V_{DD}$ | 4.75 | 5 | 5.25 | V |
| Digital Input Voltage | $V_{IN}$ | All digital inputs | -0.3 | | $V_{DD}$ +0.3 | V |
| Analog Input Voltage | $V_{INA}$ | All analog inputs | $V_{SS}$ -0.3 | | $V_{DD}$ +0.3 | V |
| Storage Temperature | $T_{stg}$ | | 0 | | 70 | °C |

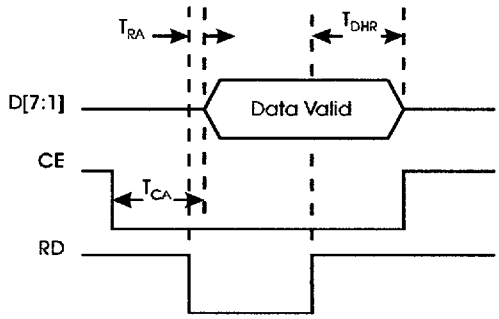
## Electrical Characteristics

The following characteristics apply for $DV_{DD}$=5V, $V_{DD}$=5V supply voltage, $f_{IN}$=1 kHz and $V_{IN}$=.3$V_{rms}$ input signal; master volume and input attenuation all 0dB, unless otherwise specified. All limits apply for T=25°C.

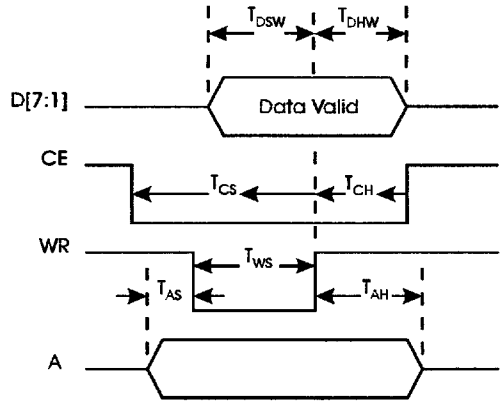
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Supply Current | $I_{VDD}$ | All xL/xR inputs, volumes mute; all digital inputs at GND level, except $\overline{CE}$, A0, $\overline{WR}$ and $\overline{RD}$ at $V_{DD}$ | | | 12 | 15 | mA |
| Input Voltage (RMS) | $V_{IN}$ | THD=0.5%, RL=10kΩ | | 1 | | | V |
| Total Harmonic Distortion | THD | 1 $V_{rms}$, $R_L$=10kΩ | $f_{IN}$=100 Hz | | .08 | 0.5 | % |
| | | | $f_{IN}$=1 kHz | | .13 | 0.5 | |
| | | | $f_{IN}$=10 kHz | | .65 | 0.8 | |
| DC Operating Voltage | $V_O$ | @ LOUT, ROUT | | | 2.14 | | V |
| AC Output Impedance | $r_{out}$ | LOUT, ROUT, $R_L$=10kΩ | | | 100 | 1k | Ω |
| Input Impedance | $r_{in}$ | xL, xR | | 100k | 300k | | Ω |
| Volume Control | | Maximum setting (0dB) | | -0.5 | 0 | 0.5 | dB |
| | | Minimum setting (28db) | | -26 | -28 | -29 | |
| Volume Step Size Error | | (Actual-Nom)/Nom | | | | 5 | % |
| Channel Separation | | Inputs mute. Drv xL, monitor xR | | -60 | | | dB |
| Input Attenuation Control | | Maximum setting (0db) | | -0.5 | 0 | 0.5 | dB |
| except Microphone input) | | Minimum setting (28dB) | | -26 | -28 | -29 | |
| (Microphone input only) | | Minimum setting (-19dB) | | -18 | -19 | -20 | |
| Input Attenuation Step Size Error | | | | | | 5 | % |
| Mute Attenuation | | $V_{IN}$=1$V_{rms}$, xL, xR | | 72 | | | dB |
| Frequency Response | | $f_{IN}$=0.02-20 kHz, rel. to 1 kHz | | | | ±0.2 | dB |
| Signal-to-Noise Ratio | SNR | $V_{IN}$=1$V_{rms}$ | | 72 | 85 | | dB |
| Power Supply Rejection Ratio | PSRR | Apply .2$V_{rms}$, 100 Hz to $V_{DD}$; mute inputs. Check LOUT. | | | -6 | | dB |
| Read Access Time | $T_{RA}$ | | | 50 | | | ns |
| Chip Enable Access Time | $T_{CA}$ | | | 50 | | | ns |
| Data Read Hold Time | $T_{DHR}$ | | | 25 | | | ns |
| Chip Enable Setup Time | $T_{CS}$ | | | 50 | | | ns |
| Write Strobe Time | $T_{WS}$ | | | 20 | | | ns |
| Address Setup Time | $T_{AS}$ | | | 5 | | | ns |
| Address Hold Time | $T_{AH}$ | | | 5 | | | ns |
| Chip Enable Hold Time | $T_{CH}$ | | | 5 | | | ns |
| Data Write Setup Time | $T_{DSW}$ | | | 20 | | | ns |
| Data Write Hold Time | $T_{DHW}$ | | | 5 | | | ns |
| Logic "1" Input | VIH | Digital signals | | 2.0 | | | V |
| Logic "0" Input | VIL | Digital signals | | | | 0.8 | V |

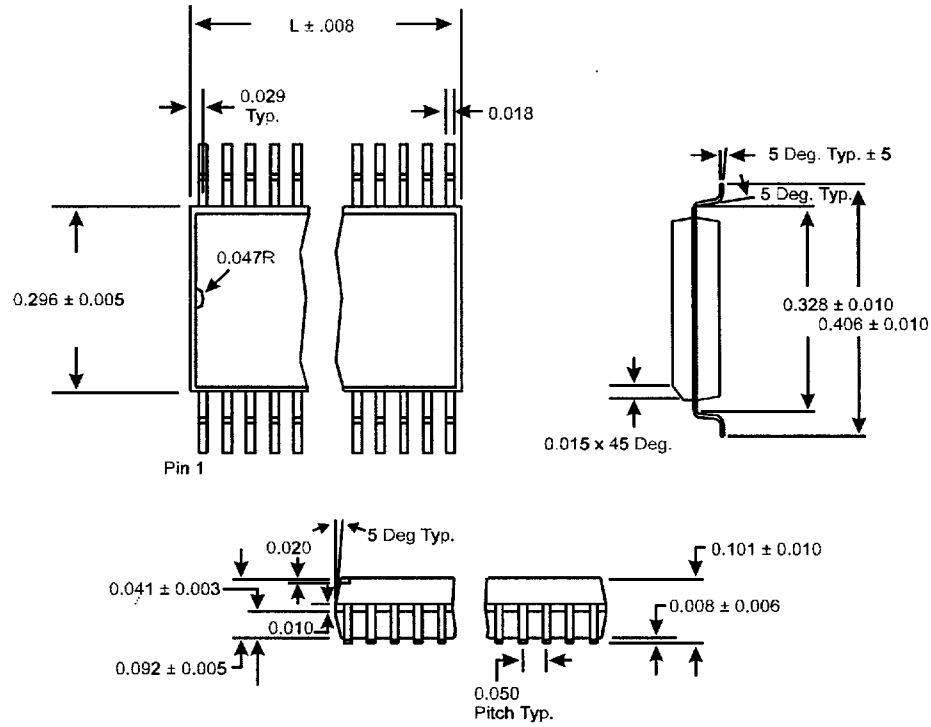
## Interface Timing Definitions

Read




Write






| LEAD COUNT | 28L |
|---|---|
| DIMENSION L | .704 |

**28-Pin SOIC Package**

## Ordering Information

### ICS2102M

Example: