Dual-PLL Motherboard Frequency Generator

Description

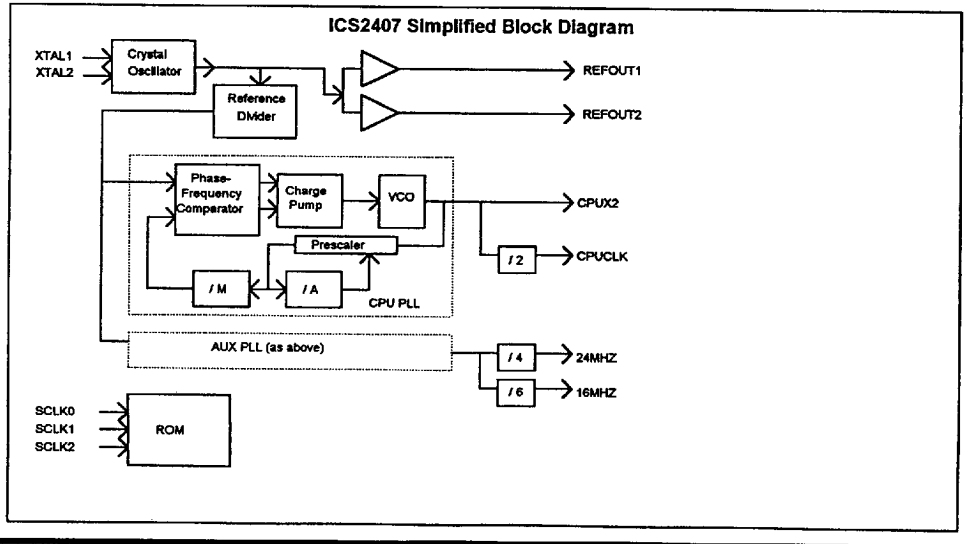
This ICS family of motherboard frequency generators all stem from the same basic design. They are dual-PLL (phase-locked loop) clock generators specifically designed for motherboard applications. Metal layer and assembly options are used to generate the three separate device types in order to optimize the functionality for specific applications. All frequencies are synthesized from a single reference clock which may be generated by the on-chip crystal oscillator or an external reference clock.

The CPU clock PLL is ROM-programmed to generate any of seven customer specified frequencies through selection of the address lines **SCLK0-SCLK2**. *In the ICS2409, ICS2419 and ICS2439 versions the SCLK3 input selects those frequencies directly or divided by two for the CPUX2 output.* The **CPUX2** output is then divided by two to generate the **CPUCLK** output. A power-down mode may be selected with the **SCLK** inputs to reduce standby current consumption to a few microamperes.

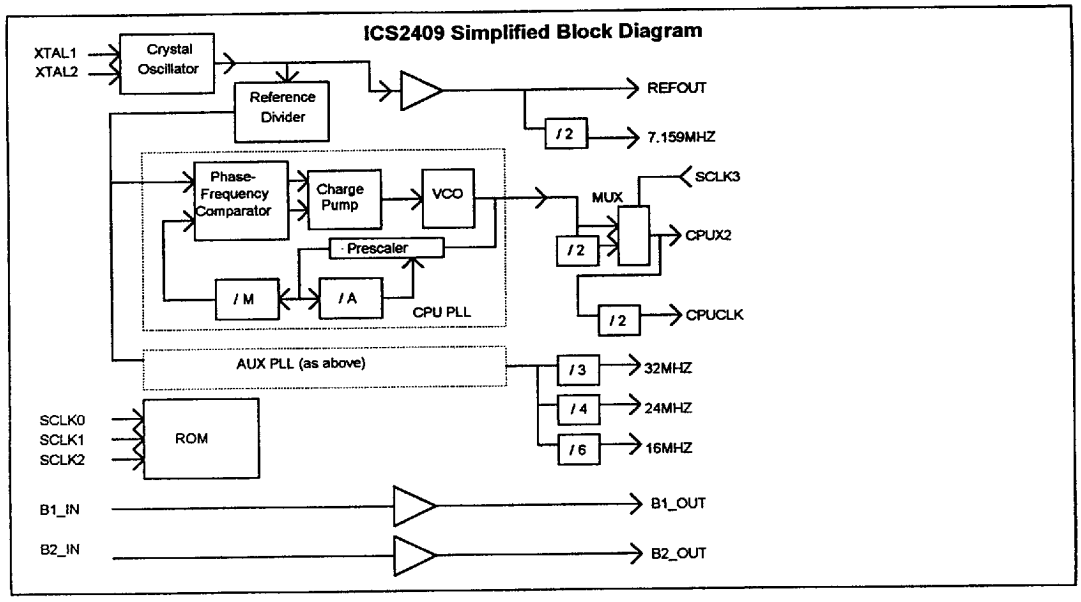
The auxiliary (AUX) PLL generates the fixed frequencies shown in Table 1 for other system uses. A buffered reference frequency output is available on the **REFOUT** pin. Two non-dedicated buffers are provided on the **ICS2409, ICS2419** and **ICS2439** for additional drive capability without adding external buffers and their board space.

Features

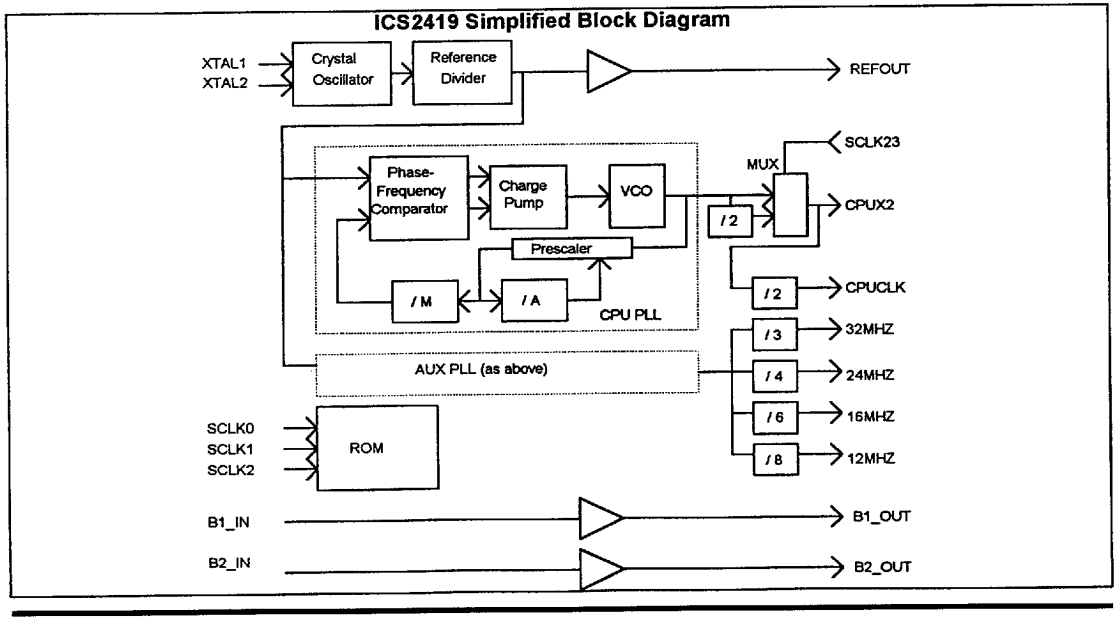
- Supports 286, 386, & 486 desktop and notebook motherboard designs
- Advanced ICS monolithic phase-locked loop technology for low short-term and "cumulative" jitter
- Completely integrated - no external loop filter capacitors required
- Dual-modulus prescaler permits high-speed operation with no sacrifice in accuracy
- Power-down mode for low standby power consumption
- Low-skew between **CPUX2** and **CPUCLK** outputs (< 1 nsec)
- 3-volt supply capability to 85 MHz (**CPUX2** output)
- Output enable (**OE**˜) pin for tristate of device outputs
- **ICS2409, ICS2419** and **ICS2439** offer 24-pin PDIP (0.3") and 24-pin SSOP (5.3mm) package options
- **ICS2407** offers 18-pin PDIP (0.3") and 18-pin SOIC (0.3") package options

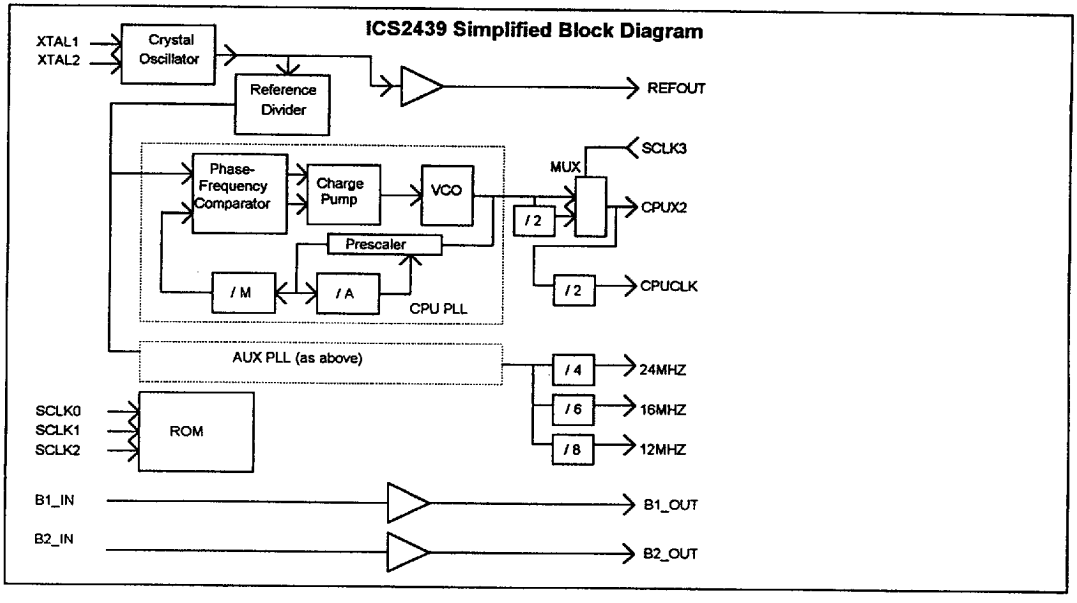


ICS2409 Simplified Block Diagram



ICS2419 Simplified Block Diagram





Circuit Function and Application

Fixed Frequencies

The ICS motherboard family supplies "fixed" frequencies normally used to provide several system functions:

- 32 MHz - ISA Bus Clock
- 24 MHz - Floppy Drives
- 16 MHz - AT Bus Clock Output
- 12 MHz - Keyboard Clock
- 7.149 MHz - Keyboard Clock

Selectable CPU Clock Frequencies

The **ICS2407, ICS2409, ICS2419** and **ICS2439** are designed to generate CPU clock options ranging from 24 MHz, to 88 MHz. For added flexibility, the **ICS2409, ICS2419** and **ICS2439** allow the user to select each of these frequencies divided by 2.

Buffered Output Pins

In addition, the **ICS2409, ICS2419** and **ICS2439** provide 2 non-dedicated buffers for additional flexibility. This allows for extra drive capability without sacrificing the extra board space required for external buffers.

Buffered XTALOUT

In motherboard applications it may be desirable to have the **ICS2439** provide the bus clock for the rest of the system. This eliminates the need for an additional 14.31818 MHz crystal oscillator on the system, saving money as well as board space. Depending on the load, it may be judicious to buffer REFOUT when using it to provide the system clock. On the **ICS2407**, there are two identical outputs, REFOUT1 and REFOUT2.

Power-Down Mode

All three devices have been optimized for use in battery operated portables. It can be placed in a power-down mode which drops its supply current requirement below 1μA(typical).

Pin Description

Input Pins

Frequency Reference

The internal reference oscillator contains all of the passive components required. An appropriate crystal should be connected between XTAL1 (1) and XTAL2 (2). In IBM compatible applications this will typically be a 14.31818 MHz crystal.

Digital Inputs

SCLK0, SCLK1, SCLK2 and SCLK3 ***(ICS2409, ICS2419 and ICS2439 only)*** are the TTL compatible frequency select inputs for the binary code corresponding to the desired frequency. All select pins have internal pull-up devices built in *(See Table 2 for a complete list of available frequencies).*

Buffer Inputs (ICS2409, ICS2419 & ICS2439)

B1_IN and B2_IN (3, 7) provide additional buffering needed on a typical board design without the added cost of external components.

Output Enable

An output enable pin OE~allows the user to tristate the device outputs. When this pin is high, all outputs are in tristate mode. When low, all outputs are enabled. This pin has an internal pull-down to enable all outputs when the pin is N/C.

ICS2407 Pinout

1	XTAL1	REFOUT1	18
2	XTAL2	VDD	17
3	VSS	N/C	16
4	REFOUT2	16MHZ	15
5	SCLK0	24MHZ	14
6	N/C	VSS	13
7	VDD	CPUX2	12
8	SCLK1	SCLK2	11
9	CPUCLK	OE~	10

18-Pin PDIP or SOIC
K-4, K-7

ICS2409 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	7.159MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	32MHZ	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

ICS2439 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	12MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	RESERVED	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

ICS2419 Pinout

1	XTAL1	REFOUT	24
2	XTAL2	B1_OUT	23
3	B1_IN	VDD	22
4	VSS	N/C	21
5	12MHZ	16MHZ	20
6	SCLK0	24MHZ	19
7	B2_IN	32MHZ	18
8	N/C	B2_OUT	17
9	VDD	VSS	16
10	SCLK1	CPUX2	15
11	SCLK3	SCLK2	14
12	CPUCLK	OE~	13

24-Pin PDIP or SSOP
K-5, K-9

Absolute Maximum Ratings

Supply Voltage ..... V_{DD} ..... -0.5V to +7V
Input Voltage ..... V_{IN} ..... -0.5V to V_{DD} + 0.5V
Output Voltage ..... V_{OUT} ..... -0.5V to V_{DD} + 0.5V
Clamp Diode Current ..... V_{IK} & I_{OK} ..... ±30mA
Output Current per Pin ..... I_{OUT} ..... ±50mA
Operating Temperature ..... T_O ..... 0°C to 70°
Storage temperature ..... T_S ..... -85°C to 150°
Power Dissipation ..... P_D 500mW

Values beyond these ratings may damage the device. This device contains circuitry to protect the inputs and outputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid applications of any voltage higher than themaximum rated voltages. For proper operation it is recommended that Vin and Vout be constrained to >=V_{SS} and <=V_{DD}.

DC Characteristics at 5 Volts V_{DD}

(0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		4.5	5.5	V
Input Low Voltage	V_{IL}	V_{DD}=5V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}=5V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}=V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}=1.20mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=1.20mA	2.4	0	V
Supply Current	I_{DD}	VCLK=40MHz	-	40	mA
Supply Current	I_{DD}	VCLK=88MHz	-	50	mA
Internal Pull-up Current	R_{UP}	V_{IN}=0.0V	30	100	µA
Internal Pull-down Current	R_{DOWN}	V_{IN}=0.0V	30	100	µA
Input Pin Capacitance	C_{IN}	F_C=1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C=1MHz	-	12	pF
Power-down Supply Currrent	I_{PN}	V_{DD}=3.3V	-	1	µA

DC Characteristics at 3.3 Volts V_{DD}

(0°C to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Operating Voltage Range	V_{DD}		3.0	3.6	V
Input Low Voltage	V_{IL}	V_{DD}=3.3V	V_{SS}	0.8	V
Input High Voltage	V_{IH}	V_{DD}=3.3V	2.0	V_{DD}	V
Input Leakage Current	I_{IH}	V_{IN}=V_{DD}	-	10	µA
Output Low Voltage	V_{OL}	I_{OL}=8.0mA	-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=8.0mA	2.4	0	V
Supply Current	I_{DD}	CPUX2=40MHz	-	35	mA
Supply Current	I_{DD}	CPUX2=88MHz	-	25	mA
Internal Pull-up Current	R_{UP}	V_{IN}=0.0V	20	70	µA
Internal Pull-down Current	R_{DOWN}	V_{IN}=0.0V	20	70	µA
Input Pin Capacitance	C_{IN}	F_C=1MHz	-	8	pF
Output Pin Capacitance	C_{OUT}	F_C=1MHz	-	12	pF
Power-down Supply Currrent	I_{PN}	V_{DD}=3.3V	-	1	µA

AC Timing Characteristics

The following notes apply to all of the parameters presented in this section.
1. REFCLK = 14.31818 MHz
2. $t_c = 1/f_c$
3. All units are in nanoseconds (ns)
4. Rise and fall time between .8 and 2.0 VDX unless otherwise stated.
5. Output pin loading = 15pF
6. Duty cycle measured at $V_{DD}/2$ unless otherwise stated.

SYMBOL	PARAMETER	MIN	MAX	NOTES
	OUTPUT TIMING @5v			
Tr	Rise Time	-	2	
Tf	Fall Time	-	2	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.0	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tristate (into and out of) time	-	15	nSec
	OUTPUT TIMING @3.3v			
Tr	Rise Time	-	3	
Tf	Fall Time	-	3	
-	Frequency Error	-	0.5	%
Tak	Clock Skew (CPUCLK & CPUX2)	-	1.5	nSec
-	Duty Cycle	45	55	%
-	Output Enable to Tristate (into and out of) time	-	20	nSec

Table 1: Fixed Output Frequencies

ICS2439	ICS2419	ICS2409	ICS2407
24 MHz	32 MHz	32 MHz	24 MHz
16 MHz	24 MHz	24 MHz	16 MHz
12 MHz	16 MHz	16 MHz	
	12 MHz	7.159 MHz	

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Table 2: CPU Clock Frequency Selection

SCLK3	SCLK2	SCLK1	SCLK0	ICS2439 Pattern 001	ICS2419 Pattern 001	ICS2409 Pattern 409	ICS2407 Pattern 407
0	0	0	0	12 MHz	12 MHz	12 MHz	12 MHz
0	0	0	1	16	16	16	16
0	0	1	0	20	20	20	20
0	0	1	1	25	25	25	25
0	1	0	0	33.33	33.33	33.33	33.33
0	1	0	1	40	40	40	40
0	1	1	0	30	30	44	44
0	1	1	1	Power-down	Power-down	Power-down	Power-down
1	0	0	0	24	24	24	
1	0	0	1	32	32	32	
1	0	1	0	40	40	40	
1	0	1	1	50	50	50	
1	1	0	0	66.66	66.66	66.66	
1	1	0	1	80	80	80	
1	1	1	0	60	60	88	
1	1	1	1	TEST	TEST	TEST	

Ordering Information

ICS2407-XXXN, ICS2407-XXXM; ICS2409-XXXN, ICS2409-XXXF
ICS2419-XXXN, ICS2419-XXXF; ICS2439-XXXN, ICS2439-XXXF

Example: