Integrated Circuit Systems, Inc.

ICS5341 GENDAC

Advance Information

16-Bit Integrated Clock-LUT-DAC

General Description

The ICS5341 GENDAC is a combination of dual programmable clock generators, a 256 x 18-bit RAM, and a triple 8-bit video DAC. The GENDAC supports 8-bit pseudo color applications, as well as 15-bit, 16-bit and 24-bit True Color bypass for high speed, direct access to the DACs.

The RAM makes it possible to display 256 colors selected from a possible 262, 144 colors. The dual clock generators use Phase Locked Loop (PLL) technology to provide programmable frequencies for use in the graphics subsystem. The video clock contains 8 frequencies, 6 of which are programmable by the user. The memory clock has two programmable frequency locations.

The three 8-bit DACs on the ICS5341 are capable of driving singly or doubly-terminated 75Ω loads to nominal 0 - 0.7 volts at pixel rates up to 135 MHz. Differential and integral linearity errors are less than 1 LSB over full temperature and V_{DD} ranges. Monotonicity is guaranteed by design. On-chip pixel mask register allows displayed colors to be changed in a single write cycle rather than by modifying the color palette.

ICS is the world leader in all aspects of frequency (clock) generation for graphics, using patented techniques to produce low jitter video timing.

Features

- **Designed for compatibility with Tseng Labs VGA controllers**
- **Triple video DAC, dual clock generator, and a color palette**
- **24, 16, 15, or 8-bit pseudo color pixel mode supports True Color, Hi-Color, and VGA modes**
- **High speed 256 x 18 color palette (135 MHz) with bypass mode and 8-bit DACs**
- **Two fixed, six programmable video (pixel) clock frequencies (CLK0)**
- **Two programmable memory (controller) clock frequency (CLK1)**
- **DAC power down in blanking mode**
- **Anti-sparkle circuitry**
- **On-chip loop filters reduce external components**
- **Standard CPU interface**
- **Single external crystal (typically 14.318 MHz)**
- **Monitor Sense**
- **Internal voltage reference**
- **135 MHz (-3), 110 MHz (-2) & 80 MHz (-1) versions**
- **Very low clock jitter**
- **Latched frequency control pin**

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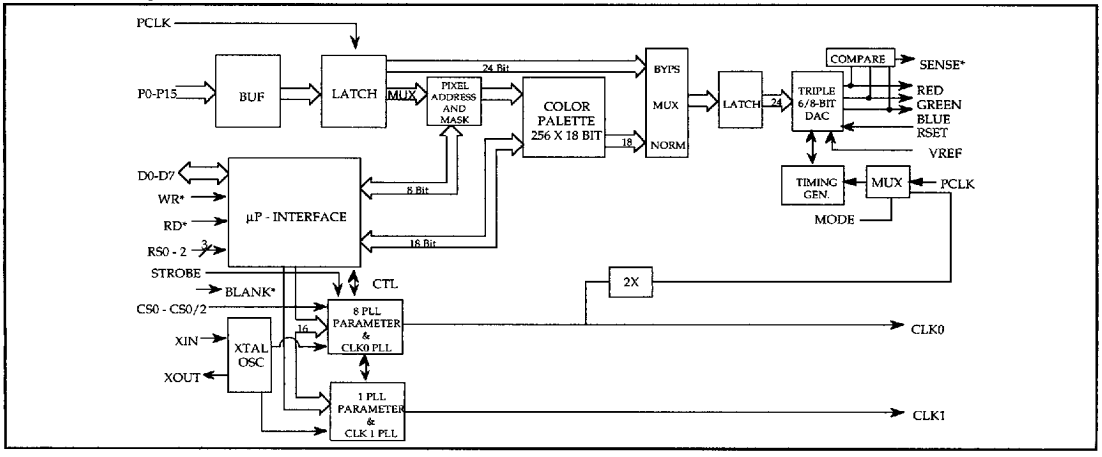
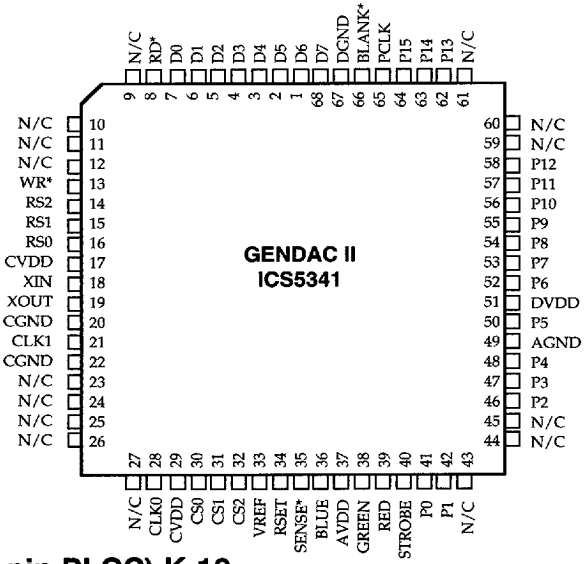
Block Diagram



Pin Configuration



Rev 1.0

Pin Description (68 pin PLCC) K-10

Symbol	Pin #	Type	Description
D7 - D0	68, 1 - 7	I/O	System data bus I/O. These bidirectional Data I/O lines are used by the host microprocessor to write (using active low WR*) information into, and read (using active low RD*) information from the six internal registers (Pixel Address, Color Value, Pixel Mask, PLL Address, PLL Parameter, and Command). During the write cycle, the rising edge of WR* latches the data into the selected register (set by the status of the three RS pins). The rising edge of RD* determines the end of the read cycle. When RD* is a logical high, the Data I/O lines no longer contain information from the selected register and will go into a tri-state mode.
RD*	8	Input	RAM/PLL Read Enable, active low. This is the READ bus control signal. When active, any information present on the internal data bus is available on the Data I/O lines, D0-D7.
WR*	13	Input	RAM/PLL Write Enable, active low. This signal controls the timing of the write operation on the microprocessor interface inputs, D0-D7.
RS2 RS1 RS0	14 15 16	Input Input Input	Register Address Select 0. These inputs control the selection of one of the six internal registers. They are sampled on the falling edge of the active enable signal (RD* or WR*).
CVDD	17	-	Crystal oscillator and CLK0 power supply connect to AVDD.
XIN	18	Input	Crystal input. A 14.318 MHz crystal should be connected to this pin.
XOUT	19	Output	Crystal output. A 14.318 MHz crystal should be connected to this pin.
CGND	20	-	VSS for CLK0. Connect to ground.

Pin Description (continued)

Symbol	Pin #	Type	Description
CLK1	21	Output	Memory clock output. Used to time the video memory.
CGND	22	-	VSS for CLK1. Connect to ground.
CLK0	28	Output	Video clock output. Provides a CMOS level pixel or dot clock frequency to the graphics controller. The output frequency is determined by the values of the PLL registers.
CVDD	29	-	CLK1 Power Supply. Connect to AVDD.
CS0	30	Input	Clock select 0. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS1	31	Input	Clock select 1. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
CS2	32	Input	Clock select 2. The status of CS0-2 determine which frequency is selected on the CLK0 (video) output. Latched by STB.
VREF	33	I/O	Internal Reference Voltage. Normally connects to a 0.1µ cap to ground. To use an external Vref, connect a 1.235V reference to this pin.
RSET	34	Input	Resistor Set. This pin is used to set the current level in the analog outputs. It is usually connected through a 140Ω, 1% resistor to ground.
SENSE*	35	Output	Monitor Sense, active low. This pin is low when any of the red, green, or blue outputs have exceeded 335mV. The chip has on-board comparators and an internal 335mV voltage reference. This is used to detect monitor type.
AVDD	37	-	DAC power supply. Connect to AVDD.
BLUE GREEN RED	36 38 39	Output Output Output	Color Signals. These three signals are the DACs' analog outputs. Each DAC is composed of several current sources. The outputs of each of the sources are added together according to the applied binary value. These outputs are typically used to drive a CRT monitor.
STROBE	40	Input	Latches the input clock select signals CS0 - CS2.
P0 - P15	41- 42 46-48, 50	Input	Pixel Address Lines. This byte-wide information is latched by the rising edge of PCLK when using the Color Palette, and is masked by the Pixel Mask register. These values are used to specify the RAM word address in the default mode (accessing RAM). In the Hi-Color XGA, and True Color modes, they represent color data for the DACs. These inputs should be grounded if they are not used.
AGND	49	-	DAC Ground. Connect to ground.
DVDD	51	-	Digital power supply.
PCLK	65 52-58, 62-64	Input	Pixel Clock. The rising edge of PCLK controls the latching of the Pixel Address and BLANK* inputs. This clock also controls the progress of these values through the three-stage pipeline of the Color Palette RAM, DAC, and outputs.
BLANK*	66	Input	Composite BLANK* Signal, active low. When BLANK* is asserted, the outputs of the DACs are zero and the screen becomes black. The DACs are automatically powered down to save current during blanking. The color palette may still be updated through D0-D7 during blanking.
DGND	67	-	Digital Ground. Connect to ground.

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Ordering Information

ICS5341V

Example: