



GENERAL DESCRIPTION

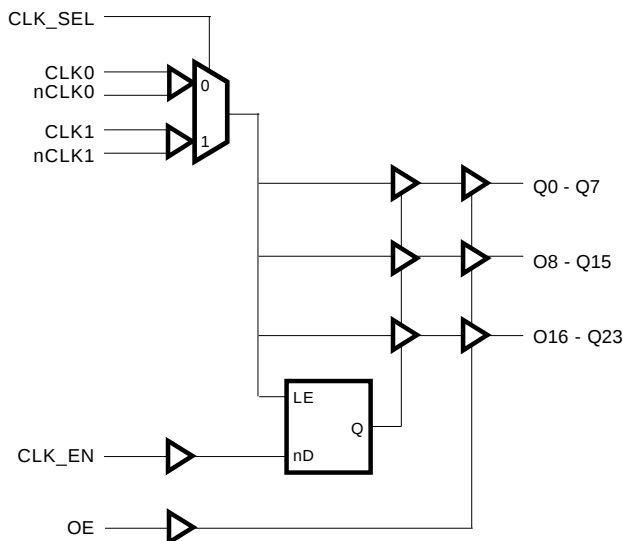
The ICS8344-01 is a low voltage, low skew fanout buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The ICS8344-01 is designed to translate any differential signal levels to LVCMOS levels. The low impedance LVCMOS outputs are designed to drive 50Ω series or parallel terminated transmission lines. The effective fanout can be increased to 48 by utilizing the ability of the outputs to drive two series terminated lines. Redundant clock applications can make use of the dual clock input. The dual clock inputs also facilitate board level testing. The output enable is synchronous which eliminates the runt clock pulses which occur during asynchronous enabling and disabling of the outputs. The outputs are driven low when disabled. The ICS8344-01 is characterized at full 3.3V, full 2.5V and mixed 3.3V input and 2.5V output operating supply modes.

Guaranteed output and part-to-part skew characteristics make the ICS8344-01 ideal for those clock distribution applications demanding well defined performance and repeatability.

FEATURES

- 24 LVCMOS outputs, 7Ω typical output impedance
- Output frequency up to 250MHz
- 85ps bank skew, 200ps output skew, 900ps part to part skew
- Translates any differential input signal (PECL, HSTL, LVDS) to LVCMOS without external bias networks
- Translates any single ended input signal to LVCMOS with resistor bias on nCLK input
- Translates any single ended input signal to inverted LVCMOS with resistor bias on CLK input
- LVCMOS control inputs
- Synchronous clock enable
- 3.3V, 2.5V or mixed 3.3V, 2.5V operating supply modes
- 48 lead low-profile QFP (LQFP), 7mm x 7mm x 1.4mm package body, 0.5mm package lead pitch
- 0°C to 70°C ambient operating temperature
- Industrial temperature version available upon request

BLOCK DIAGRAM



PIN ASSIGNMENT

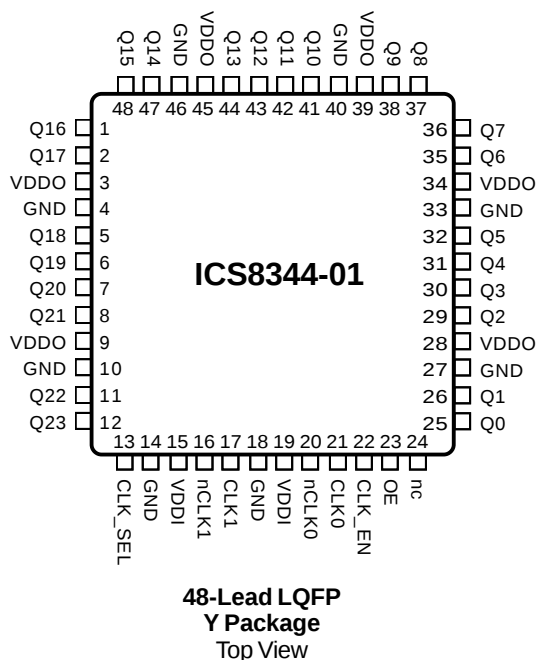




TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 2, 5, 6 7, 8, 11, 12	Q16, Q17, Q18, Q19 Q20, Q21, Q22, Q23	Output		Q16 thru Q23 outputs. 7 Ω typical output impedance.
3, 9, 28, 34, 39, 45	VDDO	Power		Output power supply. Connect 3.3V or 2.5V.
4, 10, 14, 18, 27, 33, 40, 46	GND	Power		Power supply ground. Connect to ground.
13	CLK_SEL	Input	Pulldown	Clock select input. Selects between CLK0, nCLK0 and CLK1, nCLK1 as the differential pair that controls the output.
15, 19	VDDI	Power		Input power supply. Connect 3.3V or 2.5V.
16	nCLK1	Input	Pullup	Inverting input of secondary differential clock input pair.
17	CLK1	Input	Pulldown	Non-inverting input of secondary differential clock input pair.
20	nCLK0	Input	Pullup	Inverting input of primary differential clock input pair.
21	CLK0	Input	Pulldown	Non-inverting input of primary differential clock input pair.
22	CLK_EN	Input	Pullup	Synchronous control for enabling and disabling clock outputs. LVCMOS interface levels.
23	OE	Input	Pullup	Output enable. Controls enabling and disabling of outputs Q0 thru Q23.
24	nc	Unused		Unused pin.
25, 26, 29, 30 31, 32, 35, 36	Q0, Q1, Q2, Q3 Q4, Q5, Q6, Q7	Output		Q0 thru Q7 outputs. 7 Ω typical output impedance.
37, 38, 41, 42 43, 44, 47, 48	Q8, Q9, Q10, Q11 Q12, Q13, Q14, Q15	Output		Q8 thru Q15 outputs. 7 Ω typical output impedance.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
CIN	Input Capacitance	CLK0, nCLK0, CLK1, nCLK1					pF
		CLK_SEL, CLK_EN, OE					pF
CPD	Power Dissipation Capacitance (per output)		VDDI, VDDO = 3.465V				pF
			VDDI = 3.465V, VDDO = 2.63V				pF
			VDDI, VDDO = 2.63V				pF
RPULLUP	Input Pullup Resistor				51		K Ω
RPULLDOWN	Input Pulldown Resistor				51		K Ω
ROUT	Output Impedance				7		Ω



TABLE 3A. OUPUT ENABLE FUNCTION TABLE

Bank 1		Bank 2		Bank 3	
Input	Output	Input	Output	Input	Output
OE	Q0-Q7	OE	Q8-Q15	OE	Q16-Q23
0	Hi-Z	0	Hi-Z	0	Hi-Z
1	Active	1	Active	1	Active

TABLE 3B. CLOCK SELECT FUNCTION TABLE

Control Input	Clock	
CLK_SEL	CLK0, nCLK0	CLK1, nCLK1
0	Selected	De-selected
1	De-selected	Selected

TABLE 3C. CLOCK INPUTS FUNCTION TABLE

Inputs			Outputs	Input to Output Mode	Polarity
OE	CLK0, CLK1	nCLK0, nCLK1	Q0 thru Q23		
1	0	1	LOW	Differential to Single Ended	Non Inverting
1	1	0	HIGH	Differential to Single Ended	Non Inverting
1	0	Biased; NOTE 1	LOW	Single Ended to Differential	Non Inverting
1	1	Biased; NOTE 1	HIGH	Single Ended to Differential	Non Inverting
1	Biased; NOTE 1	0	HIGH	Single Ended to Differential	Inverting
1	Biased; NOTE 1	1	LOW	Single Ended to Differential	Inverting

NOTE 1: Single ended input use requires that one of the differential inputs be biased. The voltage at the biased input sets the switch point for the single ended input. For LVCMOS input levels the recommended input bias network is a resistor to VDDI, a resistor of equal value to ground and a 0.1µF capacitor from the input to ground. The resulting switch point is VDDI/2.



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	4.6V
Inputs	-0.5V to VDD + 0.5V
Outputs	-0.5V to VDDO + 0.5V
Ambient Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only and functional operation of product at these condition or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		3.135	3.3	3.465	V
IDD	Quiescent Power Supply Current	VDDI = VIH = 3.465V VIL = 0V			60	mA

TABLE 4B. DIFFERENTIAL DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	nCLK0, nCLK1	VDDI = VIN = 3.465V		5	μA
		CLK0, CLK1	VDDI = VIN = 3.465V		150	μA
IIL	Input Low Current	nCLK0, nCLK1	VDDI = 3.465V, VIN = 0V	-150		μA
		CLK0, CLK1	VDDI = 3.465V, VIN = 0V	-5		μA

NOTE 1: For CLK, nCLK input levels see VPP and VCMR in AC Characteristics table.

TABLE 4C. LVCMOS DC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_SEL, CLK_EN, OE	VDDI = 3.465V	2	3.8	V
VIL	Input Low Voltage	CLK_SEL, CLK_EN, OE	VDDI = 3.135V	-0.3	0.8	V
IIH	Input High Current	CLK_EN, OE	VDDI = VIN = 3.465V		5	μA
		CLK_SEL	VDDI = VIN = 3.465V		150	μA
IIL	Input Low Current	CLK_EN, OE	VDDI = 3.465, VIN = 0V	-150		μA
		CLK_SEL	VDDI = 3.465, VIN = 0V	-5		μA
VOH	Output High Voltage	VDDI = VDDO = 3.135V IOH = -36mA	2.7			V
VOL	Output Low Voltage	VDDI = VDDO = 3.135V IOL = 36mA			0.5	V



TABLE 4D. POWER SUPPLY DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		3.135	3.3	3.465	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
IDD	Quiescent Power Supply Current	VDDI = VIH = 3.465V VIL = 0V			60	mA

TABLE 4E. DIFFERENTIAL DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	nCLK0, nCLK1	VDDI = VIN = 3.465V		5	μA
		CLK0, CLK1	VDDI = VIN = 3.465V		150	μA
IIL	Input Low Current	nCLK0, nCLK1	VDDI = 3.465V, VIN = 0V	-150		μA
		CLK0, CLK1	VDDI = 3.465V, VIN = 0V	-5		μA

NOTE 1: For CLKx, nCLKx input levels see VPP and VCMR in AC Characteristics table.

TABLE 4F. LVCMOS DC CHARACTERISTICS, VDDI = 3.3V±5%, VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_SEL, CLK_EN, OE	VDDI = 3.465V	2	3.8	V
VIL	Input Low Voltage	CLK_SEL, CLK_EN, OE	VDDI = 3.135V	-0.3	0.8	V
IIH	Input High Current	CLK_EN, OE	VDDI = VIN = 3.465V		5	μA
		CLK_SEL	VDDI = VIN = 3.465V		150	μA
IIL	Input Low Current	CLK_EN, OE	VDDI = 3.465, VIN = 0V	-150		μA
		CLK_SEL	VDDI = 3.465, VIN = 0V	-5		μA
VOH	Output High Voltage	VDDI = VDDO = 3.135V IOH = -36mA	1.9			V
VOL	Output Low Voltage	VDDI = VDDO = 3.135V IOL = 36mA			0.4	V



TABLE 4G. POWER SUPPLY DC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VDDI	Input Power Supply Voltage		2.375	2.5	2.625	V
VDDO	Output Power Supply Voltage		2.375	2.5	2.625	V
IDD	Quiescent Power Supply Current	VDDI = VIH = 2.625V VIL = 0V			60	mA

TABLE 4H. DIFFERENTIAL DC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
IIH	Input High Current	nCLK0, nCLK1 VDDI = VIN = 2.625V			5	μA
		CLK0, CLK1 VDDI = VIN = 2.625V			150	μA
IIL	Input Low Current	nCLK0, nCLK1 VDDI = 2.625V, VIN = 0V	-150			μA
		CLK0, CLK1 VDDI = 2.625V, VIN = 0V	-5			μA

NOTE 1: For CLKx, nCLKx input levels see VPP and VCMR in AC Characteristics table.

TABLE 4I. LVCMOS DC CHARACTERISTICS, VDDI = VDDO = 2.5V±5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
VIH	Input High Voltage	CLK_SEL, CLK_EN, OE VDDI = 2.625V	2		2.9	V
VIL	Input Low Voltage	CLK_SEL, CLK_EN, OE VDDI = 2.375V	-0.3		0.8	V
IIH	Input High Current	CLK_EN, OE VDDI = VIN = 2.625V			5	μA
		CLK_SEL VDDI = VIN = 2.625V			150	μA
IIL	Input Low Current	CLK_EN, OE VDDI = 2.625, VIN = 0V	-150			μA
		CLK_SEL VDDI = 2.625, VIN = 0V	-5			μA
VOH	Output High Voltage	VDDI = VDDO = 2.375V IOH = -27mA	1.9			V
VOL	Output Low Voltage	VDDI = VDDO = 2.375V IOL = 27mA			0.4	V



TABLE 5. AC CHARACTERISTICS, VDDI = VDDO = 3.3V±5%; VDDI = 3.3V ± 5%, VDDO = 2.5V ± 5%;
VDDI = VDDO = 2.5V ± 5%, T_A = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f _{MAX}	Maximum Input Frequency				250	MHz
V _{PP}	Peak-to-Peak Input Voltage	f = 200MHz	0.3		1.3	V
V _{CMR}	Common Mode Input Voltage	f = 200MHz	0.9		2	V
t _{pLH}	Propagation Delay, Low-to-High	0MHz ≤ f ≤ 200MHz	2.5		5	ns
t _{pHL}	Propagation Delay, High-to-Low	0MHz ≤ f ≤ 200MHz	2.5		5	ns
tsk(b)	Bank Skew; NOTE 2	Q0 - Q7	Measured on the rising edge of VDDO/2		85	ps
		Q8 - Q15			180	ps
		Q16 - Q23			100	ps
tsk(o)	Output Skew; NOTE 3	Measured on the rising edge of VDDO/2			200	ps
tsk(pp)	Part-to-Part Skew; NOTE 4	Measured on the rising edge of VDDO/2			900	ps
t _R	Output Rise Time; NOTE 5	30% to 70%	200		800	ps
t _F	Output Fall Time; NOTE 5	30% to 70%	200		800	ps
t _{PW}	Output Pulse Width	0MHz ≤ f ≤ 200MHz	t _{CYCLE} /2 - 0.25	t _{CYCLE} /2	t _{CYCLE} /2 + 0.25	ns
		f = 200MHz	2.25	2.5	2.75	ns
t _{EN}	Output Enable Time; NOTE 5	f = 10MHz			5	ns
t _{DIS}	Output Disable Time; NOTE 5	f = 10MHz			4	ns

NOTE 1: All parameters measured at 200MHz and VP_{Ptyp} unless noted otherwise. All outputs terminated with 50Ω to VDDO/2.

NOTE 2: Defined as skew within a bank of outputs at the same voltages and with equal load conditions.

NOTE 3: Defined as skew across banks of outputs at the same supply voltages and with equal load conditions.

NOTE 4: Defined as the skew at different outputs on different devices operating at the same supply voltages with equal load conditions.

NOTE 5: These parameters are guaranteed by characterization. Not tested in production.



FIGURE 1A, 1B, 1C - INPUT CLOCK WAVEFORMS

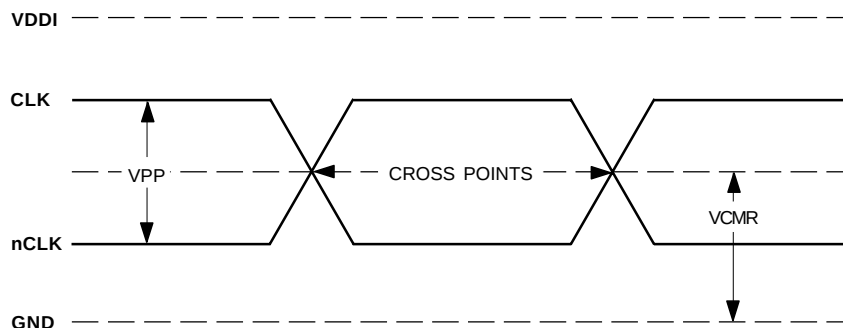


FIGURE 1A - LVDS, HSTL DIFFERENTIAL INPUT LEVELS

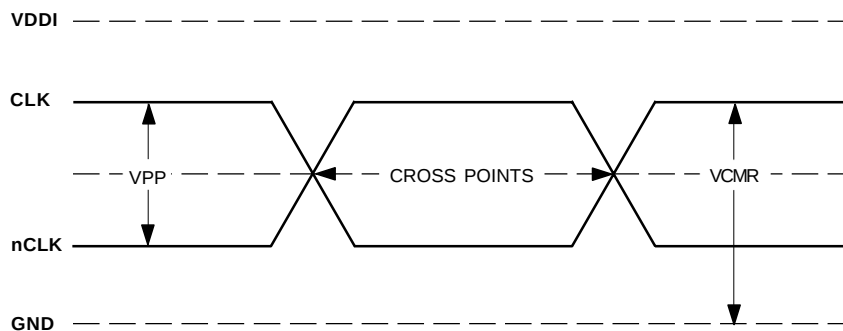


FIGURE 1B - LVPECL DIFFERENTIAL INPUT LEVEL

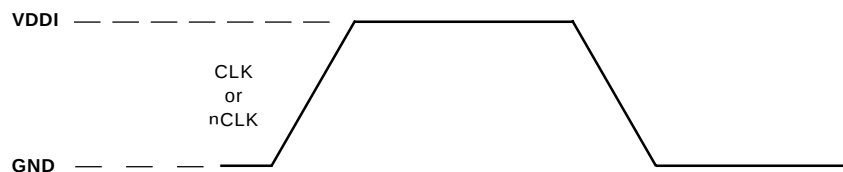


FIGURE 1C- LVCMOS AND LVTTTL SINGLE ENDED INPUT LEVEL



FIGURE 2A, 2B - TIMING WAVEFORMS

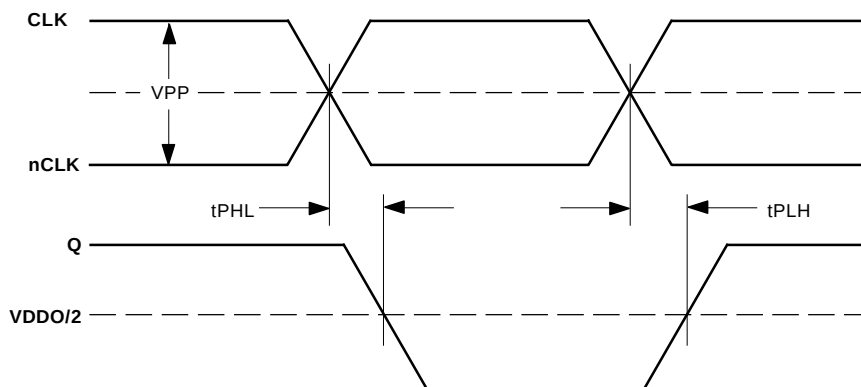


FIGURE 2A - PROPAGATION DELAYS

$f_{in} = 200\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 200\text{ps}$

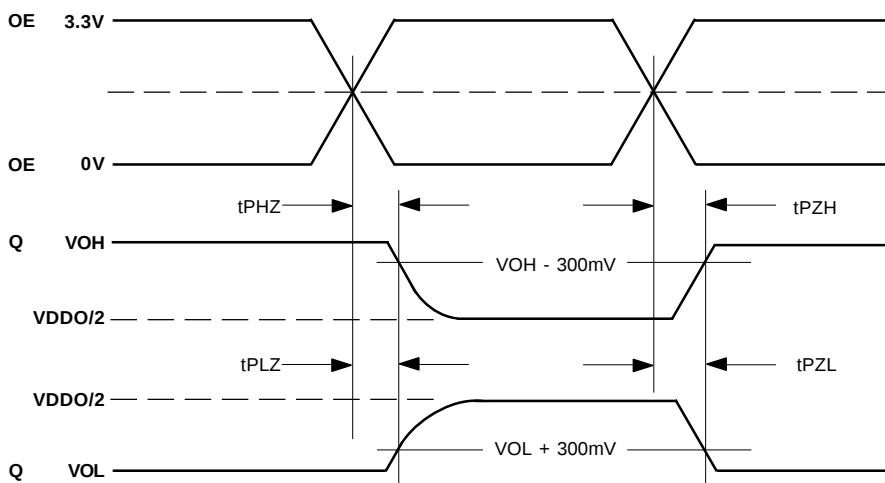


FIGURE 2B - DISABLE AND ENABLE TIMES

$f_{in} = 10\text{MHz}$, $V_{amp} = 3.3\text{V}$, $t_r = t_f = 600\text{ps}$



FIGURE 3A, 3B- SKEW DEFINITIONS & WAVEFORMS

Bank Skew - Skew between outputs within a bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

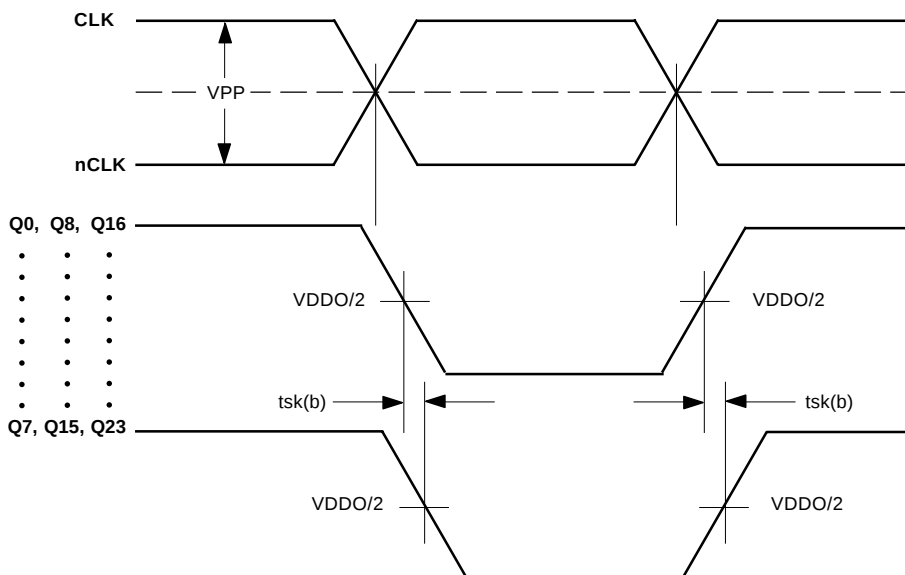


FIGURE 3A - BANK SKEW

$f_{in} = 200\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 150\text{ps}$

Output Skew - Skew between outputs of any bank. Outputs operating at the same temperature, supply voltages and with equal load conditions.

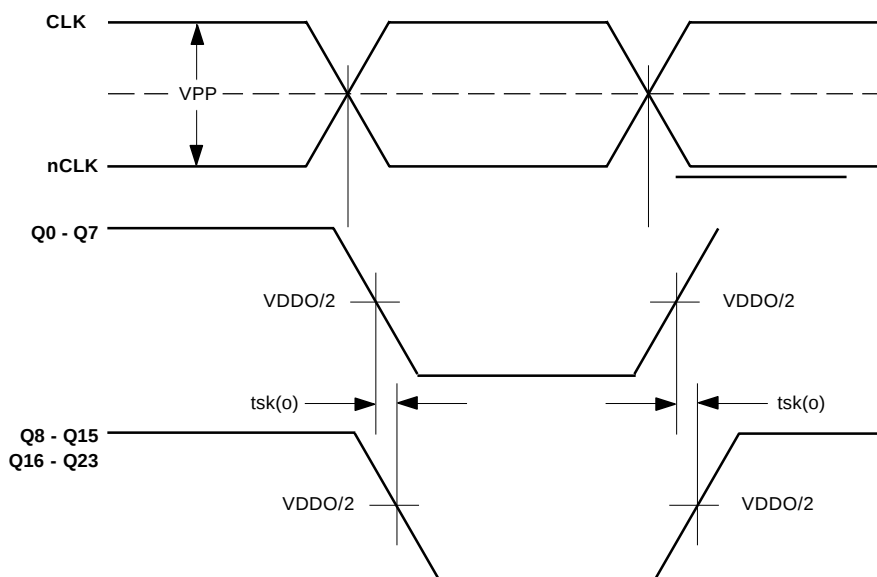


FIGURE 3B - OUTPUT SKEW

$f_{in} = 200\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 150\text{ps}$



FIGURE 4A - SKEW DEFINITIONS & WAVEFORMS

Part to Part Skew - Skew between outputs of any bank on different parts. Outputs operating at the same temperature, supply voltages and with equal load conditions.

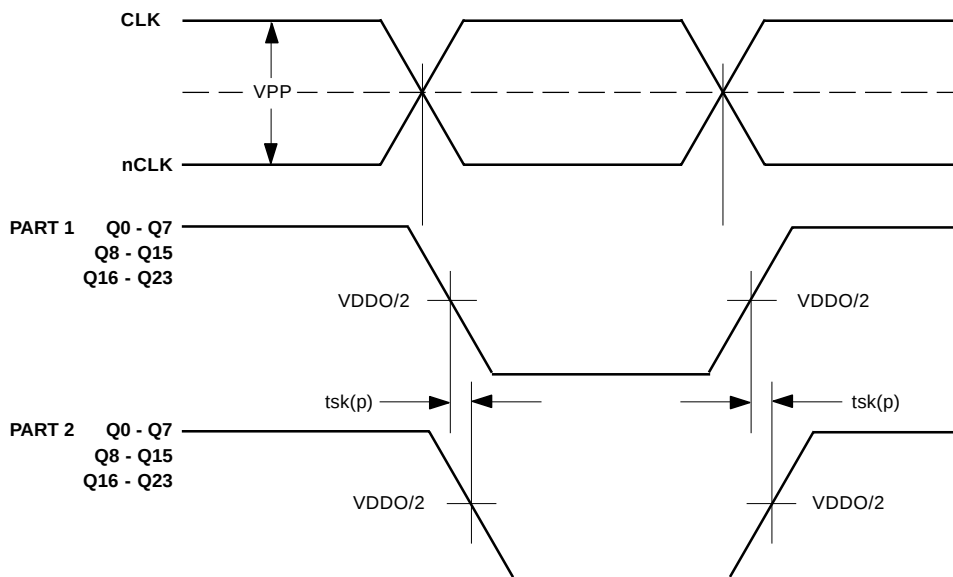


FIGURE 4B - OUTPUT SKEW

$f_{in} = 200\text{MHz}$, $V_{pp} = 300\text{mV}$, $t_r = t_f = 150\text{ps}$



PACKAGE OUTLINE - Y SUFFIX

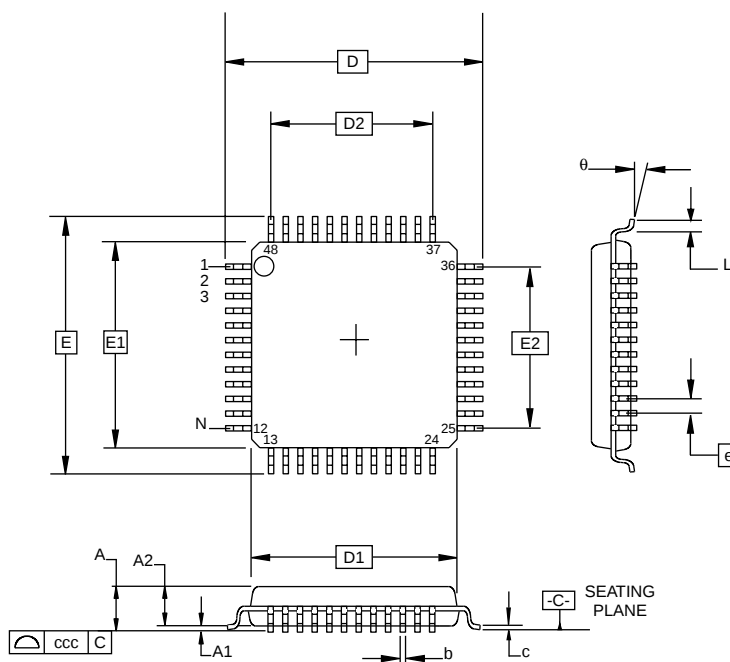


TABLE 6. PACKAGE DIMENSIONS

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	BCC		
	MINIMUM	NOMINAL	MAXIMUM
N	48		
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09		0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50	
e		0.5 BASIC	
L	0.45	0.60	0.75
θ	0°		7°
ccc			0.08

Reference Document: JEDEC Publication 95, MS-026



Integrated
Circuit
Systems, Inc.

ICS8344-01

LOW SKEW, 1-TO-24 DIFFERENTIAL-TO-LVCMOS FANOUT BUFFER

TABLE 7. ORDERING INFORMATION

Part/Order Number	Marking	Package	Count	Temperature
ICS8344BY-01	ICS8344BY-01	48 Lead LQFP	250 per tray	0°C to 70°C
ICS8344BY-01T	ICS8344BY-01	48 Lead LQFP on Tape and Reel	2000	0°C to 70°C

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