Integrated Circuit Systems, Inc.

ICS9111-01

300 MHz Clock Generator for RAMBUS™ Systems

General Description

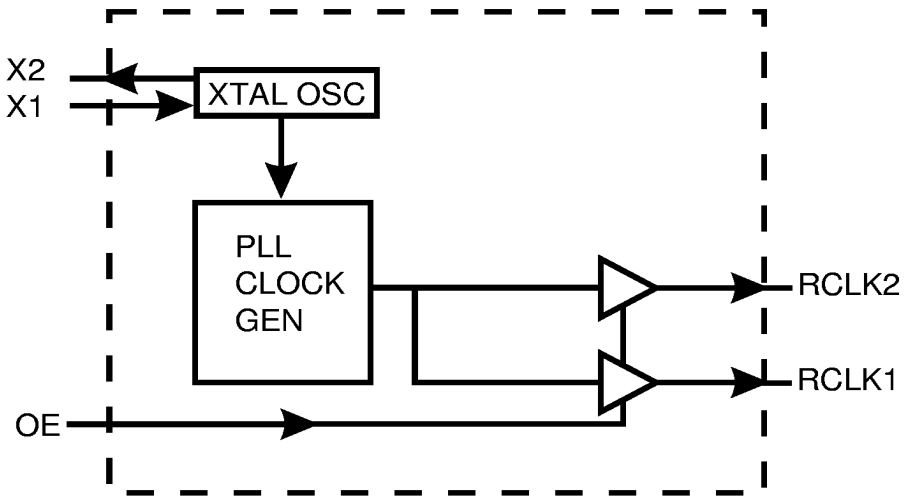
The **ICS9111-01** is a high speed clock generator designed to support the 600Mbit/line data transfer rates made possible by local phase alignment technologies such as RAMBUS™ style systems. Generating RCLK rates as high as 280 MHz in 3V systems from either a 20 MHz crystal or external system reference, the **ICS9111-01** is ideal for graphics applications.

The RCLK open collector buffer output impedance is less than 10Ω to allow external terminating impedance and voltage combinations for RAMBUS style systems. Cycle-to-cycle jitter is less than 100ps and output skew is less than 50ps and the 50% duty cycle is maintained to within ±5% for series terminations to V_{term}.

Features

- 300 MHz RCLK covers RAMBUS speeds to 600Mbit/line at 3.3V±5%.
- Output capable of running between 60 to 280 MHz with 3.3 V ± 10% V_{DD}; up to 300 MHz for 3.3 V ± 5% V_{DD}
- Less than 100ps cycle-to-cycle jitter (RCLK2) (150ps for RCLK1)
- 50 ± 5% duty cycle
- Open drain drivers allow matched termination
- Drives 20-50 Ω transmission lines
- Nominal 18.0 MHz crystal or extended reference (5 to 21.4 MHz)
- On-chip loop filter components
- 3.0V - 3.6 V supply range
- 8-pin 150-mil SOIC package
- Custom options capable

Block Diagram



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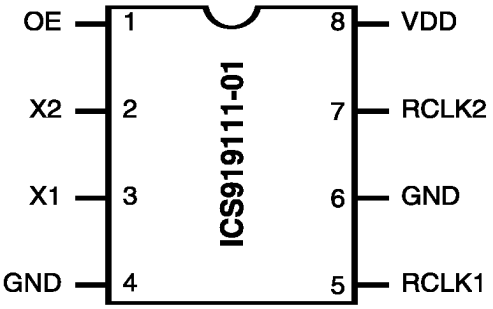
Pin Configuration



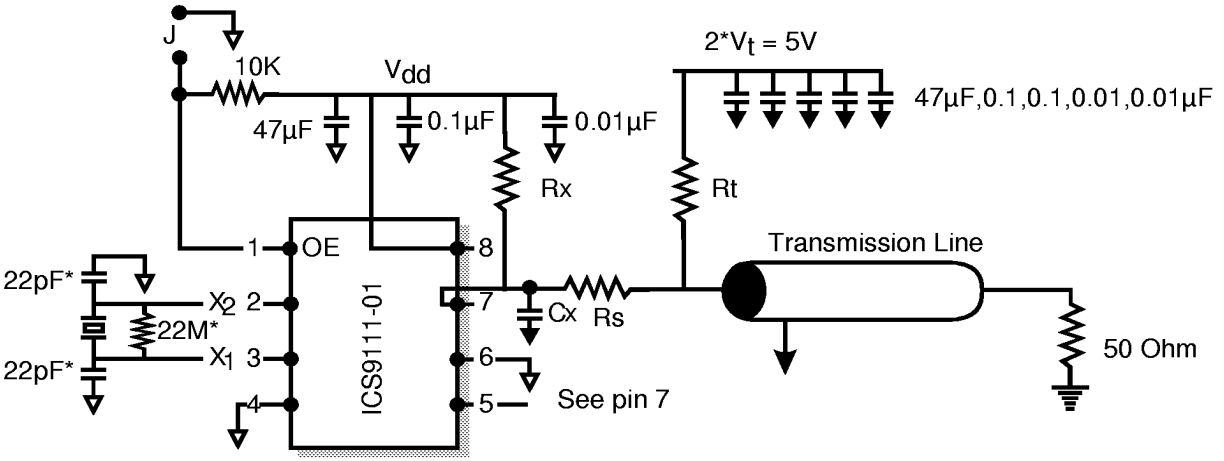
8-PIN SOIC

Functionality

RCLK Ratio	X1, X2 (MHz)	OE	RCLK (MHz)
X1*14	18.0	1	252
	18.0	0	Tristate

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	OE	IN	Output enable causes all outputs to tristate when at a low level; has a pull-up.
2	X2	IN	Crystal drive output from device, which includes crystal load capacitance.
3	X1	IN	Crystal or external clock input to device. This input includes crystal load capacitance and feedback bias resistor for a 12 to 24 MHz crystal, nominally 18 MHz.
4, 6	GND	PWR	Ground connection for logic, PLL and output buffers.
5, 7	RCLK(1,2)	OUT	Output buffer pins, device has open-drain N-channel MOSFET device going to ground. See application information for pull-up/termination recommendations.
8	V_{DD}	PWR	V_{DD} positive power supply.



* External crystal components are optional.
Device contains on-chip loadcapacitors
and feedback resistor.

Figure 1

Note:
The series resistor, R_s, sets the signal swing and the pull-up resistor, R_x, sets reference bias level, rise and fall times, and duty cycle of the signal waveform.

The recommended values for R_t and R_s are:

R_t = 50 or 25 Ohms, R_s = 8 to 12 Ohms.

Absolute Maximum Ratings

AV_{DD}, V_{DD} referenced to GND 7V
Operating temperature under bias ..... 0 to +70 °C
Storage temperature ..... -65 to +150 °C
Voltage on I/O pins referenced to GND ..... GND - 0.5 V to V_{DD} + 0.5 V
Power dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Specifications at 3.3V

VDD = 3.3V ±10%, T_A = 0-70 °C, unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
Input Low Voltage	V_{IL}		-	-	0.2V	V
Input High Voltage	V_{IH}		0.7 V_{DD}	-	-	V
Input Low Current[2]	I_{IL}	V = 0	-5.0	0	5.0	µA
Input High Current	I_{IH}	VIN = VDD	-5.0	0	5.0	µA
Input Pull-up Resistor Value[2]	R_{PU}	V_{IN} = V_{DD}-1 V	50.0	140.0	400.0	K Ohms
Output Impedance[1]	R_{OUT}		-	5.0	10.0	Ohms
Supply Current	I_{DD}	Unloaded	-	47.0	60.0	mA

Notes:
1 Parameter is guaranteed by design and characterization. Not subject to product testing.
2 The pull-up on the OE pin is measured at V_{DD}-1 V. The pull-up current switches off at inputs << V_{DD}/3.

Electrical Characteristics at 3.3 V

VDD = 3.3V ±10%, T_A = 0-70 °C, unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Output Frequency	F_{OUT1}		60.0	250.0	280.0	MHz
Output Frequency	F_{OUT2}	V_{DD} ≥3.15	60.0	250.0	300.0	MHz
Output Signal Swing[1,2]	Vs		1.2	1.4	1.6	V
Output Asymmetry	Aco		-15.0	0	15.0	%
Locking Time[1]			-	2.0	10.0	ms
Output Skew[1]	Skew	RCLK2 to RCLK1	-	-	50.0	ps
Absolute Jitter[1]	T_{jabs}	@ 252 MHz 10,000 cycles RCLK2	-100.0	50.0	100.0	ps
		@ 252 MHz 10,000 cycles RCLK1	-150.0	60.0	150.0	ps
Cycle-to-Cycle Jitter[1] Peak-Peak	T_{jcc}	@ 252 MHz 8,250 cycles RCLK2	-	-	100.0	ps p-p
		@ 252 MHz 8,250 cycles RCLK1	-	-	150.0	ps p-p
Accumulated Jitter[1] over 3 Cycles Peak - Peak	T_{jtot3}	@ 252 MHz 10,000 intervals RCLK2	-	-	150.0	ps p-p
		@ 252 MHz 10,000 intervals RCLK1	-	-	180.0	ps p-p
Accumulated Jitter[1] over 40 Cycles Peak - Peak	T_{jtot40}	@ 252 MHz 10,000 intervals	-	150.0	250.0	ps p-p
Accumulated Jitter[1] over 256 Cycles Peak - Peak	$T_{jtot256}$	@ 252 MHz 10,000 intervals	-	-	300.0	ps p-p
Narrowband Signal to Noise Ratio[1]	SNR_n	@ 252 MHz	-40.0	-	-	dBc
Narrowband Cut-off Frequency[1]	f_n	@ 252 MHz	-	-	50.0	MHz
Wideband Signal to Noise Ratio[1]	SNRw	@ 252 MHz	-100.0	-	-	dBc/Hz
Duty Cycle[1,2]		@ 50%/V_{REF}	45.0	50.0	55.0	%
Output Rise and Fall Time[1,2]	T_R, T_F	20-80%	300.0	-	500.0	ps

Notes:

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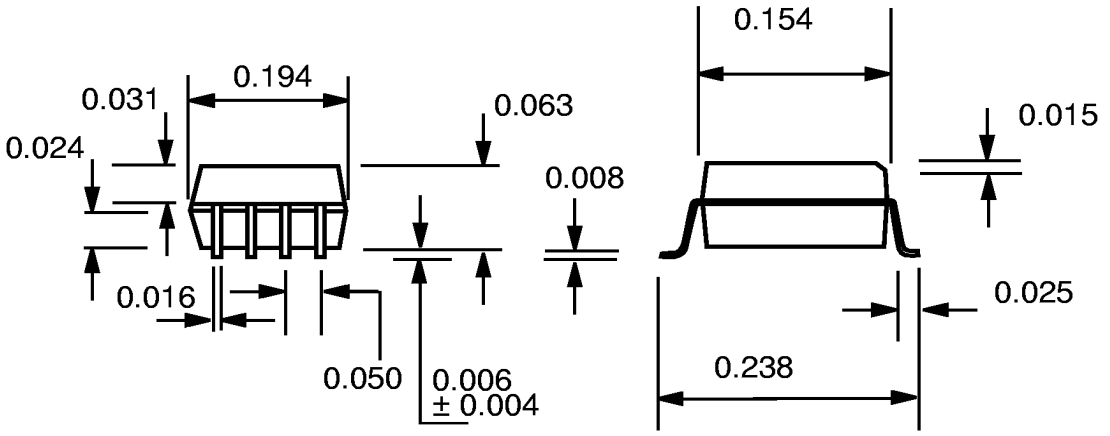
2 See Figure 1 page 3



8-Pin SOIC

Ordering Information

ICS9111M-01

Example:

ICS XXXX M-PPP

Pattern Number (2 or 3-digit number

Package Type
M =SOIC

Device Type (consists of 3 or 4-digit numbers)

Prefix
ICS, AV=Standard Device