Integrated Circuit Systems, Inc.

ICS9536-01

Advanced Information

1.0625GHz CMOS Fibre Channel Transceiver

General Description

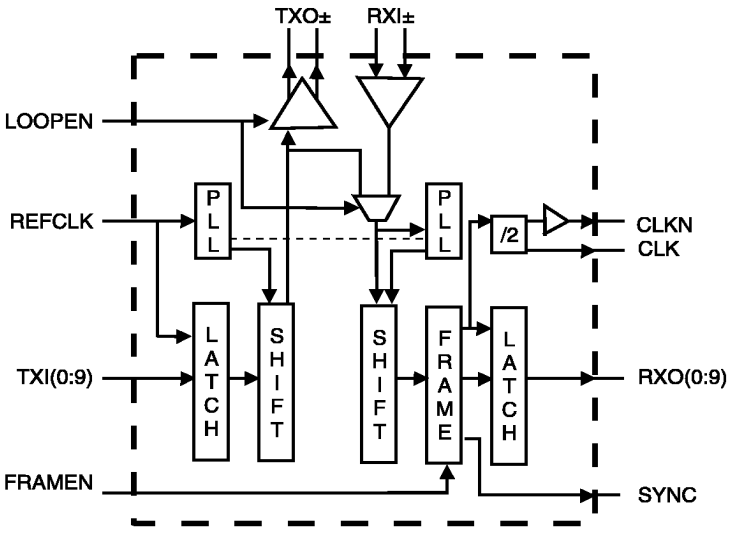
The **ICS9536-01** is an integrated 1GHz CMOS fibre channel transceiver, including TX clock generation and 10-bit parallel to serial conversion plus RX clock recovery and serial to 10-bit parallel conversion, with comma character recognition and selectable frame synchronization. An internal loop-back function provides aid in system evaluation and testing.

The **ICS9536-01** supports data rates up to 1.0625GHz and is fully compliant with ANSI X3.230-1994 (FC-0) standards. The device is pin compatible with standard transceivers but offers significantly lower power consumption and cost when compared to bipolar or GaAs technologies.

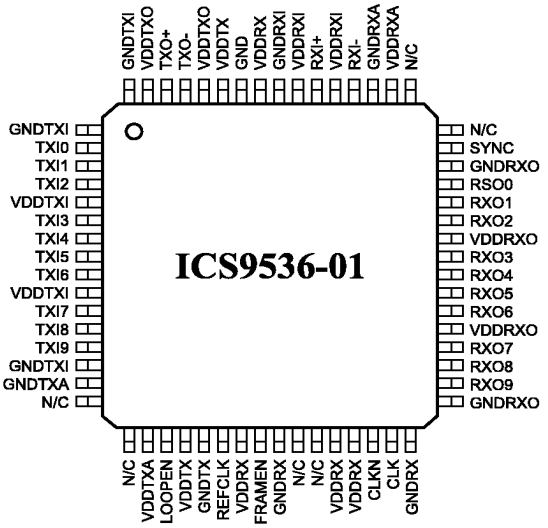
Features

- CMOS technology provides lowest cost and power
- Pin compatible with HDMP-1536 (Bipolar) and VSC7125 (GaAs) fibre channel transceivers
- ANSI X3.230-1994 (FC-0) compliant
- 1.0625GHz differential transmit and receive
- 106.25MHz 10-bit parallel data interface
- Integrated PLLs require no external components
- 64 pin QFP package, 10x10mm body, 2mm high

Block Diagram



Pin Configuration



64-pin QFP

Functionality

3.15-3.65V, 0-85°C
REFCLK=106.25MHz

LOOPEN	FRAMEN	TXO	RXI	SYNC	OPERATING MODE
0	0	Active	Active	Static	TX and RX without auto sync
0	1	Active	Active	Active	TX and RX with auto sync
1	0	Static	Ignore	Static	Internal loopback W/O auto sync
1	1	Static	Ignore	Active	Internal loopback W/ auto sync

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Transmitter Functional Description:

The transmitter accepts 10-bit wide TTL parallel data over a high speed line, as specified for the FC-0 layer of the Fibre Channel standard. Per the Fibre Channel specification, the parallel data is expected to be coded using an 8B/10B encoding scheme with special reserve characters required for link management purposes.

Transmitter Clocking:
The transmitter clock, REFCLK, is based on a user supplied reference clock. The clock recovery implemented in the receiver multiplies the REFCLK input frequency of 106.25MHz to 1062.5MHz. It is expected to be 106.25MHz and be properly aligned to the incoming parallel 10 bit wide TTL data at inputs TX[0:9]. The Transmitter Section Timing section illustrates clocking data into the transmit input bus which is latched on the positive edge of REFCLK . A PLL clock multiplier from REFCLK is used to synthesize the 1062.5MHz clock necessary for the high speed serial transmitter output.

Transmission Character Interface:
An encoded 10 bit word is defined as a transmission character. This 10 bit character, or transmission character is latched on the rising edge of REFCLK. The data is serialized, where the parallel data ,TX[0:9], is multiplexed into the 1062.5MB serial data stream and transmitted on the TX differential outputs at a baud rate of ten times the frequency of the REFCLK input. TX[0]0 is transmitted first and represents the least significant bit, and TX[9] is the most significant bit which is transmitted last.

Figure 1 illustrates the Mapping of the Transmission Character.

Receiver Functional Description:

The receiver in the ICS9536-01 receives serial input data, and establishes the correct frequency and phase relationships by recovering the bit and byte clocks.

Receiver Clocking:
The receive PLL phase aligns with the incoming data. The recovered clocks are one twentieth of the receiver data stream (53.125MHz) where a rising transition of CLK corresponds to a new word on the receiver output RXO(0:9) These byte clocks are 180 degrees out of phase with each other and are designed such that demultiplexing of a 10-bit data characters into a 20-bit halfword in the controller chip is straightfoward. The ICS9536-01 will continue to generate all the output clocks even if input data is not present. The CLK and CLKN output frequency cannot differ from their expected frequency by not more than +-1.5%.

Frame Demux, Byte Sync
By asserting FRAMEN high, received data synchronization is enabled such that the ICS9536-01 constantly examines the serial data for the presence of the "comma" character, "0011111XXX". Realignment of the 7-bit comma character will occur if the "comma" character's value is shifted in time relative to CLK and CLKN. More specifically, realignment will occur if the comma is not aligned with the rising edge of CLKN (or falling edge of CLK), or the comma straddles the boundary between two 10-bit transmission characters.

When FRAMEN is asserted, a comma character is detected and realignment of the receiver byte clocks , CLK and CKLN, may be necessary. These clocks will be fully aligned by the start of the second 4-byte set of data, such that the second comma character received will be aligned with the rising edge of CLKN. When a comma character is encountered, SYNC output is driven high, indicating that a possible realignment of the data may have occurred. The SYNC pulse is driven high, during the comma character, for a duration equal to one word of data, or one half of an CLK period.

Figure 1: Transmission Order and Mapping to Fibre Channel Character

Parallel Data Bits	T9	T8	T7	T6	T5	T4	T3	T2	T1	T0
8B/10B bit Position	j	h	g	f	i	e	d	c	b	a
Comma Character	X	X	X	1	1	1	1	1	0	0

Last Data Bit Transmitted

First Data Bit Transmitted

Output and Input Selection:

Enabling LOOPEN provides for internal loopback of the high speed serial input signal to the receiver. When the loop back feature is enabled the transmit output pins (TXO+-) toggles at the incoming data rate and the receiver's input multiplexer switches to receive the transmit serial output. This function is used for system testing exclusive of the transmission medium.

Transmitter Timing Characteristics

T_a=0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{setup}	Setup Time to Rising Edge of REFCLK	2			nsec
t_{hold}	Hold Time to Rising Edge of REFCLK	1.5			nsec
t_txlat[1]	Transmitter Latency		TBD		nsec
			TBD		bits

Note 1: The transmitter latency, as shown in Figure 3, is defined as the time between the latching in of the parallel data word (as triggered by the rising edge of the transmit byte clock. REFCLK) and the transmission of the first serial bit of that parallel word (defined by the rising edge of the first bit transmitted).

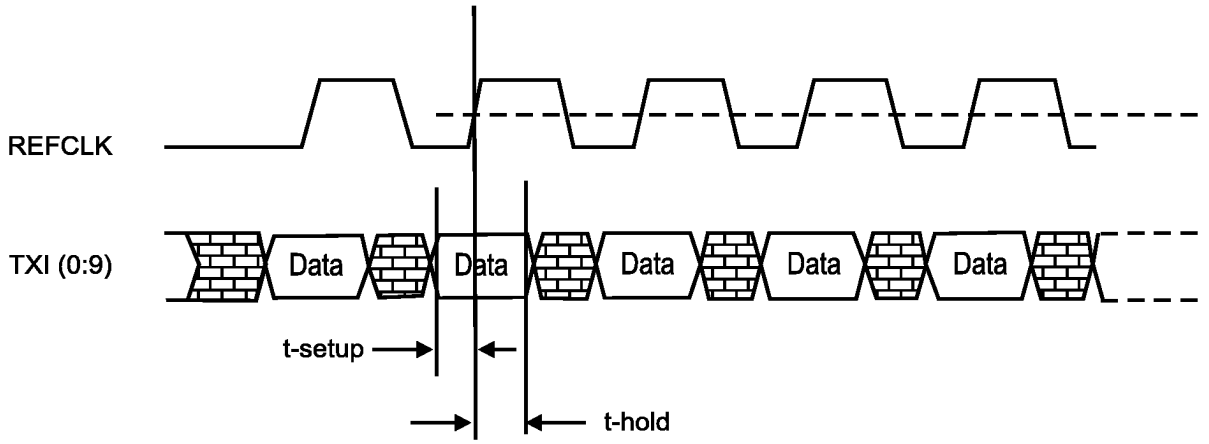

Figure 2: Transmitter Section Timing

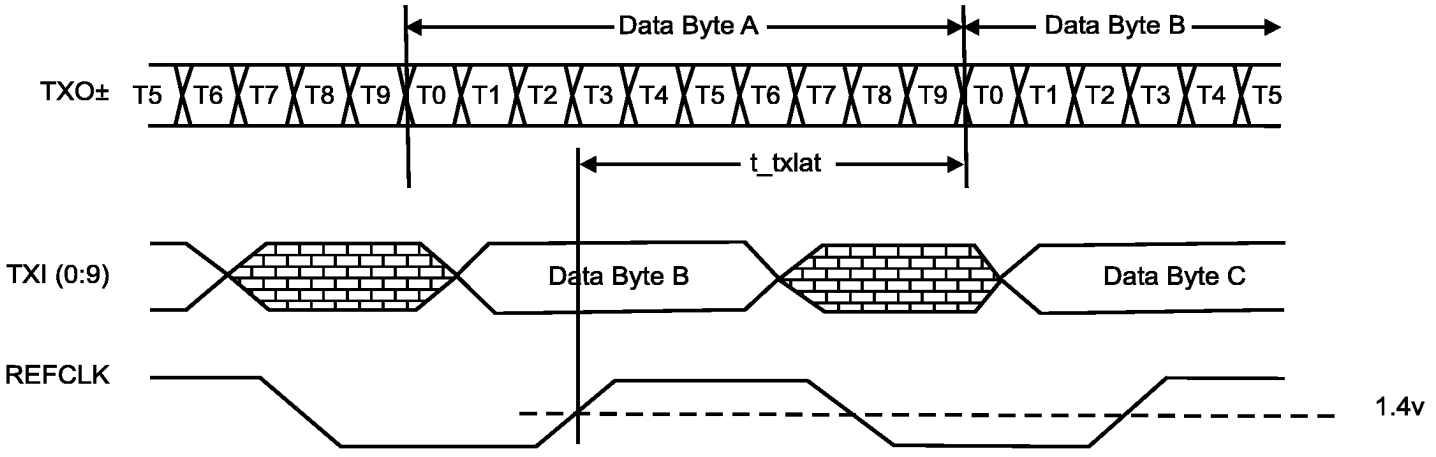

Figure 3: Transmitter Latency

Transmitter Timing Characteristics

T_a=0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max.	Units
b_sync[1,2]	Bit Sync time			2500	bits
f_lock[2]	Frequency Lock time			500	µsec
f_lock_rate[2]	Frequency Lock Rate		TBD		kHz/µsec
tvalid_before	Time data valid before rising edge of CLK		TBD		nsec
tvalid_after	Time data valid after rising edge of CLK		TBD		nsec
tduty	CLK Duty Cycle	40		60	%
tA-B	Rising Edge time difference	8.9	9.4	9.9	nsec
t_rxlat[3]	Receiver Latency		TBD		nsec
			TBD		bits

Notes:

1. This is the recovery time for input phase jumps.
2. The CLK clock skew is calculated as tA-B(max) -tA-B(min).
3. The receiver latency, as shown in Figure 4 , is defined as the time between receiving the first serial bit of a parallel data word (as defined as the first edge of the first serial) and the clocking out of that parallel word (defined by the rising edge of the receive byte clock, CLK).

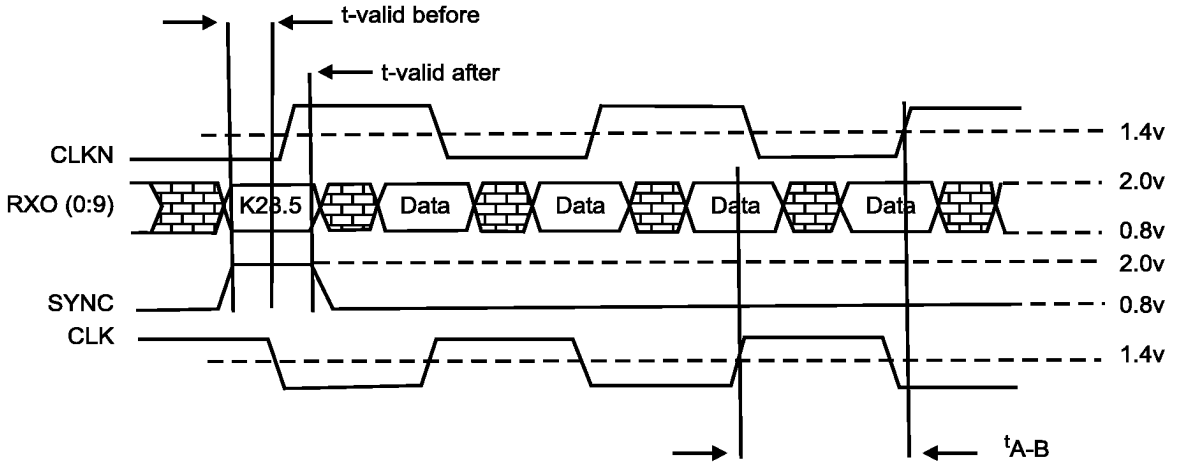

Figure 4: Receiver Section Timing

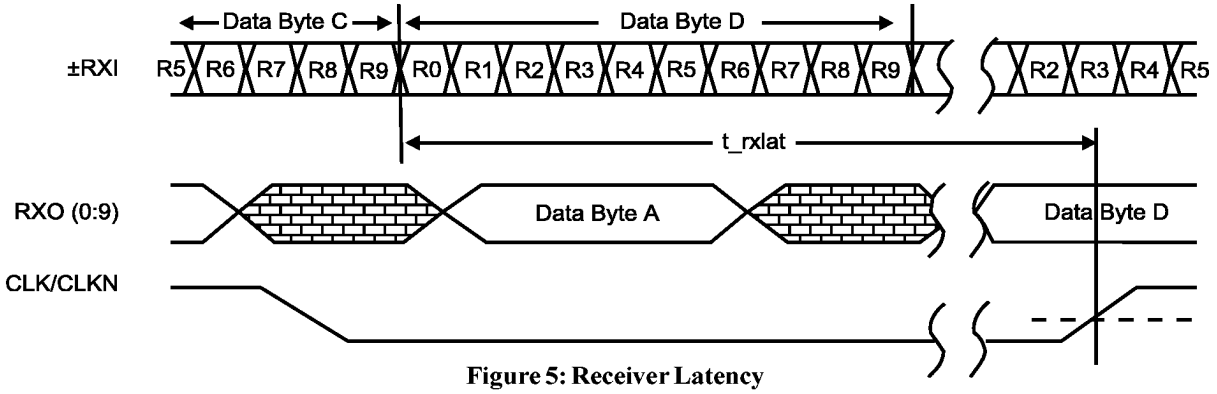

Figure 5: Receiver Latency

Pin Description ICS9536-01

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1, 14	GNDTXI	GND	TTL Transmitter Ground: Normally 0 volts.
2, 3, 4, 6, 7, 8, 9, 11, 12, 13	TXI (0:9)	IN	Data Inputs: One, 10 bit, pre-encoded data byte. TXI(0) is the first bit transmitted. TXI(0) is the least significant bit.
5, 10	VDDTXI	PWR	TTL Power Supply: Normally 3.3V. Used for all TTL transmitter input buffer cells.
15	GNDTXA	PWR	Analog Ground: Normally 0V. Used to provide a clean ground plane for the PLL and high-speed analog cells.
16, 17, 48, 49	N/C	N/C	Not connected
18	VDDTXA	PWR	Analog Power Supply: Normally 3.3V. Used to provide a clean supply line for the PLL and high speed analog cells.
19	LOOPEN	IN	Loopback enable Input: When set high, the high speed serial signal is internally wrapped from the transmitter's serial loopback outputs back to the receiver's loopback inputs. When set low, ±TXO outputs and ±TXI inputs are active.
20, 59	VDDTX	PWR	Logic Power Supply: Normally 3.3V. Used for internal transmitter logic. It should be isolated from the noisy TTL supply as well as possible.
21, 25, 58	GNDTX	PWR	Logic Ground: Normally 0V. This ground is used for internal logic. It should be isolated from the noisy TTL ground as well as possible.
22	REFCLK	IN	Reference Clock and Transmit Byte Clock: A 106.25MHz clock supplied by the host system. The transmitter section accepts this signal as the frequency clock. It is multiplied by 10 to generate the serial bit clock and other internal clocks. The transmit side also uses this clock as the transmit byte clock for the incoming parallel data TXI(0)..TXI(9).
23, 28, 57	VDDRX	PWR	Logic Power Supply: Normally 3.3V. Used for internal receive logic. It should be isolated from the noisy TTL supply as well as possible.
24	FRAMEN	IN	Enable Byte Sync Input: When high, turns on the internal byte sync function to allow clock synchronization to a comma character (or a K28.5 character) of positive disparity (0011111010). When the line is low, the function is disabled and will not reset registers and clocks, or strobe the BYTSYNC line.

Pin Description ICS9536-01 Continued:

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
29, 37, 42	VDDRX	PWR	TTL Power Supply: Normally 3.3V. Used for all TTL receiver output buffer cells.
30, 31	CLK CLKN	OUT	Receiver Byte Clocks: The receiver section recovers two 53.125MHz receive byte clocks. These two clocks are approximately 180 degrees out of phase. Their receiver parallel data outputs are alternatively clocked on the rising edge of theese clocks. CLK aligns and outputs the comma character (for byte alignment) when detected.
32, 33, 46	GNDRX	PWR	TTL Receiver Ground: Normally 0V. Used for the TTL output cells of the receiver section.
45, 44, 43, 41, 40, 39, 38, 36, 35, 34	RXO (0:9)	OUT	Data Outputs: One 10 bit data byte. RS(0) is the first bit received. RS(0) is the least signficant bit.
47	SYNC	OUT	Byte Sync Output; An active high output. Used to indicate detection of either a comma character or a K28.5 special character of positive disparity. It is only active when FRAMEN is enable.
50	VDDRXA	PWR	Analog Power Supply: Normally 3.3V. Used to provide a clean supply line for the PLL and high speed analog cells.
51	GNDRXA	PWR	Analog Ground: Normally 0V. Used to provide a clean ground plane for the receiver PLL and high-speed analog cells.
52 54	RXI- RXI+	IN	Serial Data Inputs: High speed inputs. Serial data is accepted from the ±DIN inputs when LOOPEN is low.
53, 55	VDDRXI	PWR	High Speed Supply: Normally 3.3V. Used only for the high speed reciever cell (HS_IN). Noise on this line should be minimized for best operation.
56	GNDRXI	PWR	Ground: Normally 0V.
60, 63	VDDTX0	PWR	High Speed Supply: Normally 3.3V. Used by the transmitter side for the high speed circuitry. Noise on this line should be minimized for best operation.
61 62	+DOUT -DOUT	OUT	Serial Data Outputs: High speed outputs. These lines are active when LOOPEN is set low. When LOOPEN is set high, these outputs toggle at the incoming data rate.
64	GNDTX	PWR	Ground: Normally 0V.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Guaranteed Operating Rates

Ta=0°C to +70°C, V_{CC} = 3.15V to 3.45V

Parallel Clock Rate (MHz)		Serial Baud Rate (MBaud)	
Min.	Max.	Min.	Max.
106.20	106.30	1062.0	1063.0

Transceiver Reference Clock Requirements

Ta=0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max	Unit
f	Nominal Frequency (for Fibre Channel Compliance)	106.20	106.25	106.30	MHz
F_{tol}	Frequency Tolerance	-100		+100	ppm
Symm	Symmetry	40		60	%

DC Electrical Characteristics

Ta=0°C to +70°C, V_{CC} = 3.15V to 3.45V

Symbol	Parameter	Min.	Typ.	Max	Unit
$V_{IH,TTL}$	TTL Input High Voltage Level, Guaranteed high signal for all inputs	2		V_{CC}	V
$V_{IL,TTL}$	TTL Input Low Voltage Level, Guaranteed low signal for all inputs	0		0.8	V
$V_{OH,TTL}$	TTL Output High Voltage Level, I_{OH} = 400µA	2.4		V_{CC}	V
$V_{OL,TTL}$	TTL Output Low Voltage Level, I_{OL} = 1mA	0		0.6	V
$I_{IH,TTL}$	Input High Current (Magnitude), V_{IN} = V_{CC}		.004	40	µA
$I_{IL,TTL}$	Input Low Current (Magnitude), V_{IN}= 0 volts		295	600	µA
$I_{CC,TRx}$[1,2]	Transceiver V_{CC} Supply Current, Ta = 25°C		195		mA

Notes:

1, Measurement Conditions: Tested sending 1062.5 MBd PRBS 2/7-1 sequence from a serial BERT with both TXO outputs biased with 150Ω resistors.

2, Typical specified with VOC = 3.3 volts, maximum specified with VOC = 3.45 volts.

Advanced Information

Application Comparison Between; Vitesse VSC7125, HDMP-1536 and ICS9536-01

Pinout Difference:

	HDMP-1536		VITESSE VSC7125		
PIN NUMBER	PIN LABEL	DESCRIPTION	PIN LABEL	DESCIRPTION	TO USE ICS9536 YOU MUST PERFORM;
18	VCC_TXA	TX Analog Supply, 3.3V	TEST 1	Factory Test Pin. Nominally tied to +3.3V.	Tie to VDD Note:1
20	VCC_TX	TX Analog Supply, 3.3V	TEST2	Factory Test Pin. Nominally tied to +3.3V.	Tie to VDD Note:1
23	VCC_RX	RX PECL Logic Supply +3.3V.	TEST3	Factory Test Pin. Nominally tied to +3.3V.	Tie to VDD Note:1
50	VCC_RXA	RX Analog Supply +3.3V.	VDD	Digital Supply, +3.3V.	Tie to VDD Note:1
57	VCC_RX	RX PECL Logic Supply +3.3V.	VDDANA	Analog Power Supply +3.3V	Tie to VDD Note:1
64	GND_TXHS	High Speed Ground	no connect	Pin is not used	Ground this pin.

Note:
1. Use 0.1µf bypass capacitor.

Comma Detection or Word Alignment:

The VSC7125 provides 7-bit comma character recognition or word alignment. When an improperly aligned comma is encountered, the internal data is shifted such that the comma character is aligned properly by the start of the second set of the 4-byte sequence.

When a comma character is detected in the ICS9536, realignment of the receiver clocks can be performed. These clocks are stretched, such that correct alignment occurs at the start of the second 4-byte data set. The second comma character, occurring in the second 4-byte data set will be aligned with the rising edge of the byte clock, CLK.

Termination:

The Vitesse data sheet for the VSC715 does not explicitly describe termination requirements in a detailed fashion (it specifies 75Ω).

The termination required for ICS9536 is: