Integrated Circuit Systems, Inc.

ICS9147-08

Frequency Generator & Integrated Buffers for 686 Series CPUs

General Description

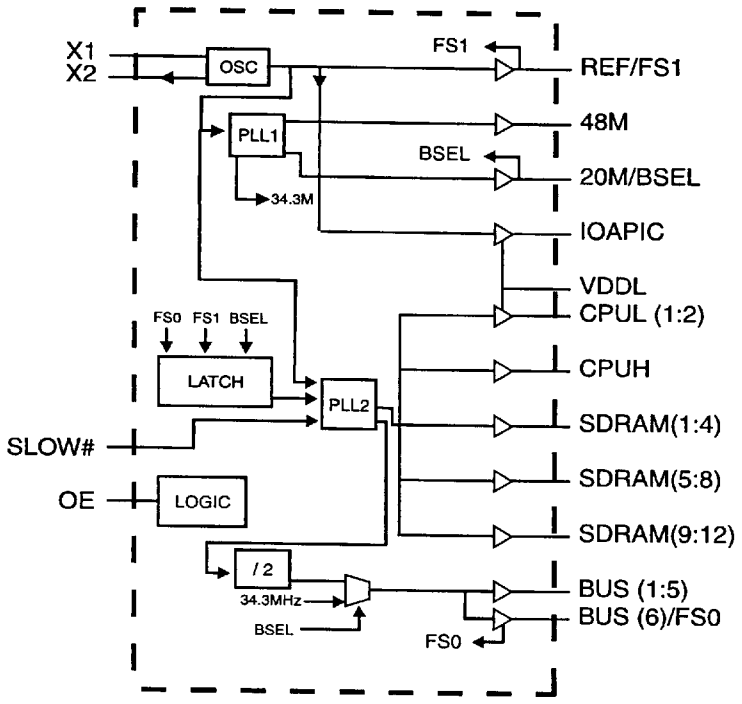
The **ICS9147-08** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel Pentium and PentiumPro, AMD or Cyrix processors. Three bidirectional I/O pins (FS0, FS1, BSEL) are latched at power-on to the functionality table. The Six BUS clocks can be selected as either synchronous at 1/2 CPU speed or asynchronous at 34.3MHz selected by BSEL latched input.The inputs provide for test mode conditions to aid in system level testing. An output enable pin tristates all outputs for system testing. The slow clock mode will transition the CPU, SDRAM and PCI clocks from 60 or 66.6 MHz CPU to half speed when SLOW# input is low.

High drive BUS and SDRAM outputs typically provide greater than 1V/ns slew rate into 30pF loads. CPU outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates. Seperate buffer supply pin VDDL allows for nominal 3.3V voltage or reduced voltage swing (from 2.9 to 2.5V) for CPUL (1:2) and IOAPIC outputs.

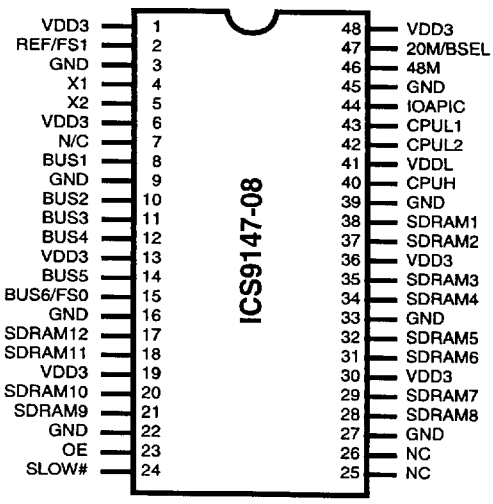
Features

- Total of 15 CPU speed clocks:
  - Two copies of CPU clock with VDDL (2.5 to 3.3V)
  - Twelve (12) SDRAM (3.3v) plus one CPUH (3.3V) clocks
- Six copies of PCI clock (synchronous with CPU clock/2 or asynchronous 34.3 MHz)
- Slow clock mode ramps CPU PLL to half speed (from 60 or 66.6 MHz)
- 250ps output skew window for CPU andSDRAM clocks and 500ps window BUS clocks.
- CPU clocks to BUS clocks skew 1-3ns (CPU early)
- Two copies of Ref. clock @14.31818 MHz (One driven by VDDL as IOAPIC)
- One 48 MHz (3.3 V TTL) for USB support and single 20 MHz for Data Communications
- ±100PPM Freq accuracy with better than: ±30PPM initial XTAL accuracy, and ±70PPM due to temp , aging and load CAP variation.
- Separate V_{DDL} for CPUL (1:2) clock buffers and IOAPIC to allow 2.5V output (or Std. Vdd)
- 3.0V – 3.7V supply range w/2.5V compatible outputs
- 48-pin SSOP package

Block Diagram



Pin Configuration



48-Pin SSOP

Pentium is a trademark of Intel Corporation

Functionality with (14.31818 MHz input)

Address Select			CPUL (1:2) CPUH SDRAM (1:12)	BUS (1:6) (MHz)		20M (MHz)	48M (MHz)
SLOW#	FS1	FS0	(MHz)	BSEL=1	BSEL=0	(MHz)	(MHz)
0	0	0	30.0	15.0	34.3	20	48
0	0	1	33.3	16.7	34.3	20	48
0	1	0	83.3	41.65	34.3	20	48
0	1	1	TEST/2	TEST/4	TEST/7	TEST/12	TEST/5
1	0	0	60.0	30.0	34.3	20	48
1	0	1	66.6	33.3	34.3	20	48
1	1	0	75.0	37.5	34.3	20	48
1	1	1	100.0	50.0	34.3	20	48

**Test: is the frequency applied to the X1 input. Can be crystal or tester generated clock overriding crystal at X1 pin.

Output Enable (pin 13) Function

OE	CPUL, CPUH, SDRAM, BUS, 20, 48, REF
0	Tristate
1	Running

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF	OUT	Reference clock output*
	FS1	IN	Logic input frequency select Bit1*. Input latched at Poweron.
3, 9, 16, 22, 27, 33, 39, 45	GND	PWR	Ground.
4	X1	IN	Crystal input. Nominally 14.318 MHz. (External crystal load caps required)
5	X2	OUT	Crystal output. (External crystal load caps required)
41	VDDL	PWR	2.5 or 3.3V buffer power for CPUL and IOAPIC output buffers.
8, 10, 11, 12, 14,	BUS (1:5)	OUT	BUS clock outputs. see select table for frequency
15	BUS6	OUT	BUS clock output. See select table for frequency.*
	FS0	IN	Logic input frequency select Bit0.*. Input latched at Poweron.
23	OE	IN	Logic input for output enable, tristates all outputs when low. Has a 40Kohm pullup to VDD.
24	SLOW#	IN	Logic input to frequency select table, has 40k ohm pullup to VDD, will smoothly transition 60 or 66.6 MHz to half speed when input goes to low
47	20M	OUT	20 MHz fixed clock* (Freq is < 1PPM accurate with exact 14.318 MHz input)
	BSEL	IN	Logic input* for selecting synchronous or asynchronous BUS frequency- see table above. Input latched at Poweron.*
1, 6, 13, 19, 30, 36, 48	VDD	PWR	3.3 volt core logic and buffer power
17, 18, 20, 21, 28, 29, 31, 32, 34, 35, 37, 38	SDRAM (1:12)	OUT	SDRAM clocks at CPU speed. See select table for frequency.
40	CPUH	OUT	CPU clock operates at SDRAM VDD level (3.3V nom).
42, 43	CPUL (1:2)	OUT	CPU clock output clocks .See select table for frequency. Operates at down to 2.5V controlled by VDDL pin.
7, 25, 26	N/C	—	Pins not internally connected.
46	48M	OUT	48 MHz fixed clock output.
44	IOAPIC	OUT	Reference clock (14.318MHz) powered by VDDL, operating 2.5 to 3.3V.

* Bidirectional input/output pins, input logic level determined at internal power-on-reset are latched. Use 10Kohm resistor to program logic Hi to VDD or GND for logic low. Internal input has No pullup or pulldown.

Absolute Maximum Ratings

Supply Voltage ..... 7.0 V
Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V
Ambient Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 –70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}	Latched inputs and Fulltime inputs	-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}	Latched inputs and Fulltime inputs	$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN} = 0V (Fulltime inputs)	-28.0	-10.5	-	µA
Input High Current	I_{IH}	V_{IN}=V_{DD} (Fulltime inputs)	-5.0	-	5.0	µA
Output Low Current	I_{OL1a}	V_{OL} = 0.8V; CPU, SDRAM IOAPIC, REF, BUS; V_{DD2} = 3.3V	19.0	30.0	-	mA
	I_{OL1b}	V_{OL} = 0.8V; CPUL, IOAPIC; VDD2 = 2.5V	19.0	30.0		mA
Output High Current	I_{OH1a}	V_{OH} = 2.0V; CPU, SDRAM IOAPIC, REF, BUS; V_{DD2} = 3.3V	-	-26.0	-16.0	mA
	I_{OH1b}	V_{OH} = 2.0V; CPUL, IOAPIC; V_{DD2} = 2.5V		-12.5	-9.5	mA
Output Low Current	I_{OL2}	V_{OL} = 0.8V; for fixed 24, 48	16.0	25.0	-	mA
Output High Current	I_{OH2}	V_{OH} = 2.0V; for fixed 24, 48	-	-22.0	-14.0	mA
Output Low Voltage	V_{OL1a}	I_{OL} = 10mA; CPU, SDRAM IOAPIC REF, BUS;V_{DD2} = 3.3V	-	0.3	0.4	V
	V_{OL1b}	I_{OL} = 10mA; CPUL, IOAPIC; V_{DD2}=2.5V		0.3	0.4	V
Output High Voltage	V_{OH1a}	I_{OH} = -10mA; CPU, SDRAM, IOAPIC, REF, BUS; V_{DD} = 3.3V	2.4	2.8	-	V
	V_{OH1b}	I_{OH} = -10mA; CPUL, IOAPIC; VDD2=2.5V	1.95	2.1		V
Output Low Voltage	V_{OL2}	I_{OL} = 8mA; for fixed 24, 48MHz CLKs	-	0.3	0.4	V
Output High Voltage	V_{OH2}	I_{OH} = -8mA; for fixed 24, 48MHz CLKs	2.4	2.8	-	V
Supply Current	I_{DD}	@66.6 MHz; all outputs unloaded	-	120	180	mA

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

Electrical Characteristics at 3.3V

$V_{DD\,L}=V_{DD}=3.0-3.7V, T_A=0-70°C$ unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time[1]	Tr1	20pF load, 0.8 to 2.0V CPU, SDRAM, BUS & REF	-	0.9	1.5	ns
Fall Time[1]	Tf1	20pF load, 2.0 to 0.8V CPU, SDRAM, BUS & REF	-	0.8	1.4	ns
Rise Time[1]	Tr2	20pF load, 20% to 80% CPU, SDRAM, BUS & REF	-	1.5	2.5	ns
Fall Time[1]	Tf2	20pF load, 80% to 20% CPU, SDRAM, BUS & REF	-	1.4	2.4	ns
Rise Time[1]	Tr3	20pF load, 0.8 to 2.0V fixed 20 & 48 clocks	-	0.9	1.5	ns
Fall Time[1]	Tf3	20pF load, 2.0 to 0.8V fixed 20 & 48 clocks	-	1.1	1.5	ns
Rise Time[1]	Tr4	20pF load, 0.4 to 2.0V , CPUL with VDDL = 2.5V	-	2.0	2.5	ns
Fall Time[1]	Tf4	20pF load, 2.0 to 0.4V, CPUL with VDDL = 2.5V	-	1.6	2.5	ns
Duty Cycle[1]	Dt	20pF load @ VOUT=1.4V All clocks except 48MHz and REF	45	50	55	%
Duty Cycle[1]	DT2	20pF load @ VOUT=1.4V 48MHz and REF outputs	40	50	60	%
Jitter, One Sigma[1]	Tjis1	CPU & BUS Clocks; Load=20pF, SDRAM; Load = 30pF, VDDL = 3.3 or 2.5V FOUT=25 MHz, BSEL=1	-	50	150	ps
Jitter, Absolute[1]	Tjab1	CPU & BUS Clocks; Load=20pF, SDRAM; Load = 30pF, VDDL = 3.3 or 2.5V FOUT≥25 MHz, BSEL=1	-250	-	250	ps
Jitter, One Sigma[1]	Tjis2	Fixed CLK; Load=20pF	-	1	3	%
Jitter, Absolute[1]	Tjab2	Fixed CLK; Load=20pF	-5	2	5	%
Jitter, Cycle to Cycle[1]	Tcc1	CPU Clocks, Load=20pF BSEL=1		-	250	ps
Jitter, Cycle to Cycle[1]	Tcc2	CPU Clocks, Load=20pF BSEL=1 VDDL=2.5V		-	350	ps
Input Frequency[1]	Fi		12.0	14.318	16.0	MHz
Ratio of nominal to output frequency	Fout1	With input driven at 14.31818MHz to 20.0, 48.0MHz	-1	-0.1	+1	ppm
Logic Input Capacitance[1]	CIN	Logic input pins	-	5	-	pF
Crystal Oscillator Capacitance[1, 2]	CINX	X1, X2 pins	2	4	6	pF
Power-on Time[1]	ton	From VDD=1.6V to 1st crossing of 66.6 MHz VDD supply ramp < 40ms	-	2.5	4.5	ms
Clock Skew Window[1]	Tsk1	CPU to CPU or SDRAM; Load=20pF; @1.4V (Same VDD)	-	150	250	ps
Clock Skew Window[1]	Tsk2	BUS to BUS; Load=20pF; @1.4V	-	300	500	ps
Clock Skew Window[1]	Tsk3	CPU to BUS; Load=20pF; @1.4V (CPU is early)	1	2.1	3	ns
Clock Skew Window[1]	Tsk4	CPUL to BUS, VDDL=2.5V Vth=1.25, CPUL (BUS Vth=1.4V)	0.25	0.70	2.25	ns
Clock Skew Window[1]	Tsk5	SDRAM, CPUH (@3.3V, Vth=1.4V) to CPUL (@2.5V Vth=1.25V) Load=20pF (2.5V CPUL is late)	350	600	850	ps

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.
Note2: Crystal load caps must be connected externally.

Shared Pin Operation - Input/Output Pins

Pins 2, 15 and 47 on the **ICS9147-08** serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 4-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm(10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figs. 1 and 2 show the recommended means of implementing this function. In Fig. 1 either one of the resistors is loaded onto the board (selective stuffing) to configure the device's internal logic. Figs. 2a and b provide a single resistor loading option where either solder spot tabs or a physical jumper header may be used.

These figures illustrate the optimal PCB physical layout options. These configuration resistors are of such a large ohmic value that they do not effect the low impedance clock signals. The layouts have been optimized to provide as little impedance transition to the clock signal as possible, as it passes through the programming resistor pad(s).

Test Mode Operation

The **ICS9147-08** includes a production test verification mode of operation. This requires that the FS1 and FS0 pins be programmed to a logic high and the SLOW# pin be programmed to a logic low (see Shared Pin Operation section). In this mode the device will output the following frequencies.

Pin		Frequency
REF, IOAPIC		REF
48MHz		REF/5
20MHz		REF/12
CPU, SDRAM		REF2
BUS	BSEL=1	REF/4
BUS	BSEL=0	REF/7

Note: REF is the frequency of either the crystal connected between the devices X1and X2, or, in the case of a device being driven by an external reference clock, the frequency of the reference (or test) clock on the device's X1 pin.

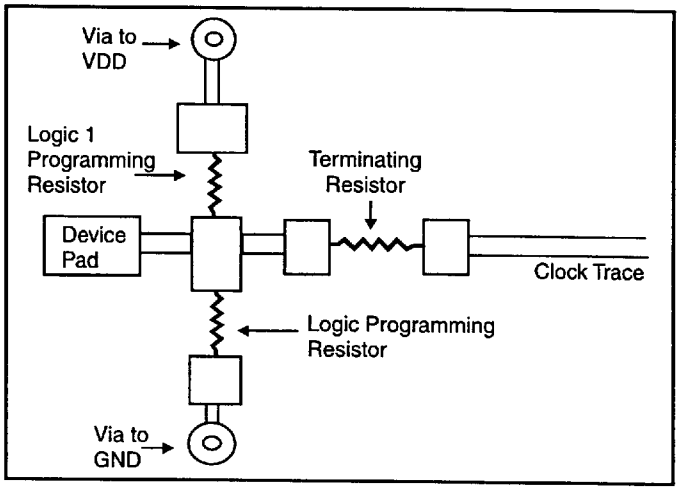


Fig. 1

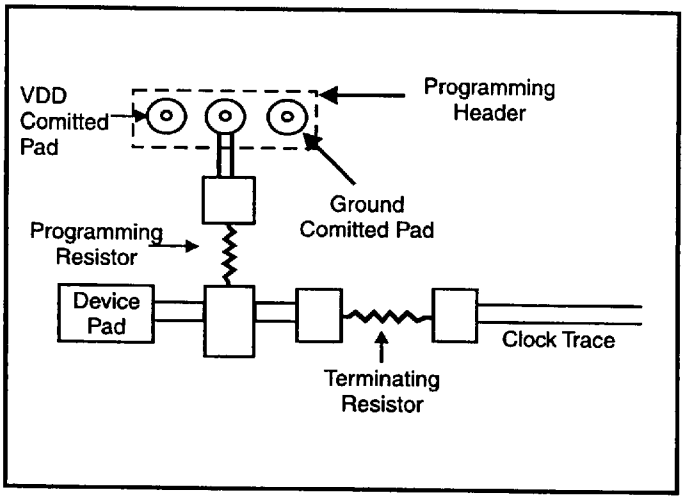


Fig. 2a

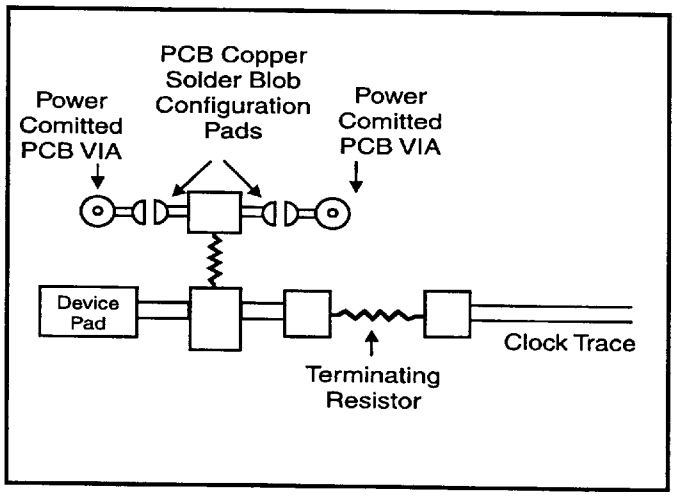
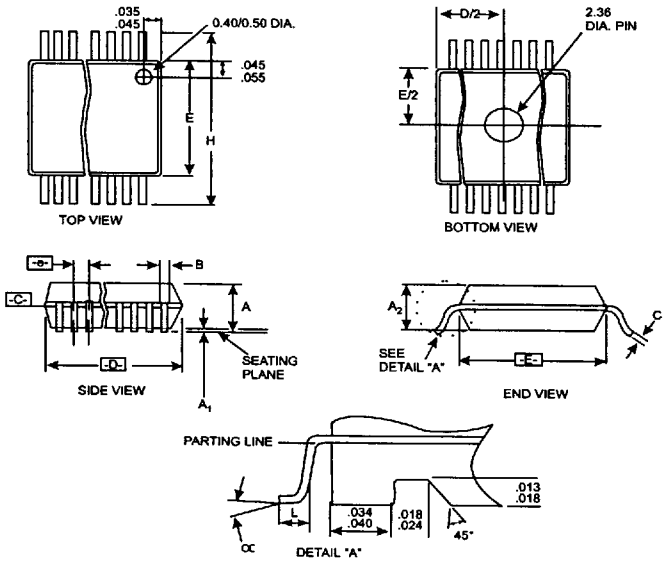


Fig. 2b



SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016	AD	.720	.725	.730	56
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9147F-08

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS = Standard Device