Integrated Circuit Systems, Inc.

ICS9148-01

Advanced Information

Frequency Generator & Integrated Buffers for PENTIUM™

General Description

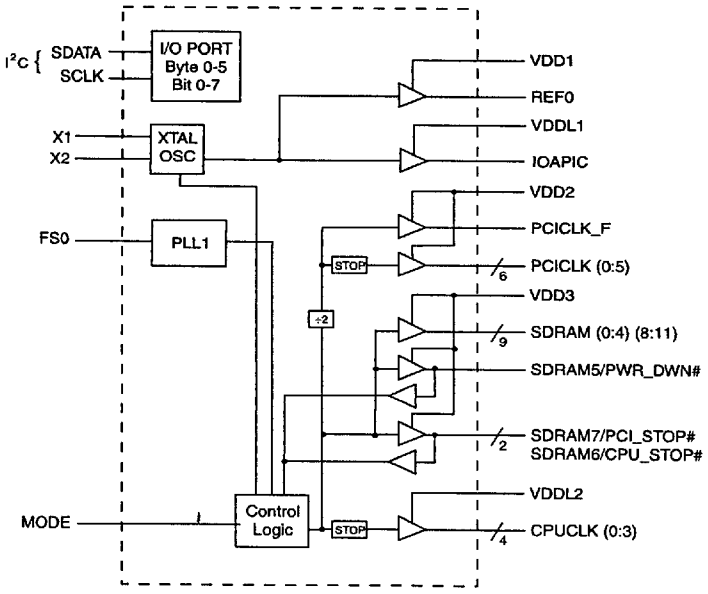
The **ICS9148-01** generates all clocks required for high speed RISC or CISC microprocessor systems such as Intel PentiumPro. Two different reference frequency multiplying factors are externally selectable with smooth frequency transitions. An output enable is provided for testability.

High drive BCLK outputs typically provide greater than 1V/ns slew rate into 30pF loads. PCLK outputs typically provide better than 1V/ns slew rate into 20pF loads while maintaining 50±5% duty cycle. The REF clock outputs typically provide better than 0.5V/ns slew rates.

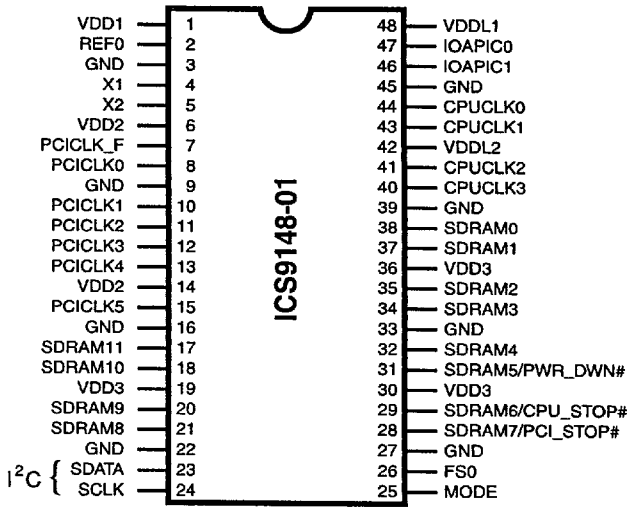
Features

- Generates four processor, six bus, one 14.31818MHz and 12 SDRAM clocks.
- Synchronous clocks skew matched to 250ps window on CPU, SDRAM and 500ps window on BUS clocks.
- CPUCLKs to BUS clocks skew 1-4 ns (CPU early)
- Test clock mode eases system design
- Selectable multiplying ratios
- Custom configurations available
- Output frequency ranges to 100MHz (depending on option)
- 3.0V – 3.7V supply range
- PC serial configuration interface
- Power Management Control Input pins
- 48-pin SSOP package

Block Diagram



Pin Configuration



48-Pin SSOP

Functionality

FS0	CPUCLK, SDRAM (MHz)	X1, REF (MHz)	PCICLK (MHz)
0	60.0	14.318	30
1	66.6	14.318	33.3

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Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	REF0	OUT	14.318 MHz reference clock outputs.
3, 9, 16, 22, 27, 33, 39, 45	GND	PWR	Ground.
4	X1	IN	Crystal input, has internal crystal load cap
5	X2	OUT	Crystal output, has internal load cap and feedback resistor to X1
25	MODE	IN	Mode select pin for enabling power management features.
7	PCLK_F	OUT	Free running BUS clock during PCI_STOP# = 0.
8, 10, 11, 12 13, 15	PCICLK (0:5)	OUT	BUS clock outputs.
26	FS0	IN	Select pin for enabling 66.6 MHz or 60 MHz.
23	SDATA	IN	Serial data in for serial config port.
24	SCLK	IN	Clock input for serial config port.
1, 6, 14, 19, 30, 36,	VDD1, VDD2, VDD3	PWR	Nominal 3.3V power supply, see power groups for function.
17, 18, 20, 21, 32, 34, 35, 37, 38	SDRAM (0:4) (8:11)	OUT	SDRAM clocks 60/66.6MHz.
42, 48	VDDL2, VDDL1	PWR	CPU and IOAPIC clock power supply, either 2.5 or 3.3V nominal
40, 41, 43, 44	CPUCLK (0:3)	OUT	CPU output clocks, powered by VDDL2 (60 or 66.6 MHz)
46, 47	IOAPIC (0:1)	OUT	IOAPIC clock output, (14.318 MHz) powered by VDDL1
28	SDRAM7	OUT	SDRAM clock 60/66.6 MHz selected
	PCI_STOP#	IN	Halts PCICLK (0:5) at logic "0" level when low
29	SDRAM6	OUT	SDRAM clock 60/66.6 MHz selected
	CPU_STOP#	IN	Halts CPUCLK clocks at logic "0" level when low
31	SDRAM5	OUT	SDRAM clock 60/66.6 MHz selected
	PWR_DWN#	IN	Powers down chip, active low

Power Groups

VDD1 = REF0, X1, X2
VDD2 = PCICLK_F, PCICLK (0:5)
VDD3 = SDRAM (0:4) (8:11) SDRAM5/PWR_DWN#,
SDRAM6/CPU_STOP#, SDRAM7/PCI_STOP#, supply for PLL Core.
VDDL1 = IOAPIC (0:1)
VDDL2 = CPUCLK (0:3)

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Power-On Conditions

SEL 66/60#	MODE	PIN #	DESCRIPTION	FUNCTION
1	1	44, 43, 41, 40	CPUCLKs	66.6 MHz - w/serial config enable/disable
		38, 37, 35, 34, 32, 31, 21, 20, 18, 17, 29, 28	SDRAM	66.6 MHz - All SDRAM outputs
		8, 10, 11, 12, 14, 15, 7	PCICLKs	33.3 MHz - w/serial config enable/disable
0	1	44, 43, 41, 40	CPUCLKs	60 MHz - w/serial config enable/disable
		38, 37, 35, 34, 32, 31, 21, 20, 18, 17, 29, 28	SDRAM	60 MHz - w/serial config enable/disable
		8, 10, 11, 12, 14, 15, 7	PCICLKs	30 MHz - w/serial config enable/disable
1	0	28	PCI_STOP#	Power Management, PCI (0:5) Clocks Stopped when low
		29	CPU_STOP#	Power Management, CPU (0:3) Clocks Stopped when low
		31	SDRAM/PWR _DWN#	Used as PWR_DWN# when low
		7	PCICLK_F	33.3 MHz - 33.3 MHz - PCI Clock Free running for Power Management
		44, 43, 41, 40	CPUCLKs	66.6 MHz - CPU Clocks w/external Stop Control and serial config individual enable/disable.
		38, 37, 35, 34, 32, 21, 20, 18, 17	SDRAM	66.6 MHz - SDRAM Clocks w/serial config individual enable/disable.
		8, 10, 11, 12, 14, 15	PCICLKs	33.3 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable.
0	0	28	PCI_STOP#	Power Management, PCI (0:5) Clocks Stopped when low
		29	CPU_STOP#	Power Management, CPU (0:3) Clocks Stopped when low
		31	PWR_DWN#	Used as PWR_DWN#
		7	PCICLK_F	30 MHz - PCI Clock Free running for Power Management
		44, 43, 41, 40	CPUCLKs	60 MHz - CPU Clocks w/external Stop control and serial config individual enable/disable.
		38, 37, 35, 34, 32, 21, 20, 18, 17	SDRAM	60 MHz - SDRAM Clocks w/serial config individual enable/disable.
		8, 10, 11, 12, 14, 15	PCICLKs	30 MHz - PCI Clocks w/external Stop control and serial config individual enable/disable.

Example:
a) if MODE = 1, pins 28, 29 and 31 are configured as SDRAM7, SDRAM6 and SDRAM5 respectively.
b) if MODE = 0, pins 28, 29 and 31 are configured as PCI_STOP#, CPU_STOP# and PWR_DWN# respectively.

Power-On Default Conditions

At power-up and before device programming, all clocks will default to an enabled and "on" condition. The frequencies that are the produced are on the FS and MODE pin as shown in the table below.

CLOCK	DEFAULT CONDITION AT POWER-UP
REF 0	14.31818 MHz
IOAPIC (0:1)	14.31818 MHz

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Technical Pin Function Descriptions

VDD(1,2,3,4)
This is the power supply to the internal core logic of the device as well as the clock output buffers for REF(0:1), PCICLK, 48/24MHzA/B and SDRAM(0:7).

This pin operates at 3.3V volts. Clocks from the listed buffers that it supplies will have a voltage swing from Ground to this level. For the actual guaranteed high and low voltage levels for the Clocks, please consult the DC parameter table in this data sheet.

VDDL1,2
This is the power supplies for the CPUCLK and IOAPCI output buffers. The voltage level for these outputs may be 2.5 or 3.3 volts. Clocks from the buffers that each supplies will have a voltage swing from Ground to this level. For the actual Guaranteed high and low voltage levels of these Clocks, please consult the DC parameter table in this Data Sheet.

GND
This is the power supply ground (common or negative) return pin for the internal core logic and all the output buffers.

X1
This input pin serves one of two functions. When the device is used with a Crystal, X1 acts as the input pin for the reference signal that comes from the discrete crystal. When the device is driven by an external clock signal, X1 is the device input pin for that reference clock. This pin also implements an internal Crystal loading capacitor that is connected to ground. See the data tables for the value of this capacitor.

X2
This Output pin is used only when the device uses a Crystal as the reference frequency source. In this mode of operation, X2 is an output signal that drives (or excites) the discrete Crystal. The X2 pin will also implement an internal Crystal loading capacitor that is connected to ground. See the Data Sheet for the value of this capacitor.

CPUCLK(0:3)
These Output pins are the Clock Outputs that drive processor and other CPU related circuitry that requires clocks which are in tight skew tolerance with the CPU clock. The voltage swing of these Clocks are controlled by the Voltage level applied to the VDDL2 pin of the device. See the Functionality Table for a list of the specific frequencies that are available for these Clocks and the selection codes to produce them.

SDRAM(0:11)
These Output Clocks are use to drive Dynamic RAM's and are low skew copies of the CPU Clocks. The voltage swing of the SDRAM's output is controlled by the supply voltage that is applied to VDD3 of the device, operates at 3.3 volts.

IOAPIC
This Output is a fixed frequency Output Clock that runs at the Reference Input (typically 14.31818MHz). Its voltage level swing is controlled by VDDL1 and may operate at 2.5 or 3.3 volts.

REF0
The REF Output is a fixed frequency Clock that runs at the same frequency as the Input Reference Clock X1 or the Crystal (typically 14.31818MHz) attached across X1 and X2.

PCICLK_F
This Output is equal to PCICLK(0:5) and is FREE RUNNING, and will not be stopped by PCI_STP#.

PCICLK(0:5)
These Output Clocks generate all the PCI timing requirements for a Pentium/Pro based system. They conform to the current PCI specification. They run at 1/2 CPU frequency.

FS0
This Input pin controls the frequency of the Clocks at the CPU, PCICLK and SDRAM output pins. If a logic "1" value is present on this pin, the 66.6 MHz Clock will be selected. If a logic "0" is used, the 60MHz frequency will be selected.

MODE
This Input pin is used to select the Input function of the I/O pins. An active Low will place the I/O pins in the Input mode and enable those stop clock functions.

PWR_DWN#
This is an asynchronous active Low Input pin used to Power Down the device into a Low Power state by not removing the power supply. The internal Clocks are disabled and the VCO and Crystal are stopped. Powered Down will also place all the Outputs in a low state at the end of their current cycle. The latency of Power Down will not be greater than 3ms. The I^2C inputs will be Tri-Stated and the device will retain all programming information. This input pin only valid when MODE=0 (Power Management Mode)

CPU_STOP#
This is a synchronous active Low Input pin used to stop the CPUCLK clocks in an active low state. All other Clocks including SDRAM clocks will continue to run while this function is enabled. The CPUCLK's will have a turn ON latency of at least 3 CPU clocks. This input pin only valid when MODE=0 (Power Management Mode)

PCI_STOP#
This is a synchronous active Low Input pin used to stop the PCICLK clocks in an active low state. It will not effect PCICLK_F nor any other outputs. This input pin only valid when MODE=0 (Power Management Mode)

I^2C
The SDATA and SCLOCK Inputs are use to program the device. The clock generator is a slave-receiver device in the I^2C protocol. It will allow read-back of the registers. See configuration map for register functions. The I^2C specification in Philips I^2C Peripherals Data Handbook (1996) should be followed.

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General I^2C serial interface information

A. For the clock generator to be addressed by an I^2C controller, the following address must be sent as a start sequence.

Clock Generator Address (7 bits)							
A6	A5	A4	A3	A2	A1	A0	R/W#
1	1	0	1	0	0	1	0

B. The clock generator is a slave/receiver I^2C component. It can read back the data stored in the latches for verification. (set R/W# to 1 above)

C. The data transfer rate supported by this clock generator is 100K bits/sec (standard mode)

D. The input is operating at 3.3V logic levels.

E. The data byte format is 8 bit bytes.

F. To simplify the clock generator I^2C interface, the protocal is set to use only block writes from the controller. The bytes must be accessed in sequential order from lowest to highest byte with the ability to stop after any complete byte has been transferred. The clock generator can be issued a Byte count after the address and a command code of 0000 0000 to indicate that N Bytes of data will be sent. Then, N may be 1, 2 to 7, to load (Byte 0) only, (Byte 0 and 1) to (Byte 0, 1, 2, 3, 4, 5, 6).

G. In the power down mode (PWR_DWN# Low), the SDATA and SCLK pins are tristated and the internal data latches maintain all prior programming information.

H. At power-on, all registers are set to a default condition. See Byte 0 detail for default condition, Bytes 1 through 5 default to a 1 (Enabled output state).

Serial Configuration Command Bitmaps

Byte 0: Functional and Frequency Select Clock Register (Default=0)

BIT	PIN#	DESCRIPTION
Bit 7	-	Reserved
Bit 6	-	Must be 0 for normal operation
Bit 5	-	Must be 0 for normal operation
		In Spread Spectrum, Controls type (0=centered, 1=down spread)
Bit 4	-	Must be 0 for normal operation
		In Spread Spectrum, Controls Spreading (0=1.8%, 1=0.6%)
Bit 3	-	Reserved
Bit 2	-	Reserved
Bit 1 Bit 0	-	Bit1 Bit0 1 1 - Tri-State 1 0 - Spread Spectrum Enable 0 1 - Testmode 0 0 - Normal operation

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Select Functions

FUNCTION DESCRIPTION	OUTPUTS				
	CPU	PCI, PCI_F	SDRAM	REF	IOAPIC
Tri - State	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Test Mode	TCLK/2[1]	TCLK/4[1]	TCLK/2[1]	TCLK[1]	TCLK[1]

Notes:
1. REF is a test clock on the X1 inputs during test mode.

Byte 1: CPU Clock Register

BIT	PIN#	DESCRIPTION
Bit 7	-	Reserved
Bit 6	-	Reserved
Bit 5	-	Reserved
Bit 4	-	Reserved
Bit 3	40	CPUCLK3 (Active/Inactive)
Bit 2	41	CPUCLK2 (Active/Inactive)
Bit 1	43	CPUCLK1 (Active/Inactive)
Bit 0	44	CPUCLK0 (Active/Inactive)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 2: PCICLK Clock Register

BIT	PIN#	DESCRIPTION
Bit 7	-	Reserved
Bit 6	7	PCICLK_F (Active/Inactive)
Bit 5	15	PCICLK5 (Active/Inactive)
Bit 4	13	PCICLK4 (Active/Inactive)
Bit 3	12	PCICLK3 (Active/Inactive)
Bit 2	11	PCICLK2 (Active/Inactive)
Bit 1	10	PCICLK1 (Active/Inactive)
Bit 0	8	PCICLK0 (Active/Inactive)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 3: SDRAM Clock Register

BIT	PIN#	DESCRIPTION
Bit 7	28	SDRAM7 (Active/Inactive) Desktop only
Bit 6	29	SDRAM6 (Active/Inactive) Desktop only
Bit 5	31	SDRAM5 (Active/Inactive) Desktop only
Bit 4	32	SDRAM4 (Active/Inactive)
Bit 3	34	SDRAM3 (Active/Inactive)
Bit 2	35	SDRAM2 (Active/Inactive)
Bit 1	37	SDRAM1 (Active/Inactive)
Bit 0	38	SDRAM0 (Active/Inactive)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Byte 4: SDRAM Clock Register

BIT	PIN#	DESCRIPTION
Bit 7	-	Reserved
Bit 6	-	Reserved
Bit 5	-	Reserved
Bit 4	-	Reserved
Bit 3	17	SDRAM11 (Active/Inactive)
Bit 2	18	SDRAM10 (Active/Inactive)
Bit 1	20	SDRAM9 (Active/Inactive)
Bit 0	21	SDRAM8 (Active/Inactive)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

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Byte 5: Peripheral Clock Register

BIT	PIN#	DESCRIPTION
Bit 7	-	Reserved
Bit 6	-	Reserved
Bit 5	46	IOAPIC1 (Active/Inactive)
Bit 4	47	IOAPIC0 (Active/Inactive)
Bit 3	-	Reserved
Bit 2	-	Reserved
Bit 1	-	Reserved
Bit 0	2	REF0 (Active/Inactive)

Notes: 1 = Enabled; 0 = Disabled, outputs held low

Power Management

Clock Enable Configuration

CPU_STOP#	PCI_STOP#	PWR_DWN#	CPUCLK	PCICLK	Other Clocks, SDRAM, REF, IOAPICs	Crystal	VCOs
X	X	0	Low	Low	Stopped	Off	Off
0	0	1	Low	Low	Running	Running	Running
0	1	1	Low	33.3/30 MHz	Running	Running	Running
1	0	1	66.6/60 MHz	Low	Running	Running	Running
1	1	1	66.6/60 MHz	33.3/30 MHz	Running	Running	Running

Full clock cycle timing is guaranteed at all times after the system has initially powered up except where noted. The first clock pulse coming out of a stopped clock condition may be slightly distorted due to clock network charging circuitry. Board routing and signal loading may have a large impact on the initial clock distortion also.

ICS9148-01 Power Management Requirements

SIGNAL	SIGNAL STATE	Latency No. of rising edges of free running PCICLK
CPU_ STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PCI_STOP#	0 (Disabled)[2]	1
	1 (Enabled)[1]	1
PWR_DWN#	1 (Normal Operation)[3]	3mS
	0 (Power Down)[4]	2max

Notes.
1. Clock on latency is defined from when the clock enable goes active to when the first valid clock comes out of the device.
2. Clock off latency is defined from when the clock enable goes inactive to when the last clock is driven low out of the device.
3. Power up latency is when PD# goes inactive (high) to when the first valid clocks are output by the device.
4. Power down has controlled clock counts applicable to CPUCLK, SDRAM, PCICLK only.
   The REF and IOAPIC will be stopped independant of these.

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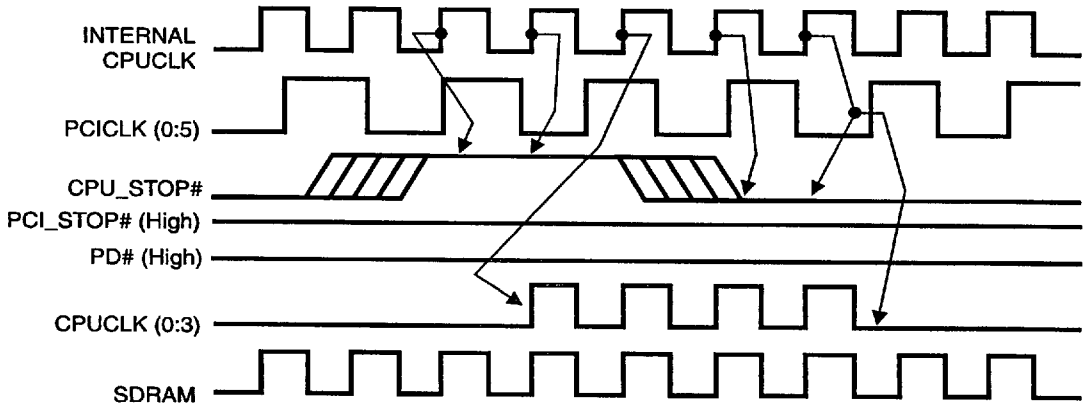
CPU_STOP#Timing Diagram

CPUSTOP# is an asychronous input to the clock synthesizer. It is used to turn off the CPUCLKs for low power operation. CPU_STOP# is synchronized by the **ICS9148-01**. The minimum that the CPUCLK is enabled (CPU_STOP# high pulse) is 100 CPUCLKs. All other clocks will continue to run while the CPUCLKs are disabled. The CPUCLKs will always be stopped in a low state and start in such a manner that guarantees the high pulse width is a full pulse. CPUCLK on latency is less than 4 CPUCLKs and CPUCLK off latency is less than 4 CPUCLKs.



Notes:

1. All timing is referenced to the internal CPUCLK.
2. CPU_STOP# is an asynchronous input and metastable conditions may exist. This signal is synchronized to the CPUCLKs inside the **ICS9148-01.**
3. All other clocks continue to run undisturbed.
4. PD# and PCI_STOP# are shown in a high (true) state.

PCI_STOP# Timing Diagram

PCI_STOP# is an asynchronous input to the **ICS9148-01**. It is used to turn off the PCICLK (0:5) clocks for low power operation. PCI_STOP# is synchronized by the **ICS9148-01** internally. The minimum that the PCICLK (0:5) clocks are enabled (PCI_STOP# high pulse) is at least 10 PCICLK (0:5) clocks. PCICLK (0:5) clocks are stopped in a low state and started with a full high pulse width guaranteed. PCICLK (0:5) clock on latency cycles are only one rising PCICLK clock off latency is one PCICLK clock.

(Drawing shown on next page.)

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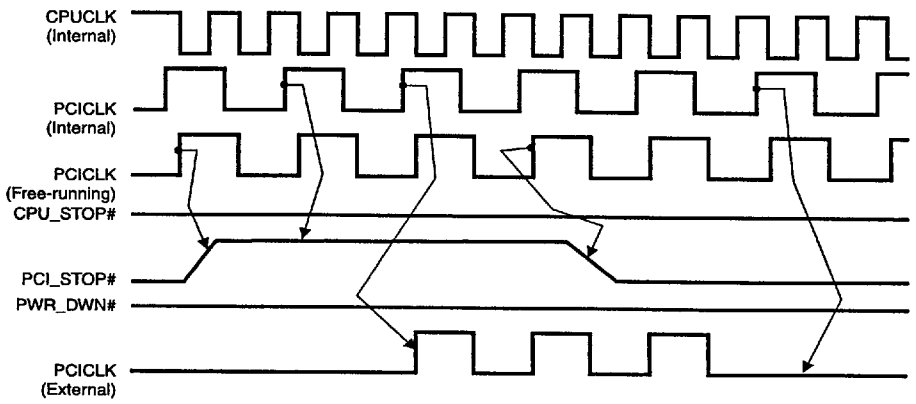
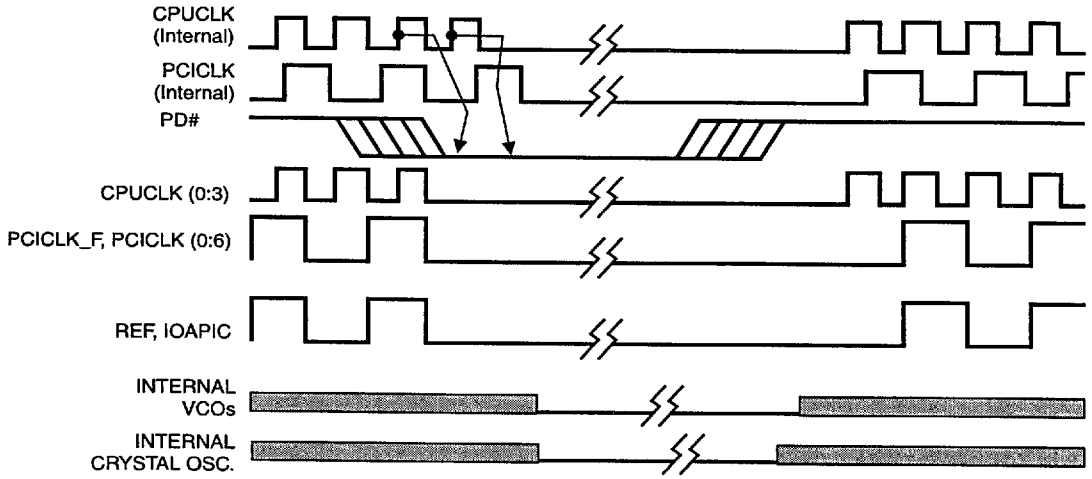


Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device.)
2. PCI_STOP# is an asynchronous input, and metastable conditions may exist. This signal is required to be synchronized inside the ICS9148.
3. All other clocks continue to run undisturbed.
4. PD# and CPU_STOP# are shown in a high (true) state.

PD# Timing Diagram

The power down selection is used to put the part into a very low power state without turning off the power to the part. PD# is an asynchronous active low input. This signal is synchronized internal by the **ICS9148-01** prior to its control action of powering down the clock synthesizer. Internal clocks will not be running after the device is put in power down state. When PD# is active (low) all clocks are driven to a low state and held prior to turning off the VCOs and the Crystal oscillator. The power on latency is guaranteed to be less than 3mS. The power down latency is less than three CPUCLK cycles. PCI_STOP# and CPU_STOP# are don't care signals during the power down operations.



Notes:
1. All timing is referenced to the Internal CPUCLK (defined as inside the ICS9148 device).
2. PD# is an asynchronous input and metastable conditions may exist. This signal is synchronized inside the ICS9148.
3. The shaded sections on the VCO and the Crystal signals indicate an active clock is being generated.

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Absolute Maximum Ratings

Supply Voltage ..... 7.0 V

Logic Inputs ..... GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature ..... 0°C to +70°C

Storage Temperature ..... –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70° C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCT CHARACTERIZATION

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

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Electrical Characteristics at 3.3V

V_{DD} = 3.0 – 3.7 V, T_A = 0 – 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

TARGET SPECIFICATION SUBJECT TO CHANGE WITH FULL PRODUCTION CHARACTERIZATION

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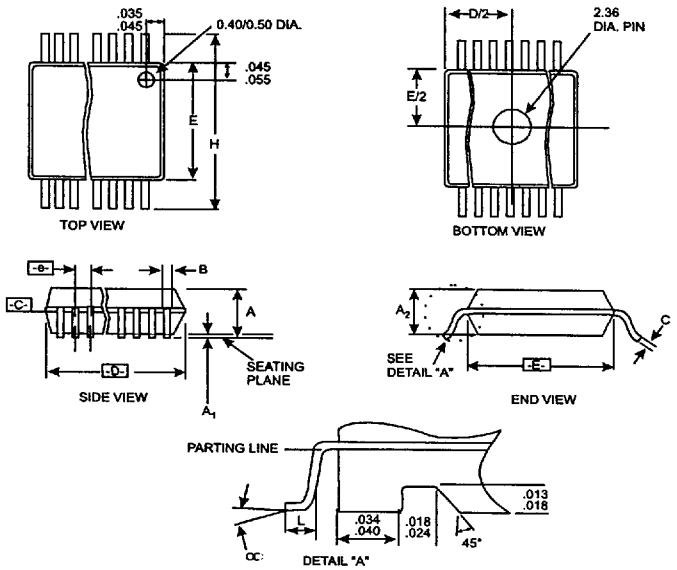

SSOP Package

SYMBOL	COMMON DIMENSIONS			VARIATIONS	D			N
	MIN.	NOM.	MAX.		MIN.	NOM.	MAX.	
A	.095	.101	.110	AC	.620	.625	.630	48
A1	.008	.012	.016					
A2	.088	.090	.092					
B	.008	.010	.0135					
C	.005	-	.010					
D	See Variations							
E	.292	.296	.299					
e	0.025 BSC							
H	.400	.406	.410					
h	.010	.013	.016					
L	.024	.032	.040					
N	See Variations							
∝	0°	5°	8°					
X	.085	.093	.100					

Ordering Information

ICS9148F-01

Example:

ICS XXXX F - PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  F=SSOP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV = Standard Device

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