Integrated Circuit Systems, Inc.

ICS9158

Integrated Buffer and Motherboard Frequency Generator

General Description

The **ICS9158** is a low cost frequency generator designed specifically for desktop and notebook PC applications. Eight high drive, skew-controlled copies of the CPU clock are available, eliminating the need for an external buffer.

Each high drive (50mA) output is capable of driving a 30pF load and has a typical duty cycle of 50/50. The CPU clock outputs are skew-controlled to within ±250ps. The CPU clocks provide all necessary frequencies for 286, 386, 486 and Pentium systems, including support for the latest speeds of processors.

The CPU clock offers the unique feature of smooth, glitch-free transitions from one frequency to the next, making this the ideal device to use whenever slowing the CPU speeds. The **ICS9158** makes a gradual transition between frequencies so that it meets the Intel cycle-to-cycle timing specification for 486 systems.

ICS has been shipping Motherboard Frequency Generators since April 1990, and is the leader in the area of multiple output clocks on a single chip. The **ICS9158** is a third generation device, and uses ICS's patented analog CMOS Phase-Locked Loop technology for low phase jitter. ICS offers a broad family of frequency generators for motherboards, graphics and other applications, including cost effective versions with only one or two output clocks. Consult ICS for all of your clock generation needs.

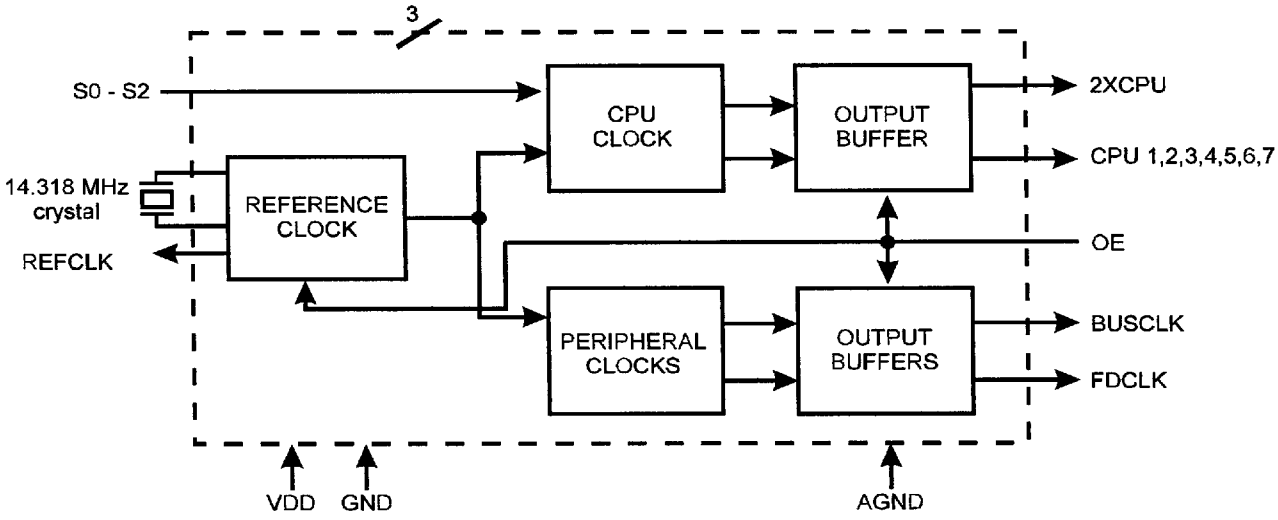
Features

- Eight skew-free, high drive CPU clock outputs
- Up to 100 MHz output at 5V
- ±250ps skew between CPU and 2XCPU outputs
- Outputs can drive up to 30pF load
- 50mA output drivers
- Typical 50/50 duty cycle
- Compatible with 486 and Pentium CPUs
- Glitch-free start and stop clock option
- Optional power-down mode supports Energy Star ("green") PCs
- On-chip loop filter components
- Low power, high speed 0.8µ CMOS technology
- 24-pin PDIP or SOIC package

Clock Table (in MHz)

Clock	ICS9158
BUSCLK	16
FDCLK	24
REFCLK	14.318
CPUCLK	4,8,30,20,25,33.3,40, or 50
2XCPUCLK	8,16,60,40,50,66.6,80, or 100

Block Diagram



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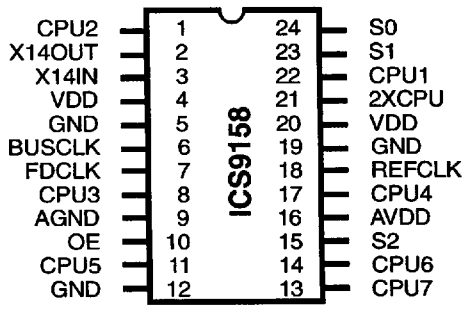
Pin Configuration



24-Pin PDIP or SOIC

Pin Descriptions for ICS9158

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
1	CPU2	Output	CPU clock output.
2	X14OUT	-	Crystal connection.
3	X14IN	-	Crystal connection.
4	VDD	-	Digital POWER SUPPLY (+5V).
5	GND	-	Digital GROUND.
6	BUSCLK	Output	16 MHz clock output.
7	FDCLK	Output	24 MHz floppy disk/combination I/O clock output.
8	CPU3	Output	CPU clock output.
9	AGND	-	ANALOG GROUND.
10	OE	Input	OUTPUT ENABLE. Tristates all outputs when low.*
11	CPU5	Output	CPU clock output.
12	GND	-	Digital GROUND.
13	CPU7	Output	CPU clock output.
14	CPU6	Output	CPU clock output.
15	S2	Input	CPU clock frequency select 2.*
16	AVDD	-	ANALOG power supply (+5V).
17	CPU4	Output	CPU clock output.
18	REFCLK	Output	14.318 MHz clock output.
19	GND	-	Digital GROUND.
20	VDD	-	Digital POWER SUPPLY (+5V).
21	2XCPU	Output	2X CPU clock output.
22	CPU1	Output	CPU clock output.
23	S1	Input	CPU clock frequency select #1.*
24	S0	Input	CPU clock frequency select #0.*

* Input has internal pull-up to VDD.

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Absolute Maximum Ratings

AVDD, VDD referenced to GND 7V
Operating temperature under bias..... 0°C to +70°C
Storage temperature ..... -40°C to +150°C
Voltage on I/O pins referenced to GND..... GND -0.5V to VDD +0.5V
Power dissipation ..... 0.5 Watts

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics at 5V

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}				0.8	V
Input High Voltage	V_{IH}		2.0			V
Input Low Current	I_{IL}	V_{IN}=0V	-5		5	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5		5	µA
Output Low Voltage	V_{OL}	I_{OL}=20.0mA		0.25	0.4	V
Output High Voltage (Note 1)	V_{OH}	I_{OH}=-30mA	2.4	3.5		V
Output Low Current (Note 1)	I_{OL}	V_{OL}=0.8V	45	65		mA
Output High Current (Note 1)	I_{OH}	V_{OH}=2.0V		-55	-35	mA
Supply Current	I_{DD}	No load, 80 MHz		43	65	mA
Output Frequency Change over Supply and Temperature (Note 1)	F_D	With respect to typical frequency		0.002	0.01	%
Short Circuit Current (Note 1)	I_{SC}	Each output clock	25	56		mA
Pull-up Resistor Value (Note 1)	R_{PU}	Input pin		680		kΩ
Input Capacitance (Note 1)	C_i	Except X1, X2			8	pf
Load Capacitance (Note 1)	C_L	Pins X1, X2		20		pf

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

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Electrical Characteristics *(continued)*

V_{DD} = +5V±10%, T_A=0°C to 70°C unless otherwise stated

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Output Rise time, 0.8 to 2.0V (Note 1)	t_r	30pF load	-	1	2	ns
Rise time, 20% to 80% V_{DD} (Note 1)	t_r	30pF load	-	2.5	3	ns
Output Fall time, 2.0 to 0.8V (Note 1)	t_f	30pF load	-	0.5	1	ns
Fall time, 80% to 20% V_{DD} (Note 1)	t_f	30pF load	-	1.5	2	ns
Duty cycle (Note 1)	d_t	30pF load	40/60	48/52	60/40	%
Jitter, one sigma (Note 1)	t_{j1s}	As compared with clock period		0.5	2.0	%
Jitter, absolute (Note 1)	t_{jab}		-5	2	5	%
Jitter, absolute (Note 1)	t_{jab}	16-100 MHz clocks	-500		500	ps
Input Frequency	f_i			14.318		MHz
Clock skew window between CPU and 2XCPU outputs (Note 1)	T_{sk}			100	250	ps
Frequency Transition time (Note 1)	t_{ft}	From 4 to 50 MHz		13	20	ms

Note 1: Parameter is guaranteed by design and characterization. Not 100% tested in production.

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ICS9158 CPU Clock Decoding Table

(using 14.318 MHz input. All frequencies in MHz)

CLOCK#2 CPU and 2XCPU

S2 (Pin 15)	S1 (Pin 23)	S0 (Pin 24)	2XCPU (Pin 21)	CPU
0	0	0	7.580	3.790
0	0	1	15.511	7.756
0	1	0	59.875	29.938
0	1	1	40.090	20.045
1	0	0	50.113	25.057
1	0	1	66.476	33.238
1	1	0	79.772*	39.886*
1	1	1	100.226*	50.113*

*5V only

Peripheral Clocks

BUSCLK (Pin 6)	FDCLK (Pin 7)
16.002	24.003

Reference Clock

REFCLK (Pin 18)
14.318

Frequency Transitions

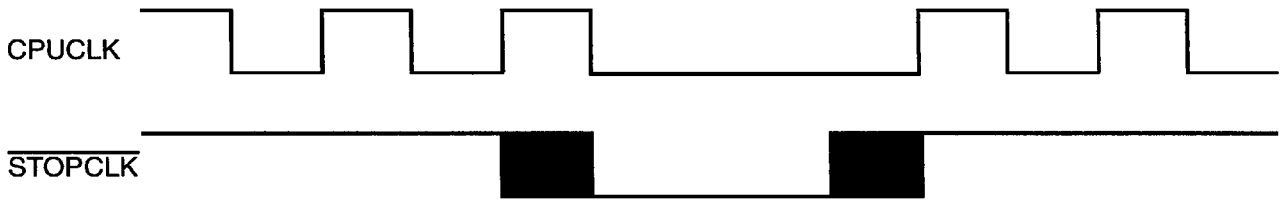
A key feature of the **ICS9158** is its ability to provide smooth, glitch-free frequency transitions on the CPU and 2XCPU clocks when the frequency select pins are changed. The frequency transition rate does not violate the Intel 486 or Pentium specification of less than 0.1% frequency change per clock period.

Using an Input Clock as a Reference

The **ICS9158** is designed to accept a 14.318 MHz crystal as the input reference. With some external changes, it is possible to use a crystal oscillator or other clock sources. Please see application note AAN04 for details on driving the **ICS9158** with a clock.

Stop Clock Feature (Optional Mask Version)

The **ICS9158** incorporates a unique stop clock feature compatible with static logic processors. When the stop clock pin goes low, the CPUCLK will go low after the next occurring falling edge. When STOPCLK again goes high, CPUCLK resumes on the next rising edge of the internal clock. This feature enables fast, glitch-free starts and stops of the CPUCLK and is useful in Energy Start motherboard applications. Please contact ICS marketing for more details.



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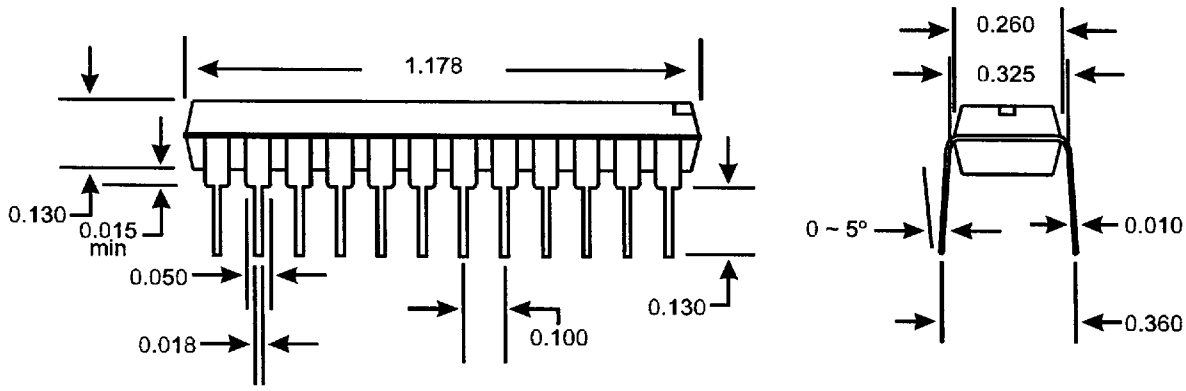

24-DIP Package

Ordering Information

ICS9158N-01

Example:

ICS XXXX M -PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  N=DIP
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device; GSP=Genlock Device

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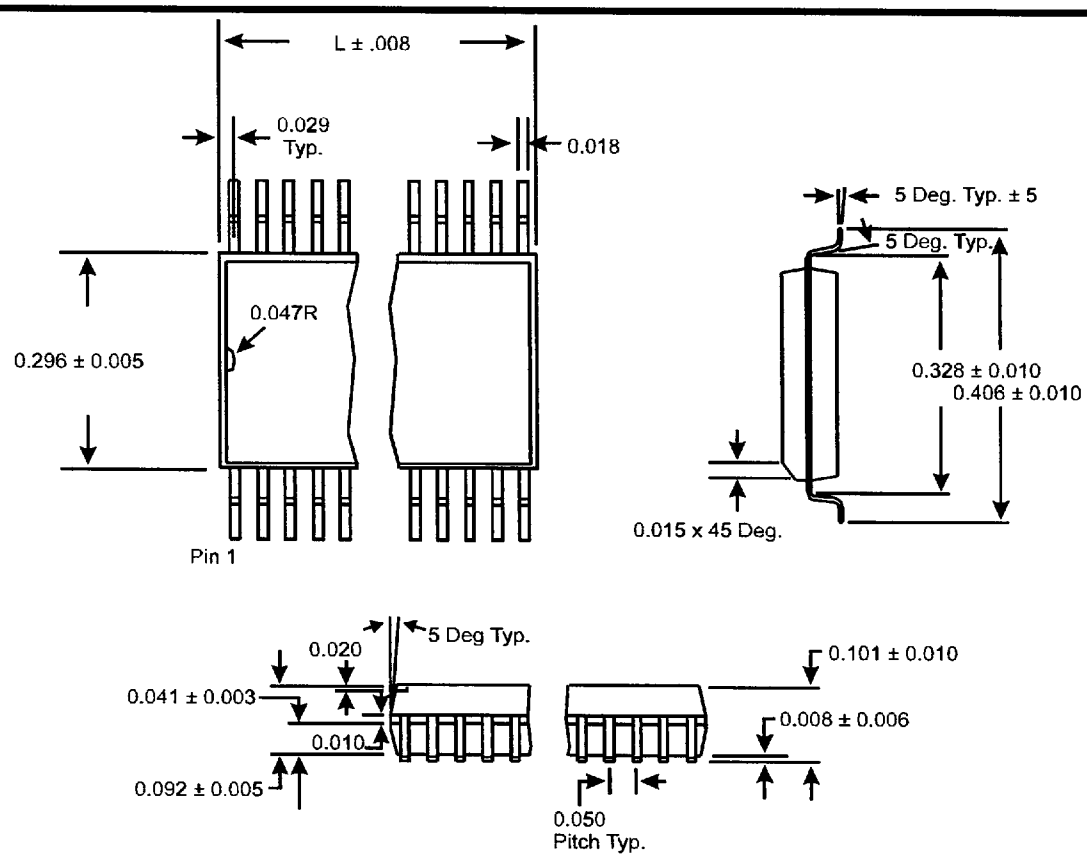

LEAD COUNT	24L
DIMENSION L	0.604

24 Lead SOIC

Ordering Information

ICS9158M-01

Example:

ICS XXXX M -PPP

- **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **Package Type**
  M=SOIC
- **Device Type (consists of 3 or 4 digit numbers)**
- **Prefix**
  ICS, AV=Standard Device; GSP=Genlock Device

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