Frequency Generator and Integrated Buffer for PENTIUM™

General Description

The **ICS9159-02** generates all clocks required for high speed RISC or CISC microprocessor systems such as 486, Pentium, PowerPC,™ etc. Four different reference frequency multiplying factors are externally selectable with smooth frequency transitions. These multiplying factors can be customized for specific applications. A test mode is provided to drive all clocks directly.

High drive BCLK outputs provide greater than 1V/ns slew rate into 30pf loads. PCLK outputs provide better than 1V/ns slew rate into 20pf loads while maintaining ±5% duty cycle.

Features

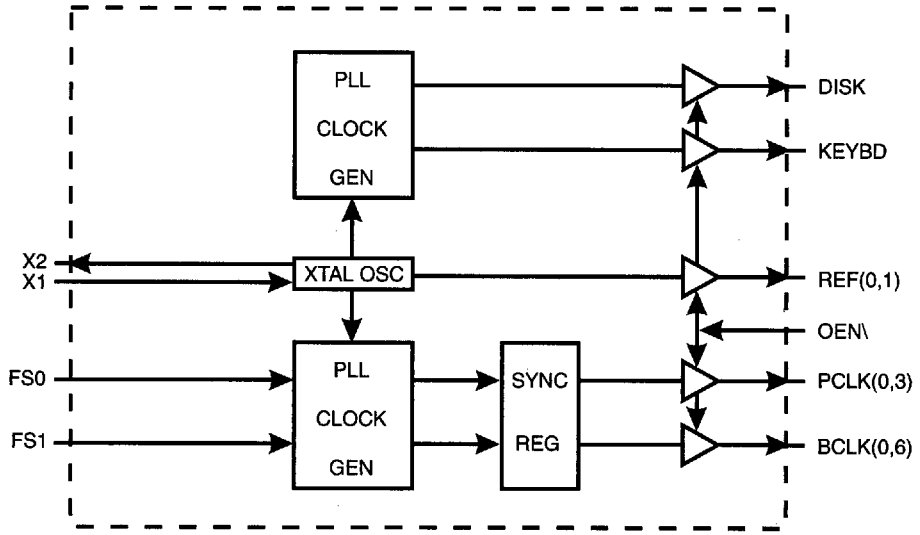
- Generates up to four processor and six bus clocks, plus disk, keyboard and reference clocks
- Synchronous clocks skew matched to ±250ps
- Output frequency ranges to 100 MHz
- Test clock mode eases system design
- Selectable multiplying and processor/bus ratios
- Stop clock control stops clocks glitch-free
- Custom configurations available
- 3.0V - 5.5V supply range
- 28-pin SOIC package

C

Applications

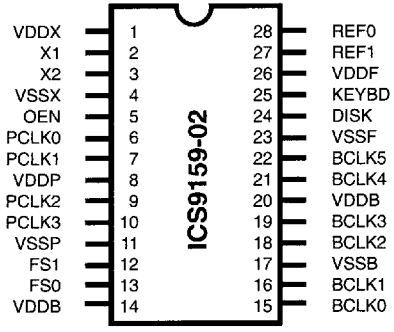
- Ideal for high-speed RISC or CISC systems such as 486, Pentium, PowerPC, etc.

Block Diagram



Pentium is a trademark of Intel Corporation.
PowerPC is a trademark of Motorola Corporation.

Pin Configuration



28-Pin SOIC
K-7

ICS9159-02 Functionality

FS1	FS0	*VCO	X1, REF (MHz)	PCLK(0,3) (MHz)
0	0	230/33x X1	14.31818	50
0	1	176/21x X1	14.31818	60
1	0	212/23x X1	14.31818	66
1	1	Test mode	TCLK	TCLK/2

*VCO range is limited from 60 - 200 MHz.

PCLK(0,3)	BCLK(0,5)	DISK	KEYBD
VCO/2	PCLK/2	24 MHz	12 MHz
TCLK/2	TCLK/4	TCLK/4	TCLK/8

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	DESCRIPTION
2	X1	IN	XTAL or external reference frequency input. This input includes XTAL load capacitance and feedback bias for a 10 - 30 MHz XTAL.
3	X2	OUT	XTAL output which includes XTAL load capacitance.
1 4	VDDX VSSX	PWR	XTAL oscillator circuit power supplies.
6, 7, 9, 10	PCLK(0,3)	OUT	Processor clock outputs which are a multiple of the input reference frequency as shown in the table below. Duty cycle is 50/50±5% with a maximum frequency of 100 MHz. Custom multiplying configurations are available.
8 11	VDDP VSSP	PWR	PCLK power supplies. VSSP and VDDP power PCLK(0,3) outputs and the internal PCLK PLL.
13, 12	FS(0,1)	IN	Frequency multiplier select pins. See table below. These inputs have internal pull-up devices.
15, 16, 18 19, 21, 22	BCLK(0,5)	OUT	Bus clock outputs are fixed at ½ the PCLK frequency. In all cases, the duty cycle is 50/50±5%.
17 14, 20	VSSB VDDB	PWR	BCLK power supplies. VSSB and VDDB power BCLK(0,5) outputs. Output levels can be customized by connecting VDDB to voltages less than VDDF.
5	OEN	IN	OEN tristates all outputs when low. This input has an internal pull-up device.
24	DISK	OUT	The DISK controller clock is fixed at 12 MHz.
25	KEYBD	OUT	The KEYBD clock is fixed at 12 MHz.
23 26	VSSF VDDF	PWR	Fixed clock (DISK and KEYBD) output and PLL power supplies.
28, 27	REF(0,1)	OUT	REF is a buffered copy of the crystal oscillator or reference input clock, nominally 14.31818 MHz.

Timing Specifications

3.3V ±5% or 5.0V ±5% VDD, 0-70°C, measured at 1.5V, Cload=20pf

PIN	JITTER cycle-cycle	SKEW to PCLK	SKEW to BCLK	SLEW, LOAD	DUTY CYCLE
PCLK(0,3)	<±200ps	<±250ps	<±750ps	>1.0V/ns, 20pf	<±5%
BCLK(0,5)	<±300ps	<±750ps	<±500ps	>1.0V/ns, 30pf	<±5%

Absolute Maximum Ratings

Supply voltage ..... 7.0 V
Logic inputs ..... GND -0.5V to V_{DD} +0.5V
Ambient operating temp ..... 0 to +70°C
Storage temperature ..... -65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

C

Electrical Characteristics at 3V

V_{DD} =3.0 - 3.7V

DC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Input Low Voltage	V_{IL}		-	-	$0.2V_{DD}$	V
Input High Voltage	V_{IH}		$0.7V_{DD}$	-	-	V
Input Low Current	I_{IL}	V_{IN}=0V	-	10.5	28.0	µA
Input High Current	I_{IH}	V_{IN}=V_{DD}	-5.0	-	5.0	µA
Output Low Current	I_{OL}	V_{OL}=0.8V; for PCLKS & BCLKS	30.0	47.0	-	mA
Output High Current	I_{OH}	V_{OL}=2.0V; for PCLKS & BCLKS	-	-66.0	-42.0	mA
Output Low Current	I_{OL}	V_{OL}=0.8V; for fixed CLKs	25.0	38.0	-	mA
Output High Current	I_{OH}	VOL=2.0V; for fixed CLKs	-	-47.0	-30.0	mA
Output Low Voltage	V_{OL}	I_{OL}=15mA; for PCLKS & BCLKS	-	0.3	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-30mA; for PCLKS & BCLKS	2.4	2.8	-	V
Output Low Voltage	V_{OL}	I_{OL}=12.5mA; for fixed CLKs	-	0.3	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-20mA; for fixed CLKs	2.4	2.8	-	V
Supply Current	I_{CC}	@66.66 MHz; all outputs unloaded	-	55	110	mA

Electrical Characteristics at 3V

V_{DD} =3.0 - 3.7V

AC Characteristics						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Rise Time 0.8 to 2.0V	T_r	20pf load	-	1.5	3	ns
Fall Time 2.0 to 0.8V	T_f	20pf load	-	0.9	2	ns
Rise Time 20% to 80%	T_r	20pf load	-	2	4.5	ns
Fall Time 80% to 20%	T_f	20pf load	-	1.8	4.25	ns
Duty Cycle	D_t	20pf load	40	50	60	%
Jitter, One Sigma	T_{jis}	CPU & Bus Clocks; Load=20pf, FOUT>25 MHz	-	50	150	ps
Jitter, Absolute	T_{jab}	CPU & Bus Clocks; Load=20pf, FOUT>25 MHz	-250	-	250	ps
Jitter, One Sigma	T_{jis}	Fixed CLK; Load=20pf; Comp. to the period	-	1	3	%
Jitter, Absolute	T_{jab}	Fixed CLK; Load=20pf; Comp. to the period	-	2	5	%
Input Frequency	F_i		-	14.318	-	MHz
Clock Skew	T_{sk}	PCLK to PCLK; Load=20pf; @1.4V	-	50	250	ps
Clock Skew	T_{sk}	BCLK to BCLK; Load=20pf; @1.4V	-	90	500	ps
Clock Skew	T_{sk}	PCLK to BCLK; Load=20pf; @1.4V	1	2.6	5	ns

Ordering Information

ICS9159-02M

Example:

ICS XXXX-PPP M

- M — **Package Type**: W=SOIC, SOP
- PPP — **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- XXXX — **Device Type (consists of 3 or 4 digit numbers)**
- ICS — **Prefix**: ICS, AV=Standard Device; GSP=Genlock Device