SONY

ICX026BLA

1/2 inch CCD Image Sensor for EIA B/W Camera

Description

The ICX026BLA is an interline transfer CCD solid-state imager suitable for EIA 1/2 inch B/W video cameras High sensitiveness is achieved through the adoption of HAD (Hole Accumulation Diode) sensors.

This chip features a field integration read out system an electronic shutter with variable charge storage time and 20pin Cer-DIP package

Features

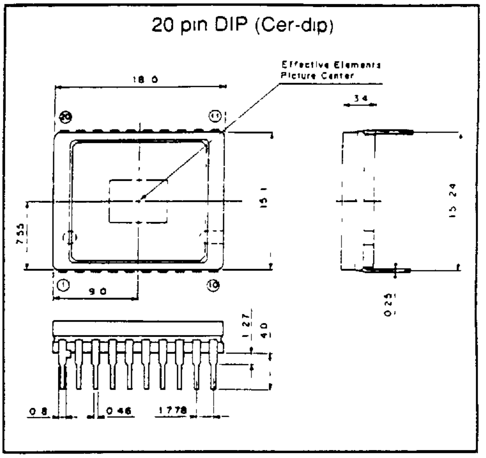
- High sensitivity (+6 dB compare with ICX026AL)
- Optical size 1/2 inch format
- Field integration read out system
- Low dark current
- Horizontal register 5V drive
- High antiblooming
- Low smear
- Variable speed electronic shutter

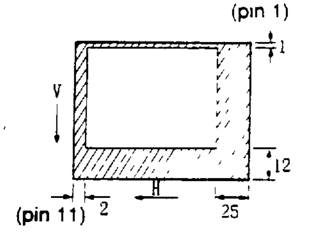
Device Structure

- Number of effective pixels 510 (H) × 492 (V)
- Number of total pixels 537 (H) × 505 (V)
- Interline transfer CCD image sensor
- Chip size 7 84 mm (H) × 6.40 mm (V)
- Unit cell size 12.7 μm (H) × 9 8 μm (V)
- Optical black
  - Horizontal (H) direction Front 2 pixels Rear 25 pixels
  - Vertical (V) direction Front 12 pixels Rear 1 pixels
- Number of dummy bits
  - Horizontal 16
  - Vertical 1 (even field only)
- Substrate material silicon

Package Outline

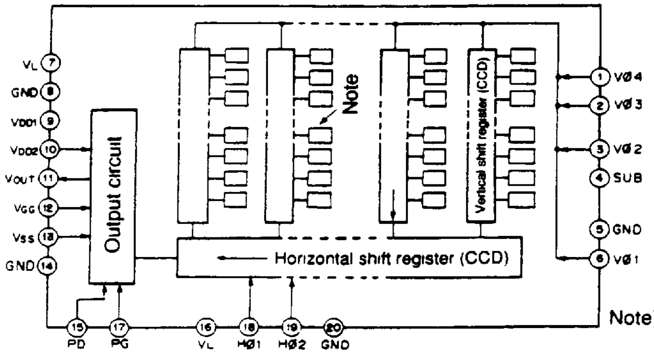
Unit mm





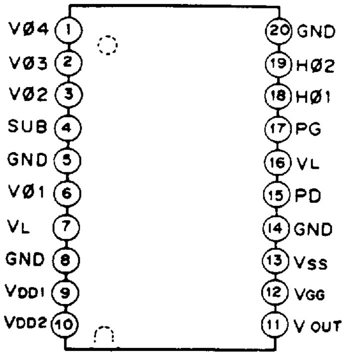
Optical black position (Top View)

Block Diagram



Note) □ : Photo sensor

Pin Configuration (Top View)



Pin Description

No	Symbol	Description	No.	Symbol	Description
1	$V\phi 4$	Vertical register transfer clock	11	V_{OUT}	Signal output
2	$V\phi 3$	Vertical register transfer clock	12	V_{GG}	Output amplifier gate bias
3	$V\phi 2$	Vertical register transfer clock	13	V_{SS}	Output amplifier source
4	SUB	Substrate (Overflow drain)	14	GND	GND
5	GND	GND	15	PD	Precharge drain bias
6	$V\phi 1$	Vertical register transfer clock	16	V_L	Protective transistor bias
7	V_L	Protective transistor bias	17	PG	Precharge gate clock
8	GND	GND	18	$H\phi 1$	Horizontal register transfer clock
9	V_{DD1}	Output amplifier drain supply	19	$H\phi 2$	Horizontal register transfer clock
10	V_{DD2}	Output amplifier drain supply	20	GND	GND

Absolute Maximum Ratings

• Substrate voltage	SUB – GND	–0.3 to +55 V
• Supply voltage	V_{DD1}, V_{DD2}, PD, V_{OUT}, V_{SS} – GND	–0.3 to +18 V
	V_{DD1}, V_{DD2}, PD, V_{OUT}, V_{SS} – SUB	–55 to +10 V
• Clock input voltage	$V\phi 1$, $V\phi 2$, $V\phi 3$, $V\phi 4$, $H\phi 1$, $H\phi 2$ – GND	–15 to +20 V
	$V\phi 1$, $V\phi 2$, $V\phi 3$, $V\phi 4$, $H\phi 1$, $H\phi 2$ – SUB	–65 to +10 V
• Voltage difference between vertical clock input pins		15 V*
• Voltage difference between horizontal clock input pins		17 V
• $H\phi 1$, $H\phi 2$ – $V\phi 4$		–17 to +17 V
• PG, V_{GG} – GND		–10 to +15 V
• PG, V_{GG} – SUB		–55 to +10 V
• V_L – SUB		–65 to +0.3 V
• Beside GND, SUB, V_L – V_L		–0.3 to +30 V
• Storage temperature		–30 to +80°C
• Operating temperature		–10 to +55°C

***Note)** +27 V (Max.) when clock width < 10 µs, duty factor < 0.1%

Bias Conditions

Item	Symbol	Min	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD1} V_{DD2}	14.55	15.0	15 45	V	$V_{DD1} = V_{DD2}$
Precharge drain voltage	V_{PD}	14.55	15 0	15.45	V	$V_{PD} = V_{DD1} = V_{DD2}$
Output amplifier gate voltage	V_{GG}	1.75	2 0	2.25	V	
Output amplifier source	V_{SS}	Ground through 680 Ω resistor ±5%				
Substrate voltage adjustment range	V_{SUB}	7		19	V	*1
Fluctuation range after substrate voltage adjustment	V_{SUB}	-3		+3	%	
Protective transistor bias	V_L	*2				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		2.5		mA	$I_{DD} = I_{DD1} + I_{DD2}$
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

Note) *1 Substrate voltage (V_{SUB}) setting value display.
Substrate voltage setting value is displayed at the back of the device through a code address. Adjust so as to obtain the displayed voltage at SUB pin.

V_{SUB} code address – two digits display □ □

Integral part Decimal part

The relation between code address of integral part and actual numerical values.

Code address of integral part	7	8	9	A	B	C	D	E	F	G	H	I	J
Numerical Value	7	8	9	10	11	12	13	14	15	16	17	18	19

<Example> F5 → 15.5 (V)

*2. V_L setting is V_{VL} of the vertical transfer clock waveform.

*3. 1) Current to earth when 18V is applied to pins V_{DD1}, V_{DD2}, V_{OUT}, V_{SS} and SUB pin However, pins that are not tested are grounded.
2) Current to earth when 20V is sequentially applied to pins $V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, $H\phi_1$ and $H\phi_2$. However, 20V is applied to SUB while pins that are not tested are grounded.
3) Current to earth when 15V is sequentially applied to pins PG and V_{GG}. However, 15V is applied to SUB while pins that are not tested are grounded.

*4 1) Current to earth when 55V is applied to SUB pin. Pins that are not tested are grounded.
2) Current to earth when V_L is grounded, GND and SUB are open and 30V is applied to other pins.

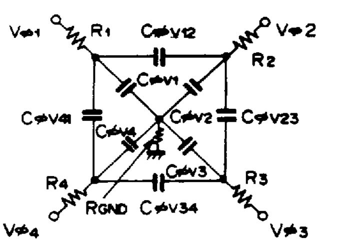
Clock Voltage Conditions

Item	Symbol	Min	Typ	Max	Unit	No	Remarks
Read out clock voltage	V_{VT}	14 3	15 0	15 7	V	2 6	*1
Vertical transfer clock voltage *2	V_{VH1} V_{VH2}, V_{VH3}, V_{VH4}	–0 2	0	0 2	V	1 2 3 6	$V_{VH}=(V_{VH1}+V_{VH2})$ 2
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9 6	–9 0	–8 3	V	1 2 3 6	$V_{VL}=(V_{VL3}+V_{VL4})$ 2
	$V_{\phi V}$	8 1	9 0	9 8	V	1 2 3 6	$V_{\phi V}=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$V_{VH1} - V_{VH2}$ |			0 2	V	3 6	
	$V_{VH3} - V_{VH}$	–0 4		0 1	V	2 3 6	
	$V_{VH4} - V_{VH}$	–0 4		0 1	V	1 3 6	
	V_{VHH}			0 8	V	1 2,3,6	High level coupling
	V_{VHL}			1 0	V	1 2 3.6	High level coupling
	V_{VLH}			0 8	V	1 2 3 6	Low level coupling
	V_{VLL}			0 8	V	1 2,3,6	Low level coupling
Horizontal transfer clock voltage	$V_{\phi H}$	4 7	5 0	5 3	V	18 19	*3
	V_{HL}	–0 05	0	0 05	V	18 19	
Precharge gate clock voltage	$V_{\phi PG}$	8 0		11 5	V	17	*4
	V_{PGL}	–0 1	0	0 1	V	17	
Substrate clock voltage	$V_{\phi SUB}$	23 0	32 0	34 0	V	4	*5

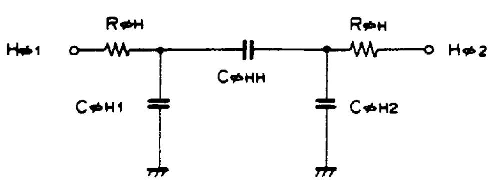
Note) *1. See Fig. 1
*2. See Fig. 2.
*3. See Fig 3.
*4. See Fig. 3.
*5. See Fig. 4.

Clock Equivalent Circuit Constant

Item	Symbol	Min	Typ	Max	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$, $C_{\phi V3}$		1000		pF	
Capacitance between vertical transfer clock and GND	$C_{\phi V2}$, $C_{\phi V4}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		1200		pF	
Capacitance between vertical transfer clocks	$C_{\phi V23}$, $C_{\phi V41}$		750		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		70		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		50		pF	
Capacitance between precharge gate clock and GND	$C_{\phi PG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		400		pF	
Vertical transfer clock serial resistor	R_1, R_2, R_3, R_4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		[illegible]5		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		[illegible]		Ω	



Vertical transfer clock equivalent circuit



Horizontal trasfer clock equivalent circuit

Drive Clock Waveform Conditions

1 Read out clock waveform

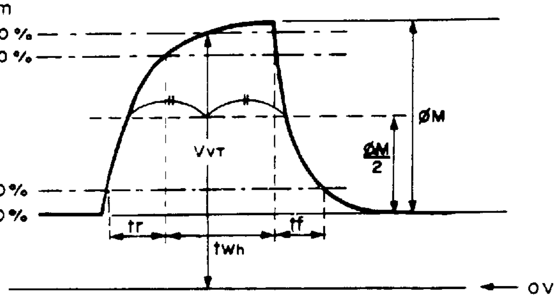


Fig.1

2 Vertical transfer clock waveform

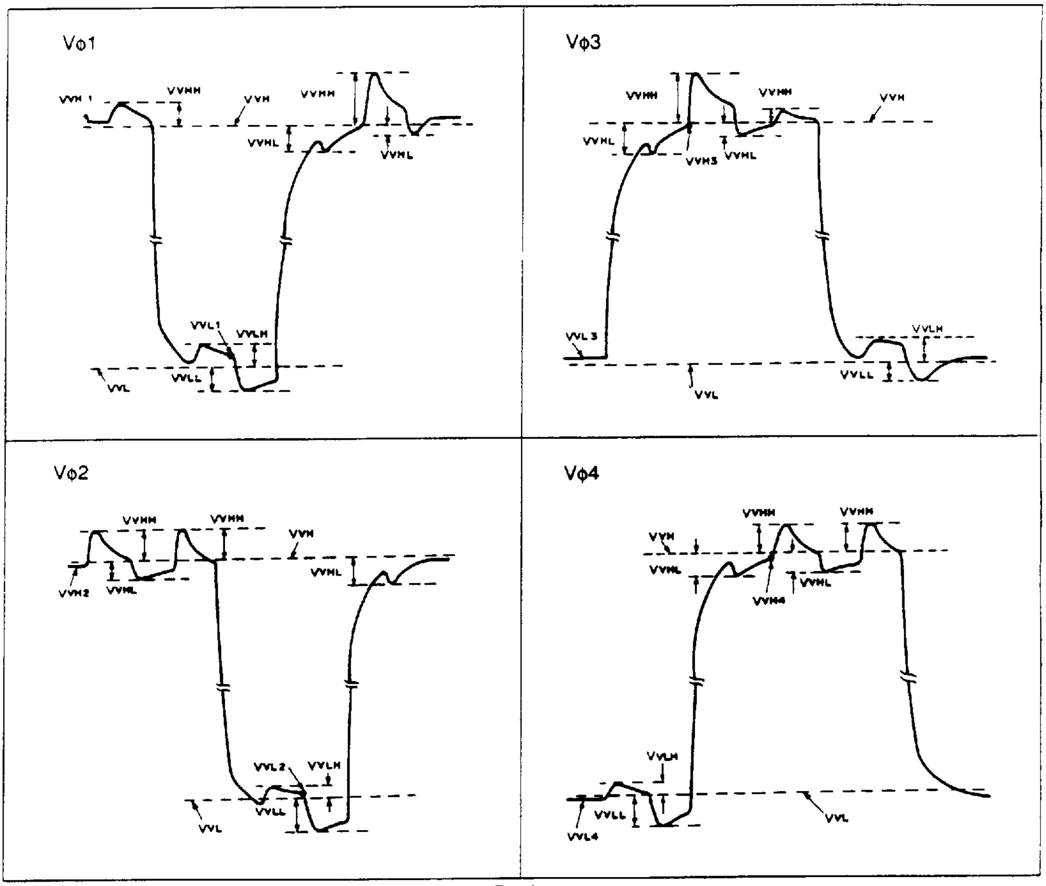


Fig.2

3 Horizontal transfer clock waveform/Precharge gate clock waveform

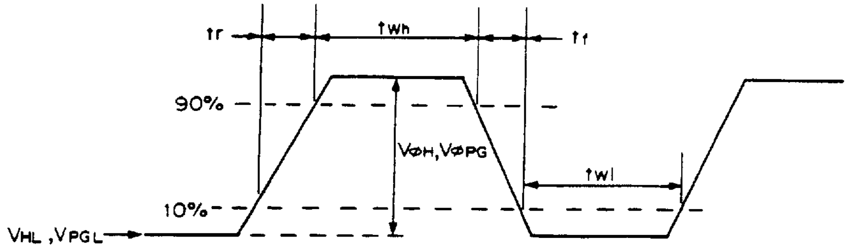


Fig 3

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max		
Read out clock	V_T	1 5	1 85							0 5			0 5	µs	During read out
Vertical transfer clock	$V_{\phi 1}, V_{\phi 2}$ $V_{\phi 3}, V_{\phi 4}$									0 45	0 015		0 25	us	*
Horizontal transfer clock	H_ϕ	37	41		38	42			12	15		10	15	ns	During imaging
Horizontal transfer clock	$H_{\phi 1}$		5 6						0 012			0 01		us	During parallel serial conversion
Horizontal transfer clock	$H_{\phi 2}$					5 6			0 012			0 01		µs	During parallel serial conversion
Precharge gate clock	ϕ_{PG}	15	17		75	81			4			3		ns	
Substrate clock	ϕ_{SUB}	1 5	2 1							0 5			0 5	us	During charge drain

*Note) When vertical transfer clock driver CXD1250 is in use.

4 Substrate clock waveform

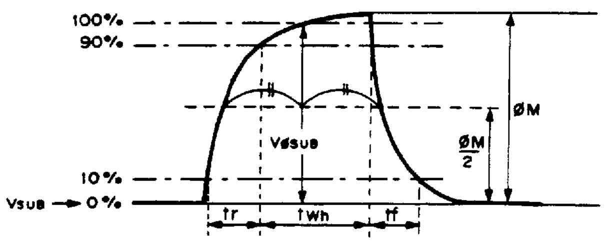


Fig. 4

Operating Characteristics

Ta = 25°C

Item	Symbol	Min	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	240	320		mV	1	
Saturation signal	Vsat	500			mV	2	Ta=55°C
Smear	SM		0.007	0.015	%	3	
Blooming margin		1000			times	4	
Video signal shading	SH			20	%	5	Zone 0 I
				25	%	5	Zone 0 to II'
Dark signal	Vdt			2	mV	6	Ta=55°C
Dark signal shading	ΔVdt			1	mV	7	Ta=55°C
Flicker	F			2	%	8	
Lag	ΔVlag			0.5	%	9	

Test Method

Test conditions

① Through the following tests the substrate voltage should set to the value displayed on the device, while the device drive conditions should be kept within the range of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OPB) is set as the reference. The values obtained at A point in the figure of the Drive Circuit are utilized.

Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/m² 3200K Halogen source), at F8 with a typical test lens, and CM-500S (t=1.0 mm) for IR cut filter.

② Standard imaging condition II: Use a light source with uniformity within 2%, color temperature of 3200K and CM-500S (t=1.0 mm) as IR cut filter. The light intensity is adjusted in accordance with the average signals (V_A) indicated in each item.

1 Set to standard imaging condition I and measure signal output (S) at the center of the screen.

2. Set to standard imaging condition II. Adjust light intensity to 10 times when the average signal V_A=150mV. Then test signal Min. Value.

3. Set to standard imaging condition II. Adjust light intensity to 500 times when the average signal V_A=150mV. Stop Read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the Max. value V_{SM} of signal output.

$$SM = (V_{SM}/V_A) \times 1/500 \times 1/10 \times 100\ (\%) \quad (1/10V)$$

4 Set to standard imaging condition II. Adjust light intensity to 1000 times when the average signal V_A=150mV. Then check that there is no blooming.

5 Video signal shading SH
Set to standard imaging condition II. Test signal Max (V_{max}) and Min (V_{min}) values Adjust light intensity to obtain an average signal (V_A) of about 150mV

$$SH = (V_{max} - V_{min})/V_A \times 100\ (\%)$$

6 Test the average signal when the device ambient temperature is at 55°C and light is obstructed with horizontal idle transfer level as reference

7 Following test 6. test Max (Vd max) and Min (Vd min) of signal output Only keep spot defects out of this range.

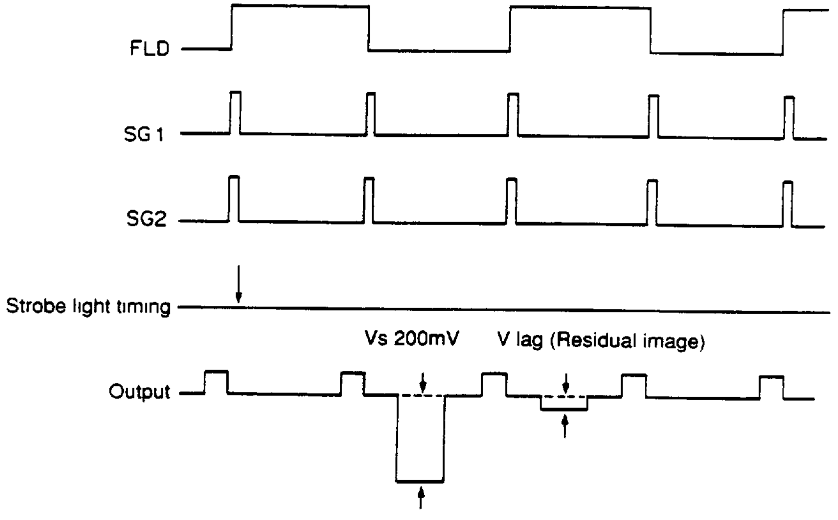
$$\Delta Vdt = Vd\ max - Vd\ min$$

8 Set to imaging condition II Test the output signal difference (ΔVf) between even and odd field At that time. adjust light intensity to obtain an average signal (V_A) of about 150 mV

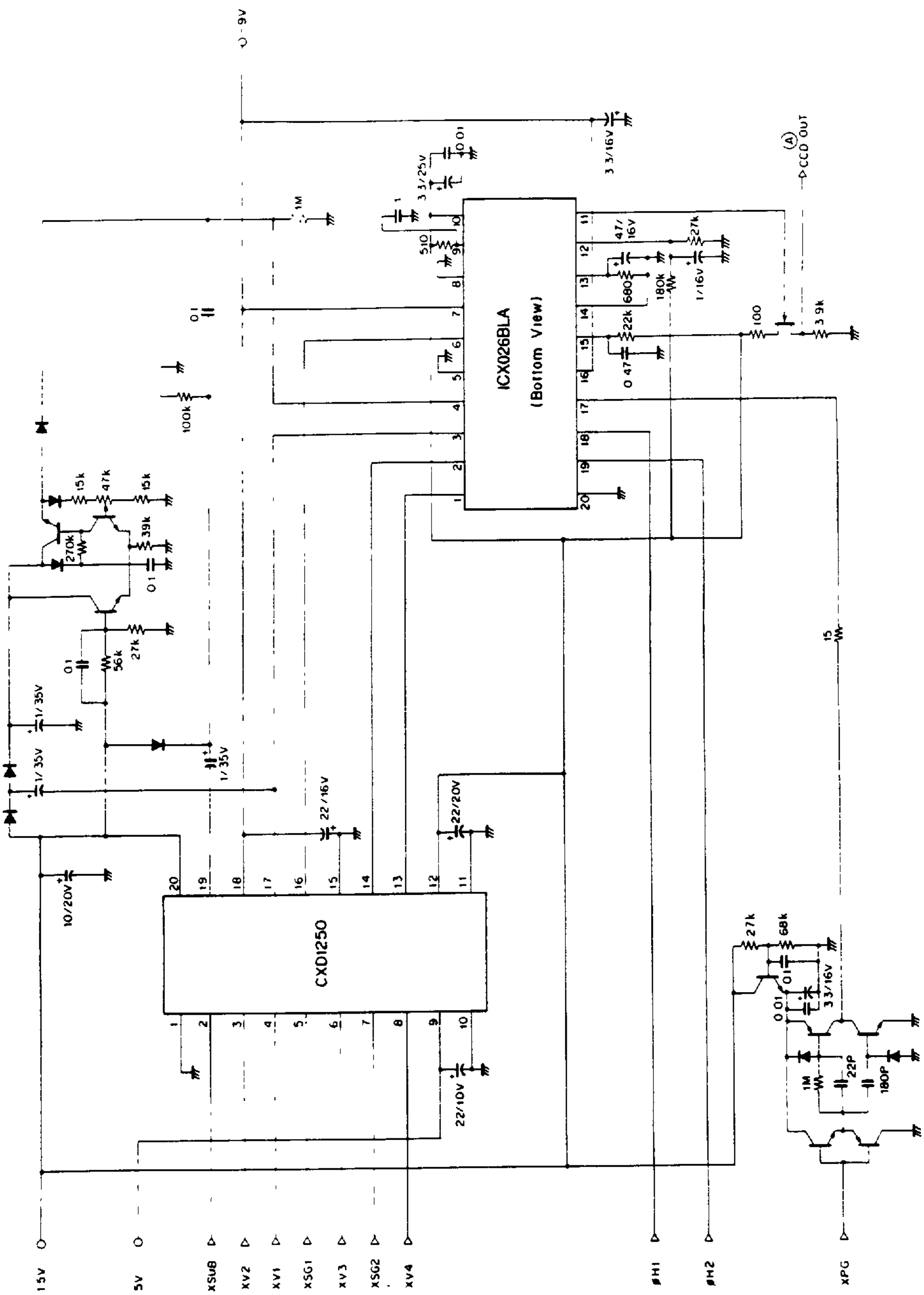
$$F = (\Delta Vf/V_A) \times 100\ (\%)$$

9 Light a stroboscopic tube with the following timing and test the residual image.

$$\Delta Vlag = (Vlag/Vs) \times 100\ (\%)$$

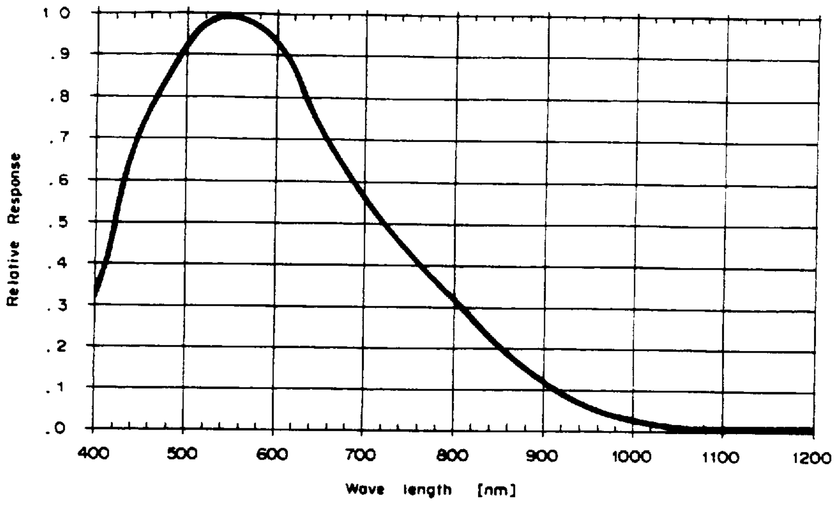


Drive Circuit

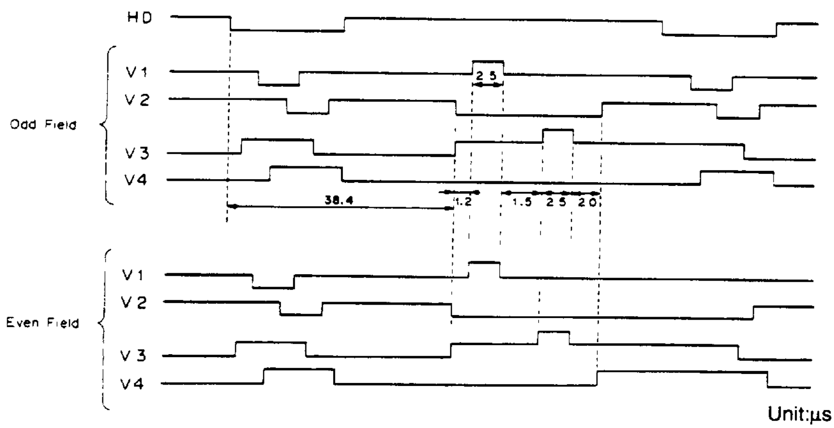


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to the

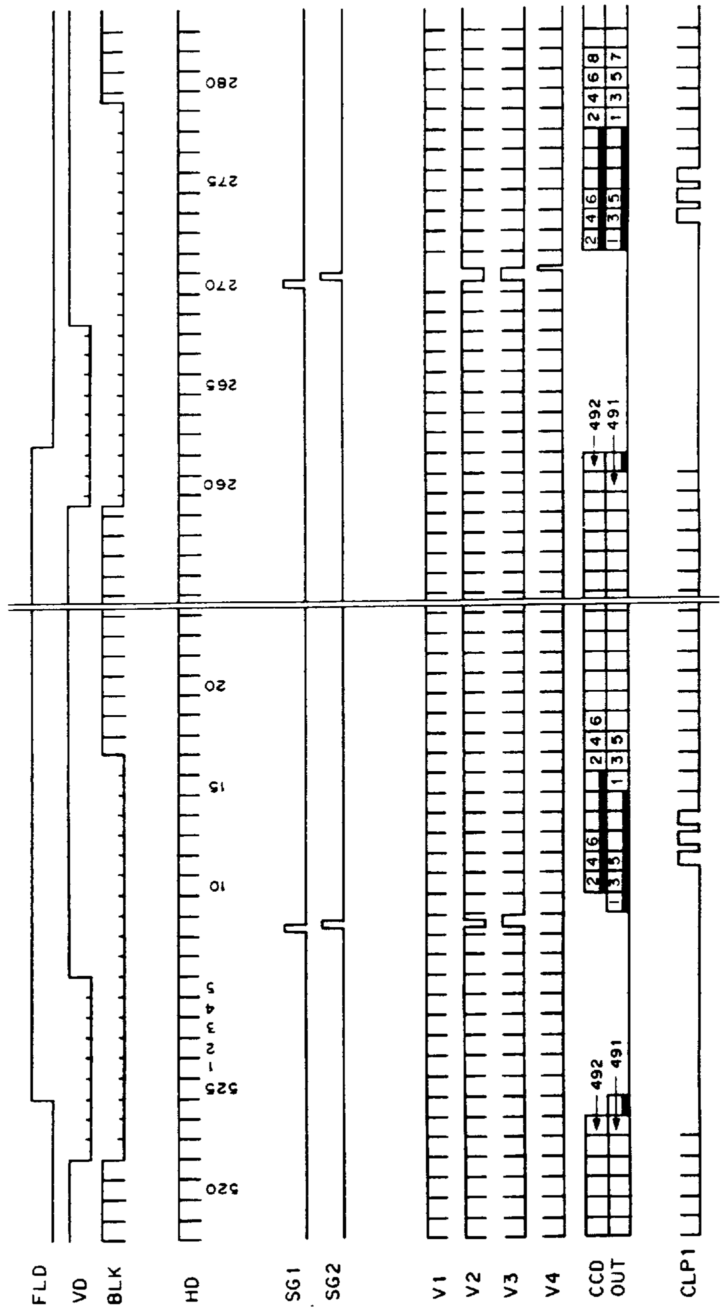
Spectral Sensitivity Characteristics
(Excluding light source characteristics, including lens characteristics)



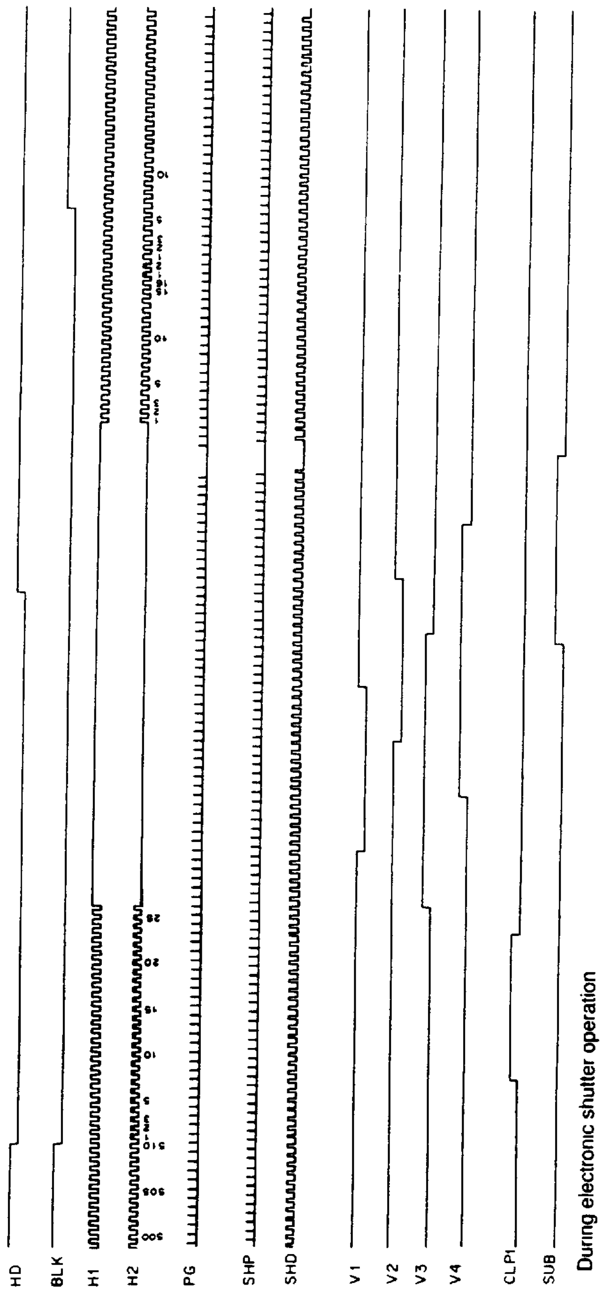
Using read out clock timing chart



Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



Handling Instructions

1) Static charge prevention
CCD image sensor are easily damaged by static discharge. Before handling be sure to take the following protective measures
   a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
   b) When handling directly use an earth band.
   c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
   d) Ionized air is recommended for discharge when handling CCD image sensor.
   e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
   a) Make sure the package temperature does not exceed 80°C.
   b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount cool sufficiently
   c) To dismount an imaging device do not use a solder pult. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
   a) Operate in clean environments (around class 1000 will be appropriate).
   b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
   c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
   d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.