1/3 inch CCD Image Sensor for CCIR B/W Camera

Description

The ICX055AL is an interline transfer CCD solid-state image sensor suitable for CCIR 1/3 inch B/W video cameras. High sensitivity is achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.

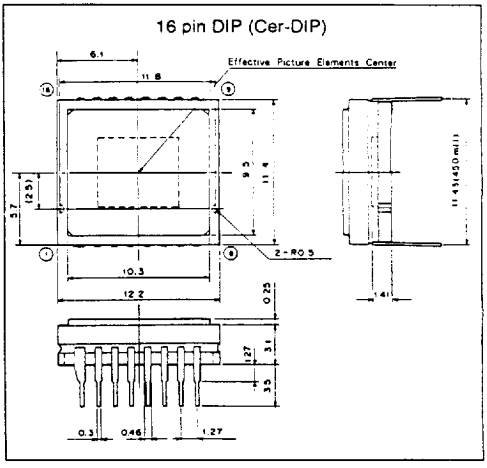
This chip features a field integration read out system, and an electronic shutter with variable charge-storage time and 16 pin small Cer-DIP package.

Features

- High sensitivity (+3dB compare with ICX045BLA) and low dark current
- Consecutive various speed shutter 1/50s. (Typ.), 1/100s to 1/10000s
- Low smear
- High antiblooming
- Horizontal register 5V drive
- Reset gate 5V drive

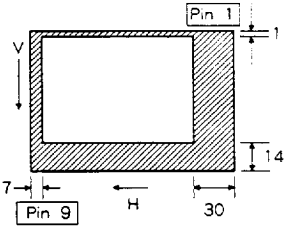
Package Outline

Unit : mm



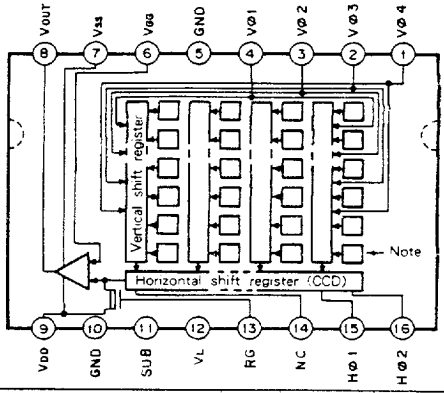
Device Structure

- Optical size 1/3 inch format
- Number of effective pixels
  500 (H) × 582 (V) Approx. 290k pixels
- Number of total pixels
  537 (H) × 597 (V) Approx. 320k pixels
- Interline transfer CCD image sensor
- Chip size 6.0mm (H) × 4.96mm (V)
- Unit cell size 9.8 µm (H) × 6.3 µm (V)
- Optical black Horizontal (H) direction Front 7 pixels Rear 30 pixels
  Vertical (V) direction Front 14 pixels Rear 1 pixels
- Number of dummy bits Horizontal 16
  Vertical 1 (even field only)
- Substrate material silicon



Optical black position (Top View)

Block Diagram
(Top View)



Note) ▭ : Photo sensor

Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	$V\phi_4$	Vertical register transfer clock	9	V_{DD}	Output amplifier drain supply
2	$V\phi_3$	Vertical register transfer clock	10	GND	GND
3	$V\phi_2$	Vertical register transfer clock	11	SUB	Substrate (Overflow drain)
4	$V\phi_1$	Vertical register transfer clock	12	V_L	Protective transistor bias
5	GND	GND	13	RG	Reset gate clock
6	V_{GG}	Output amplifier gate bias	14	NC	
7	Vss	Output amplifier source	15	$H\phi_1$	Horizontal register transfer clock
8	V_{OUT}	Signal output	16	$H\phi_2$	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB-GND		−0.3 to +55	V	
Supply voltage	V_{DD}, V_{OUT}, Vss − GND	−0.3 to +18	V	
	V_{DD}, V_{OUT}, Vss − SUB	−55 to +10	V	
Vertical clock input voltage	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ − GND	−15 to +20	V	
	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$ − SUB	to +10	V	
Voltage difference between vertical clock input pins		to +15	V	*
Voltage difference between horizontal clock input pins		to +17	V	
$H\phi_1$, $H\phi_2$–$V\phi_4$		−17 to +17	V	
$H\phi_1$, $H\phi_2$, RG, V_{GG} − GND		−10 to +15	V	
$H\phi_1$, $H\phi_2$, RG, V_{GG} − SUB		−55 to +10	V	
V_L − SUB		−65 to +0.3	V	
$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$, V_{DD}, V_{OUT}–V_L		−0.3 to +30	V	
RG–V_L		−0.3 to +24	V	
V_{GG}, Vss, $H\phi_1$, $H\phi_2$–V_L		−0.3 to +20	V	
Storage temperature		−30 to +80	°C	
Operating temperature		−10 to +60	°C	

* +27V (Max.) when clock width < 10 µs, duty factor < 0.1%.

Bias Conditions

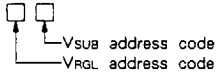
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain voltage	V_{DD}	14.55	15.0	15.45	V	
Output amplifier gate voltage	V_{GG}	1.75	2.0	2.25	V	
Output amplifier source	Vss	Ground through 680 Ω resistor				± 5%
Substrate voltage adjustment range	V_{SUB}	9.0		18.5	V	*1
Fluctuation range after substrate voltage adjustment	Δ V_{SUB}	−3		+3	%	
Reset gate clock voltage adjustment range	V_{RGL}	1.0		4.0	V	*1
Fluctuation range after reset gate clock voltage adjustment	Δ V_{RGL}	−3		+3	%	
Protective transistor bias	V_L	*2				

DC Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Output amplifier drain current	I_{DD}		3		mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*1 Substrate voltage (V_{SUB}) • reset gate clock voltage (V_{RGL}) setting value display.
Setting values of substrate voltage and reset gate clock voltage are displayed at the back of the device through a code address. Adjust substrate voltage (V_{SUB}) and reset gate clock voltage (V_{RGL}) to the displayed voltage. Fluctuation range after adjustment is ± 3%.

V_{SUB} code address–1 digit display
V_{RGL} code address–1 digit display



Code addresses and actual numerical values correspond to each other as follows.

V_{RGL} address code	1	2	3	4	5	6	7
Numerical value	1.0	1.5	2.0	2.5	3.0	3.5	4.0

V_{SUB} address code	E	f	G	h	J	K	L	m	N	P	Q	R	S	T	U	V	W	X	Y	Z
Numerical value	9.0	9.5	10.0	10.5	11.0	11.5	12.0	12.5	13.0	13.5	14.0	14.5	15.0	15.5	16.0	16.5	17.0	17.5	18.0	18.5

<Example> "5L" → V_{RGL}=3.0V
V_{SUB}=12.0V

*2 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform.

*3 1. Current to each pin when 18V is applied to V_{DD}, V_{OUT}, Vss, SUB pins, while pins that are not tested are grounded.
2. Current to each pins when 20V is applied sequentially to V φ 1, V φ 2, V φ 3 and V φ 4, while pins that are not tested are grounded. However, 20V is applied to SUB.
3. Current to each pins when 15V is applied sequentially to pins RG, H φ 1, H φ 2 and V_{GG}, while pins that are not tested are grounded. However, 15V is applied to SUB.
4. Apply 30V to Pins Vφ1, Vφ2, Vφ3, Vφ4, V_{DD}, V_{OUT}; 24V to Pin RG; and 20V to Pins V_{GG}, Vss, Hφ1, Hφ2. The above is the current that flows to Pin V_L when it is grounded. Please note that Pins GND and SUB are to be disconnected.

*4 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

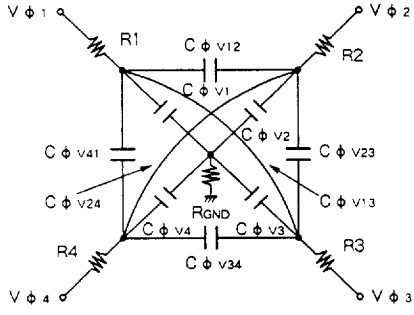
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Read out clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	–0.05	0	0.05	V	2	V_{VH}= (V_{VH1}+V_{VH2}) /2
	V_{VH3}, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	–9.0	–8.5	–8.0	V	2	V_{VL}= (V_{VL3}+V_{VL4}) /2
	V φ V	7.8	8.5	9.05	V	2	V φ V=V_{VHn} – V_{VLn} (n=1 to 4)
	|V_{VH1} – V_{VH2}|			0.1	V	2	
	V_{VH3} – V_{VH}	–0.25		0.1	V	2	
	V_{VH4} – V_{VH}	–0.25		0.1	V	2	
	V_{VHH}			0.5	V	2	High level coupling
	V_{VHL}			0.5	V	2	High level coupling
	V_{VLH}			0.5	V	2	Low level coupling
	V_{VLL}			0.5	V	2	Low level coupling
Horizontal transfer clock voltage	V φ H	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	V φ RG	4.5	5.0	5.5	V	4	*
	V_{RGLH} – V_{RGLL}			0.8	V	4	Low level coupling
Substrate clock voltage	V φ SUB	22.5	23.5	24.5	V	5	

* No adjustment of reset gate clock voltage is necessary when reset gate clock is driven as indicated below. In this case, reset gate clock voltage set point displayed on back of image sensor has no meaning.

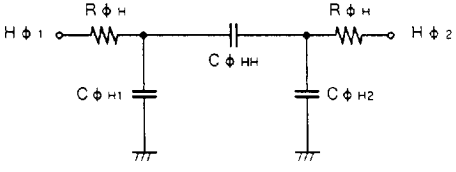
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Reset gate clock voltage	V_{RGL}	–0.2	0	0.2	V	4	
	V φ RG	8.5	9.0	9.5	V	4	

Clock Equivalent Circuit Constant

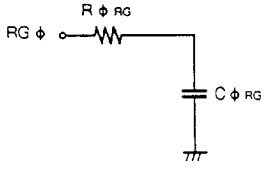
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C\phi_{V1}$, $C\phi_{V3}$		1500		pF	
	$C\phi_{V2}$, $C\phi_{V4}$		820		pF	
Capacitance between vertical transfer clocks	$C\phi_{V12}$, $C\phi_{V34}$		470		pF	
	$C\phi_{V23}$, $C\phi_{V41}$		230		pF	
	$C\phi_{V13}$		150		pF	
	$C\phi_{V24}$		230		pF	
Capacitance between horizontal transfer clock and GND	$C\phi_{H1}$, $C\phi_{H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C\phi_{HH}$		47		pF	
Capacitance between reset gate clock and GND	$C\phi_{RG}$		5		pF	
Capacitance between substrate clock and GND	$C\phi_{SUB}$		320		pF	
Vertical transfer clock serial resistor	R_1, R_3		51		Ω	
	R_2, R_4		100		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R\phi_H$		10		Ω	
Reset gate clock serial resistor	$R\phi_{RG}$		40		Ω	



Vertical transfer clock equivalent circuit



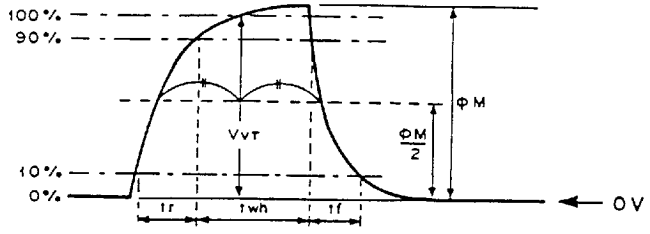
Horizontal transfer clock equivalent circuit



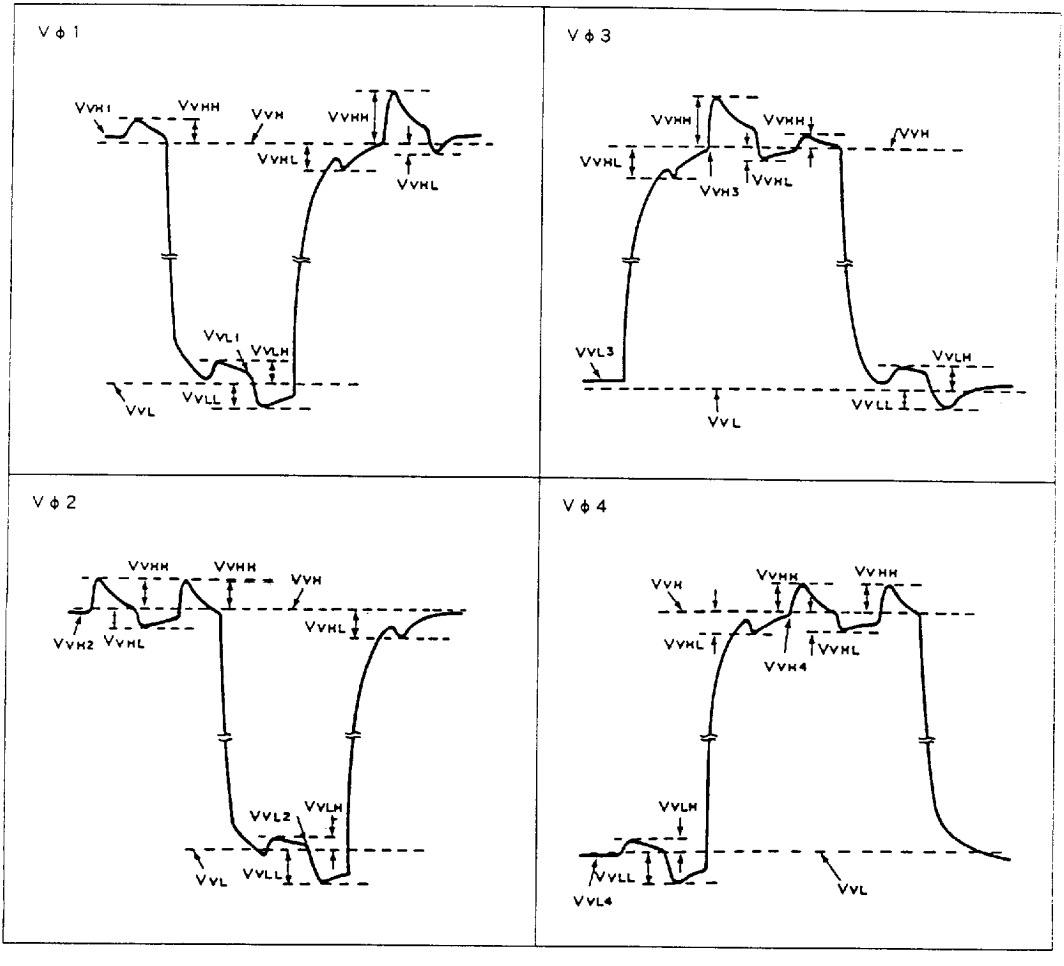
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

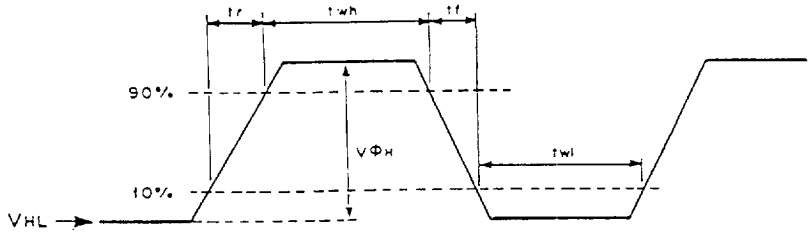
(1) Read out clock waveform



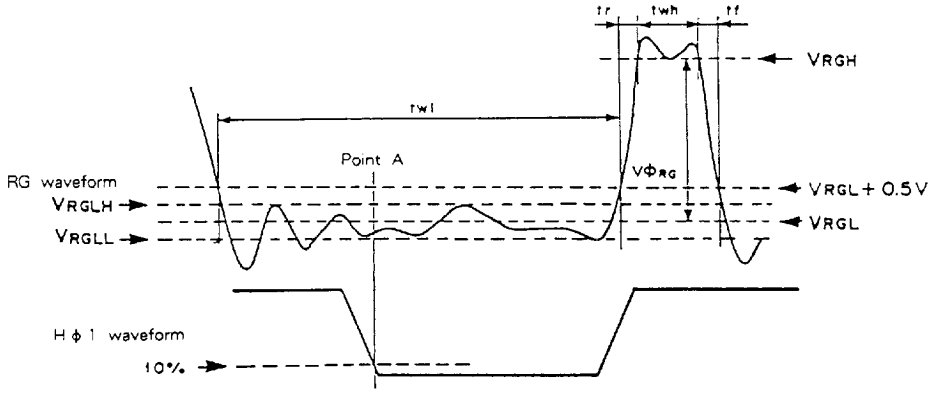
(2) Vertical transfer clock waveform



(3) Horizontal transfer clock waveform diagram



(4) Reset gate clock waveform diagram



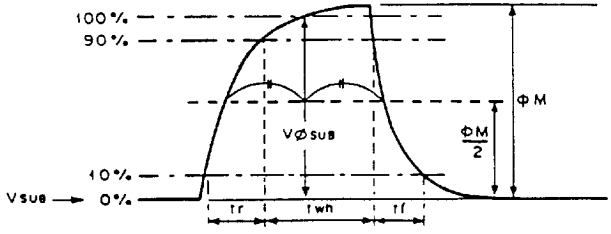
VRGLH is the maximum value and VRGLL the minimum value of the coupling waveform in the period from Point A in the diagram above to RG rise.
VRGL is the mean value for VRGLH and VRGLL.

$$V_{RGL} = (V_{RGLH} + V_{RGLL}) / 2$$

VRGH is the minimum value for twh period.

$$V\phi_{RG} = V_{RGH} - V_{RGL}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Read out clock	V_T	2.3	2.5						0.5			0.5		µs	During read out
Vertical transfer clock	$V\phi_1$, $V\phi_2$, $V\phi_3$, $V\phi_4$										0.015		0.25	µs	*1
Horizontal transfer clock	$H\phi$	37	41		38	42			12	15	*2	10	15	ns	During imaging
Horizontal transfer clock	$H\phi_1$		5.6						0.012			0.012		µs	During parallel serial conversion.
Horizontal transfer clock	$H\phi_2$					5.6			0.012			0.012		µs	
Reset gate clock	ϕ_{RG}	11	15		75	79			6.5			4.5		ns	
Substrate clock	ϕ_{SUB}	1.5	2.0							0.5			0.5	µs	During charge drain.

*1 When vertical transfer clock driver CXD1250 is in use.
*2 tf ≧ tr−2 ns

Image Sensor Characteristics

(Ta=25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Test method	Remarks
Sensitivity	S	420	500		mV	1	
Saturation signal	Vsat	630			mV	2	Ta=60℃
Smear	Sm		0.005	0.007	%	3	
Video signal shading	SH			20	%	4	Zone 0, I
				25	%	4	Zone 0 to II
Dark signal	Vdt			2	mV	5	Ta=60℃
Dark signal shading	Δ Vdt			1	mV	6	Ta=60℃
Flicker Y	F			2	%	7	
Lag	Lag			0.5	%	8	

Zone Chart of Video Signal Shading

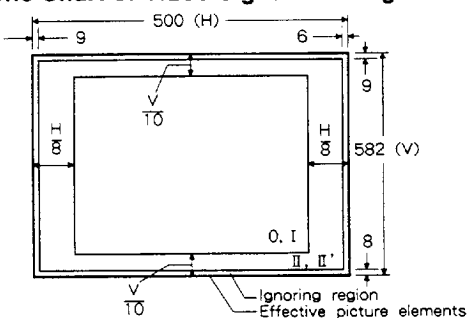


Image Sensor Characteristics Test Method

◎ Test conditions

① Through the following tests the substrate voltage and reset gate clock voltage are set to the value displayed on the device, while the device drive conditions are at the typical value of the bias and clock voltage conditions.

② Through the following tests defects are excluded and, unless otherwise specified, the optical black level (Hence forth referred to as OB) is set as the reference, the values obtained are Ⓐ point in the figure of the Drive Circuit are utilized.

◎ Definition of standard imaging conditions

① Standard imaging condition I: (As imaging device) Use a pattern box (luminance 706 cd/ m^2 , color temperature 3200K Halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter and image at F8.

② Standard imaging condition II: Image a light source (color temperature of 3200K) which uniformity of brightness is within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as IR cut filter. The light intensity is adjusted to the value indicated in each testing item by lens diaphragm.

1. Sensitivity
   Set to standard image condition I. After selecting the electronic shutter mode at a 1/250sec. shutter speed, measure the signal (Vs) at the center of the screen and substitute in the following formula.

   $$S = Vs \times \frac{250}{50} \quad [mV]$$

2. Saturation signal
   Set to standard imaging condition II. Adjust light intensity to 10 times that of signal output average value (V_A=200mV), then test signal minimum value.

3. Smear
   Set to standard imaging condition II. Adjust light intensity to 500 times that of signal output average value (V_A=200mV) with lens diaphragm at F5.6 to F8. Stop read out clock. When the charge drain executed by the electronic shutter at the respective H blankings takes place, test the maximum value VSm [mV] of signal output.

   $$Sm = \frac{VSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100\ (\%)\ (1/10V)$$

4. Video signal shading
   Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=200mV) with lens diaphragm at F5.6 to F8. Then test maximum (Vmax [mV]) and minimum (Vmin [mV]) values of signal.

   SH= (Vmax– Vmin) /200 × 100 (%)

5. Dark signal
   Test signal output average value Vdt [mV] when the device ambient temperature is at 60 ℃ and light is obstructed with horizontal idle transfer level as reference.

6. Dark signal shading
Following 5, test maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of dark signal output.

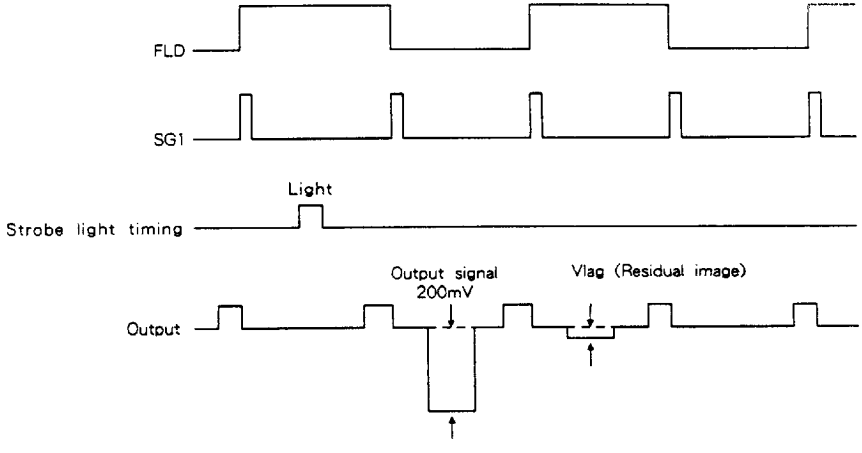
Δ Vdt=Vdmax–Vdmin [mV]

7. Flicker
Set to standard imaging condition II. Adjust light intensity to signal output average value (V_A=200mV). Then test the signal difference (Δ Vf [mV]) between even field and odd field.

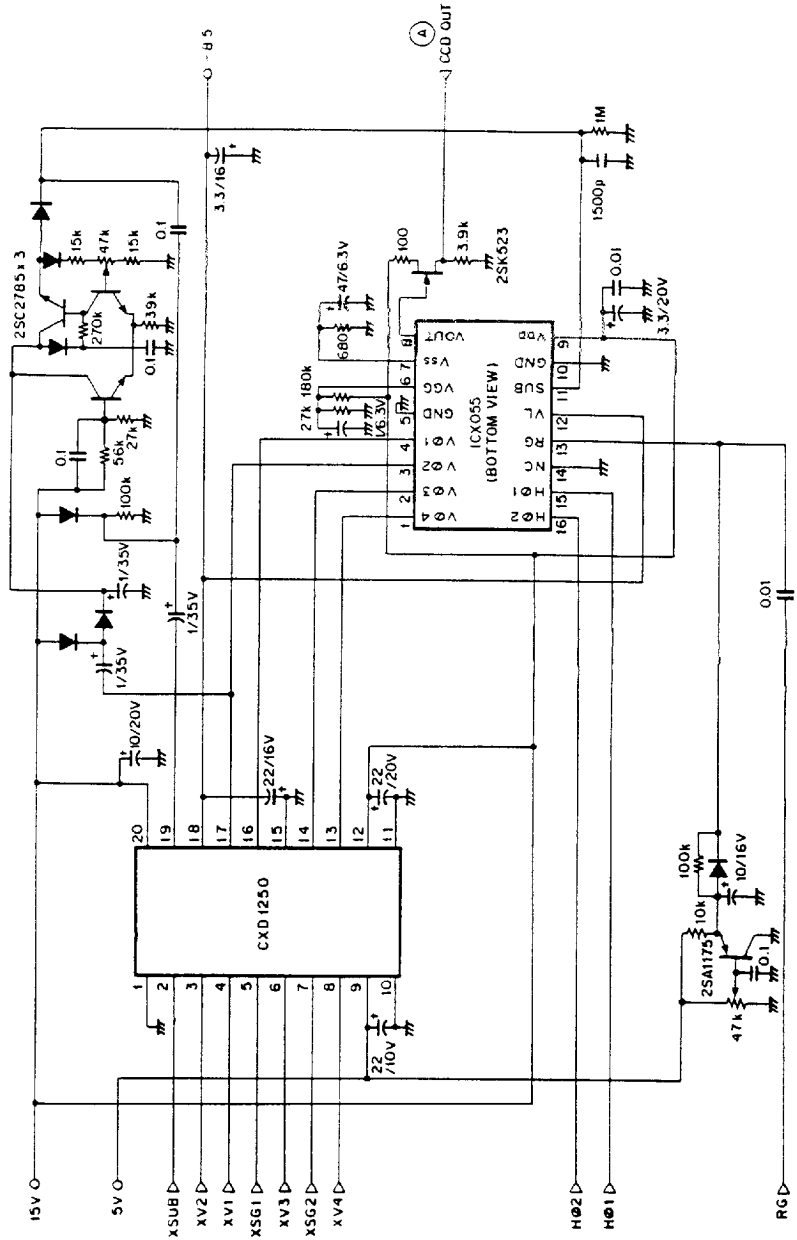
$F = (\Delta Vf/200) \times 100$ (%)

8. Residual image
Adjust signal output value by strobe light to 200mV. Then light a stroboscopic tube with the following timing and test the residual image (Vlag).

Lag = (Vlag/200) × 100 (%)

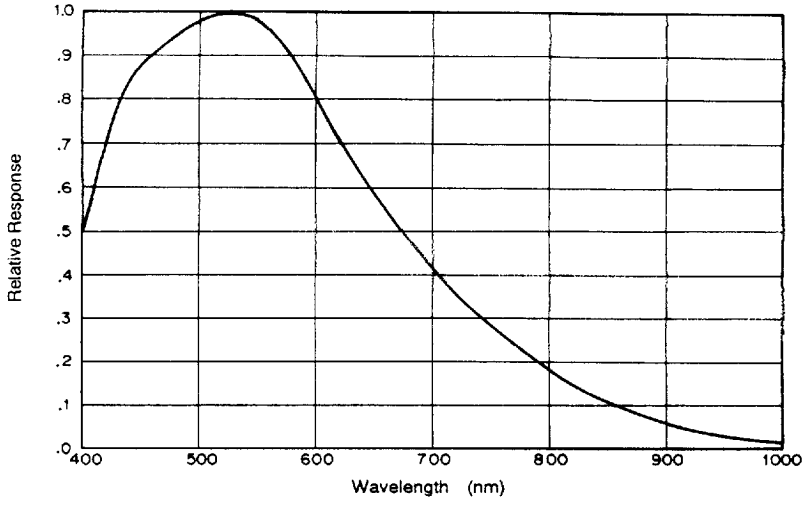


Drive Circuit

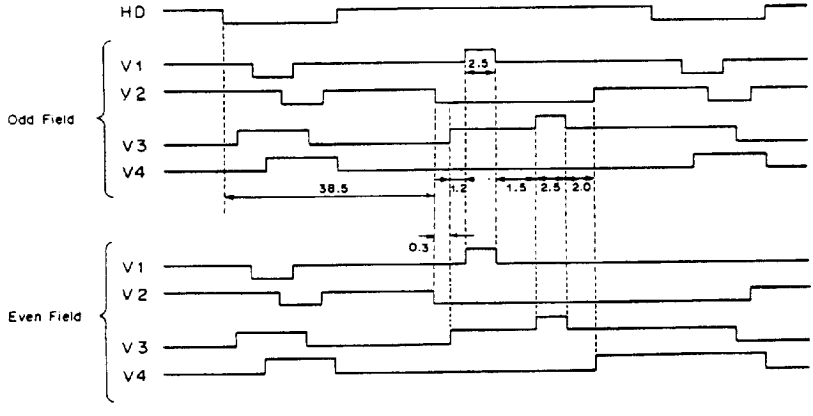


Spectral Sensitivity Characteristics

(Excluding light source characteristics, including lens characteristics)

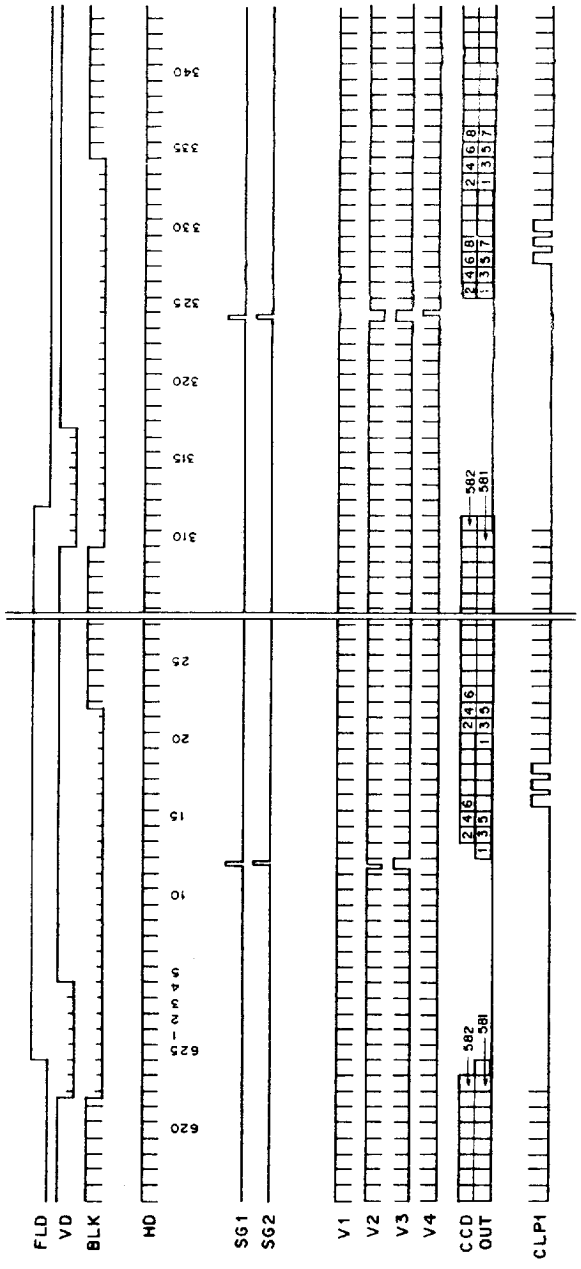


Sensor Read Out Clock Timing Chart

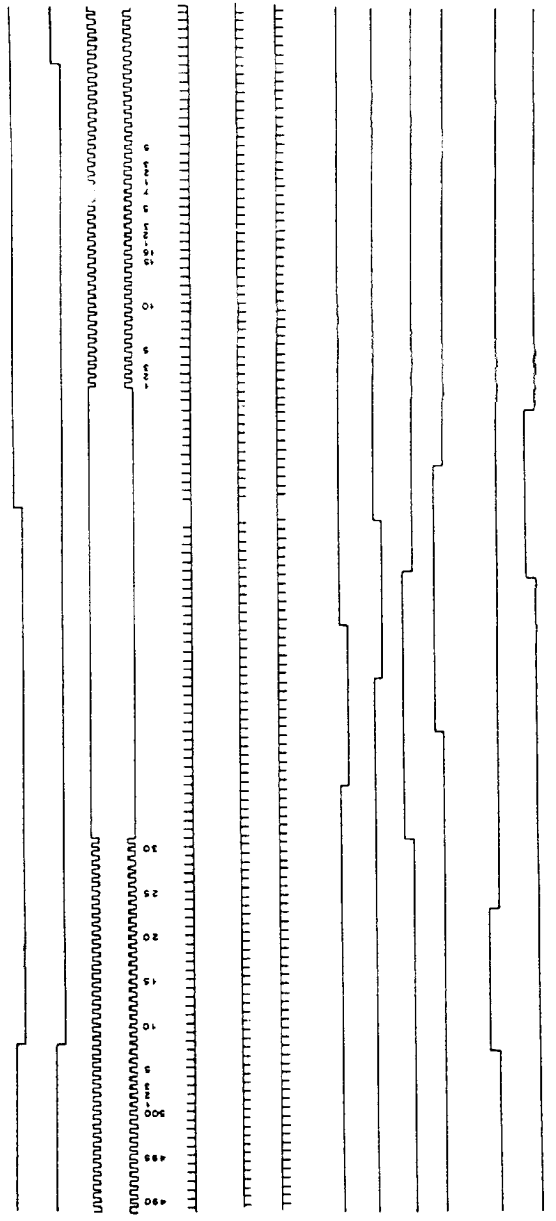


Unit : µs

Drive Timing Chart (Vertical sync)



Drive Timing Chart (Horizontal sync)



(During electronic shutter operation)

Handling Instructions

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band.
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80 °C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently.
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dirt stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air is recommended)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful not to scratch the glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods.

5) Exposure to high temperatures or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensor are precise optical equipment that should not be subject to mechanical shocks.