SONY

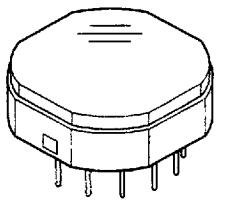
ICX057AKB

1/4-inch CCD Image Sensor for PAL Color Video Camera

Description

The ICX057AKB is an interline transfer CCD solid-state image sensor suitable for PAL 1/4-inch color video cameras. High sensitivity is achieved through the adoption of Ye, Cy, Mg, and G complementary color mosaic filters and HAD (Hole-Accumulation Diode) sensors. This chip features a field integration readout system and an electronic shutter with variable charge-storage time. Also, this outline is miniaturized by using original package.

13 pin PCA (Ceramic)

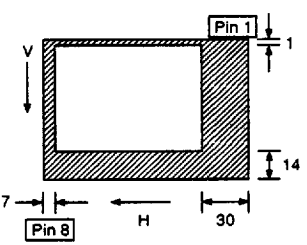


Features

- High sensitivity and low dark current
- Continuous variable-speed shutter
  1/50s (typ.), 1/100s to 1/10000s
- Low smear
- Excellent antiblooming characteristics
- Ye, Cy, Mg, and G complementary color mosaic filters on chip
- Horizontal register: 5V drive
- Reset gate: 5V drive (bias: no adjustment)
- Substrate voltage: 5 to 12.75V

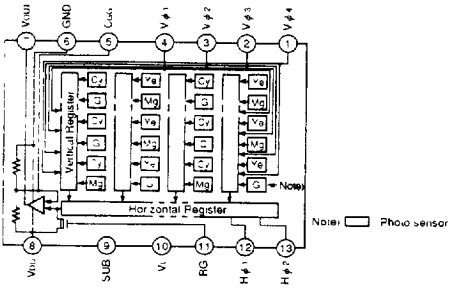
Device Structure

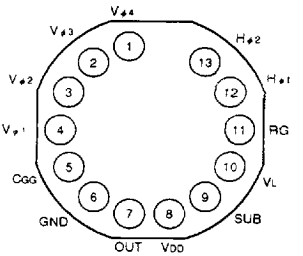
- Optical size 1/4-inch format
- Number of effective pixels
  500 (H)×582 (V) approx. 290K pixels
- Total number of pixels
  537 (H)×597 (V) approx. 320K pixels
- Interline transfer CCD image sensor
- Chip size 4.76mm (H)×4.00mm (V)
- Unit cell size 7.3 μm (H)×4.7 μm (V)
- Optical black: Horizontal (H) direction : Front 7 pixels, Rear 30 pixels
  Vertical (V) direction : Front 14 pixels, Rear 1 pixel
- Number of dummy bits : Horizontal 16
  Vertical 1 (even fields only)
- Substrate material: silicon



Optical black position
(Top View)

Block Diagram and Pin Configuration (Top View)





Pin Description

No.	Symbol	Description	No.	Symbol	Description
1	Vϕ4	Vertical register transfer clock	8	VDD	Supply voltage
2	Vϕ3	Vertical register transfer clock	9	SUB	Substrate (overflow drain)
3	Vϕ2	Vertical register transfer clock	10	VL	Protective transistor bias
4	Vϕ1	Vertical register transfer clock	11	RG	Reset gate clock
5	CGG	Output amplifier gate*1	12	Hϕ1	Horizontal register transfer clock
6	GND	GND	13	Hϕ2	Horizontal register transfer clock
7	VOUT	Signal output			

*1 DC bias is applied within the CCD, so that this pin should be grounded externally through a capacitance of 1 μF or more.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Substrate voltage SUB—GND		−0.3 to +55	V	
Supply voltage	VDD, VOUT, CGG—GND	−0.3 to +18	V	
	VDD, VOUT, CGG—SUB	−55 to +12	V	
Clock input voltage	Vϕ1, Vϕ2, Vϕ3, Vϕ4—GND	−15 to +20	V	
	Vϕ1, Vϕ2, Vϕ3, Vϕ4—SUB	to +12	V	
Voltage difference between vertical clock input pins		to +15	V	*2
Voltage difference between horizontal clock input pins		to +17	V	
Hϕ1, Hϕ2 —Vϕ4		−17 to +17	V	
Hϕ1, Hϕ2 —GND		−10 to +15	V	
Hϕ1, Hϕ2—SUB		−55 to +10	V	
VL—SUB		−65 to +0.3	V	
Vϕ1, Vϕ3, VDD, VOUT—VL		−0.3 to +27.5	V	*3
RG—GND		−0.3 to +22.5	V	
Vϕ2, Vϕ4, CGG, Hϕ1, Hϕ2, GND—VL		−0.3 to +17.5	V	
Storage temperature		−30 to +80	℃	
Operating temperature		−10 to +60	℃	

*2 +27V (Max.) when clock width < 10 μs, clock duty factor < 0.1%.

*3 When CGG or GND are grounded.
−0.3 to +17.5V when CGG and GND are to be disconnected.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.25	15.0	15.75	V	
Substrate voltage adjustment range	V_{SUB}	5.0		12.75	V	*1
Substrate voltage adjustment precision		Indicated voltage −0.1	Indicated voltage	Indicated voltage +0.1	V	
Protective transistor bias	V_L		*2			

DC Characteristics

Item	Symbol	Min.	Typ	Max.	Unit	Remarks
Supply current	I_{DD}		3	5	mA	
Input current	I_{IN1}			1	μA	*3
Input current	I_{IN2}			10	μA	*4

*1 Indications of substrate voltage (V_{SUB}) setting value
The setting value of the substrate voltage is indicated on the back of the device by a special code. Adjust the substrate voltage (V_{SUB}) to the indicated voltage.

V_{SUB} address code—one character indication □
↑
V_{SUB} code

Code and optimal setting correspond to each other as follows.

V_{SUB} code	—	=	0	1	2	3	4	6	7	8	9	A	C	d
Optimal setting	5.0	5.25	5.5	5.75	6.0	6.25	6.5	6.75	7.0	7.25	7.5	7.75	8.0	8.25

V_{SUB} code	E	f	G	h	J	K	L	m	N	P	R	S	U	V
Optimal setting	8.5	8.75	9.0	9.25	9.5	9.75	10.0	10.25	10.5	10.75	11.0	11.25	11.5	11.75

V_{SUB} code	W	X	Y	Z
Optimal setting	12.0	12.25	12.5	12.75

<Example> "L"→ V_{SUB}=10.0V

*2 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*3 1) Current to each pin when 16V is applied to V_{DD}, V_{OUT}, RG, C_{GG}, GND, and SUB pins.

2) Current to each pin when 20V is applied sequentially to $V\phi1$, $V\phi2$, $V\phi3$, and $V\phi4$ pins, while pins that are not tested are grounded. However, 20V is applied to SUB.

3) Current to each pin when 15V is applied sequentially to $H\phi1$ and $H\phi2$ pins, while pins that are not tested are grounded. However, 15V is applied to SUB.

4) Current to V_L pin when 25V is a applied to $V\phi1$, $V\phi3$, V_{DD} and V_{OUT} pins; 15V is applied to $V\phi2$, $V\phi4$, $H\phi1$ and $H\phi2$ pins and the V_L pin is grounded. Please note that GND and SUB pins are to be disconnected.

5) Current to GND pin when 20V is applied to the RG pin and the GND pin is grounded.

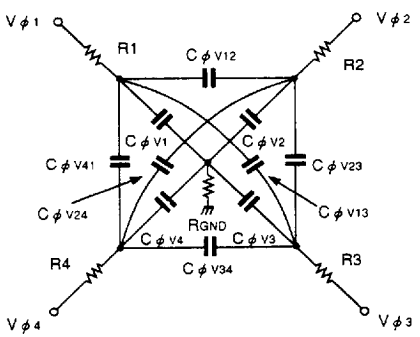
*4 Current to SUB pin when 55V is applied to SUB pin, while pins that are not tested are grounded.

Clock Voltage Conditions

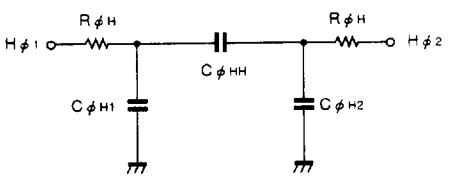
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.25	15.0	15.75	V	1	
Vertical transfer clock voltage	V_{VH1}, V_{VH2}	−0.05	0	0.05	V	2	$V_{VH}=(V_{VH1}+V_{VH2})/2$
	V_{VH3}, V_{VH4}	−0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2}, V_{VL3}, V_{VL4}	−8.5	−8.0	−7.5	V	2	$V_{VL}=(V_{VL3}+V_{VL4})/2$
	$V\phi V$	7.3	8.0	8.55	V	2	$V\phi V=V_{VHn}-V_{VLn}$ (n=1 to 4)
	$V_{VH3}-V_{VH}$	−0.25		0.1	V	2	
	$V_{VH4}-V_{VH}$	−0.25		0.1	V	2	
	V_{VHH}			0.3	V	2	High-level coupling
	V_{VHL}			0.3	V	2	High-level coupling
	V_{VLH}			0.3	V	2	Low-level coupling
	V_{VLL}			0.3	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi H$	4.75	5.0	5.25	V	3	
	V_{HL}	−0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi RG$	4.5	5.0	5.5	V	4	Input through 0.01 μF capacitance
	$V_{RGLH}-V_{RGLL}$			0.8	V	4	Low-level coupling
	V_{RGH}	V_{DD}+0.3	V_{DD}+0.6	V_{DD}+0.9	V	4	
Substrate clock voltage	$V\phi SUB$	21.25	22.5	23.75	V	5	

Clock Equivalent Circuit Constant

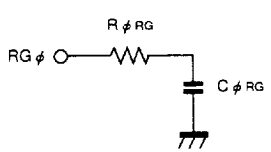
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$ $C_{\phi V3}$		680		pF	
	$C_{\phi V2}$, $C_{\phi V4}$		820		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12}$, $C_{\phi V34}$		180		pF	
	$C_{\phi V23}$, $C_{\phi V41}$		150		pF	
	$C_{\phi V13}$, $C_{\phi V24}$		62		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		30		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		18		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		3		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		190		pF	
Vertical transfer clock serial resistor	R1, R2, R3, R4		33		Ω	
Vertical transfer clock ground resistor	R_{GND}		15		Ω	
Horizontal transfer clock serial resistor	$R_{\phi H}$		24		Ω	
Reset gate clock serial resistor	$R_{\phi RG}$		40		Ω	



Vertical transfer clock equivalent circuit



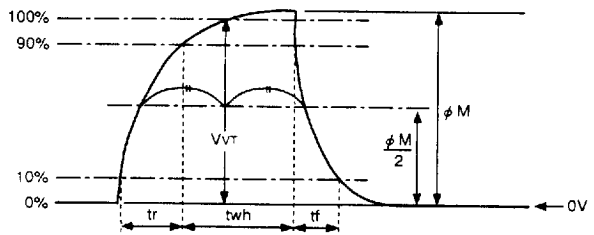
Horizontal transfer clock equivalent circuit



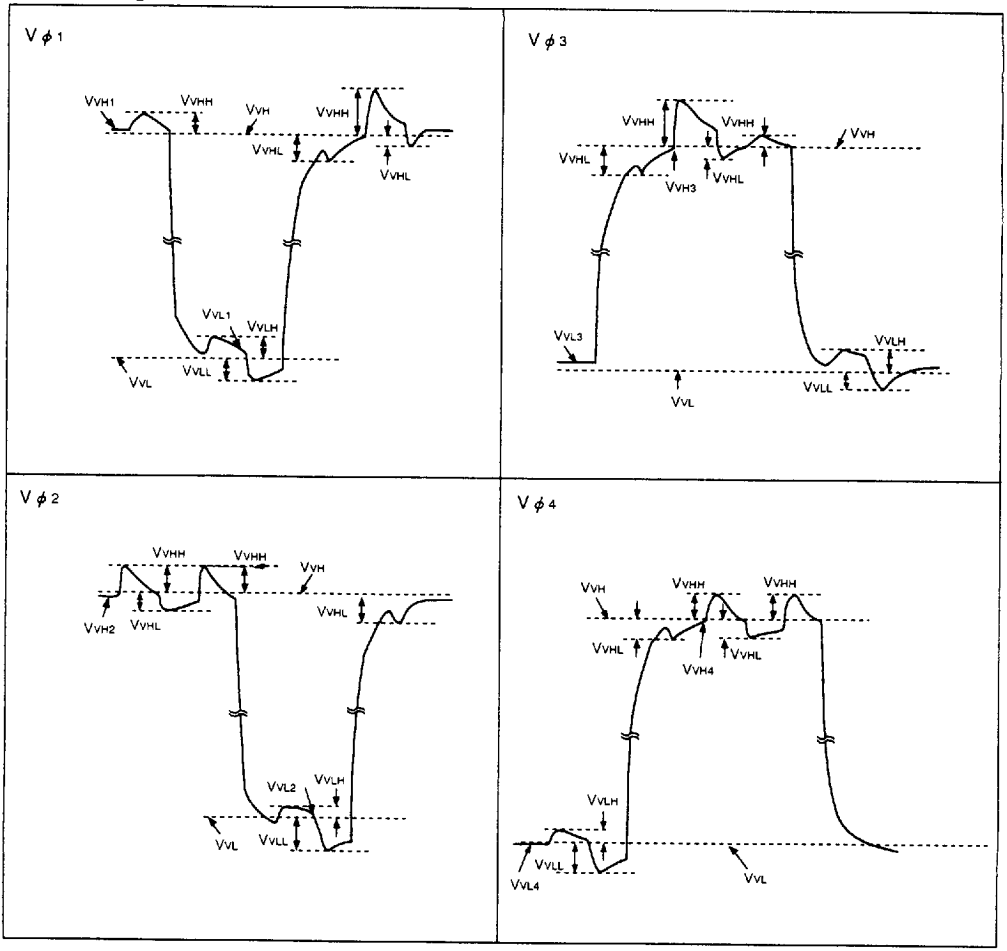
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

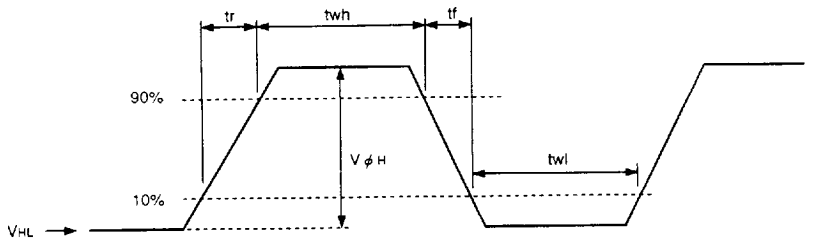
(1) Readout clock waveform



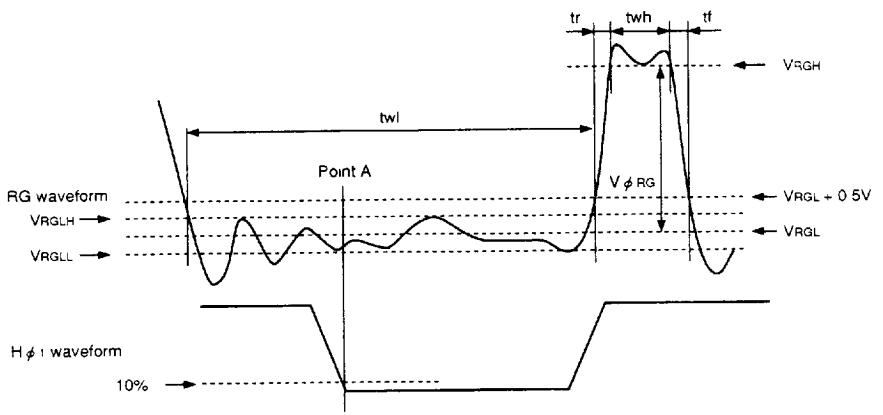
(2) Reset gate clock waveform



(3) Horizontal transfer clock waveform



(4) Reset gate clock waveform



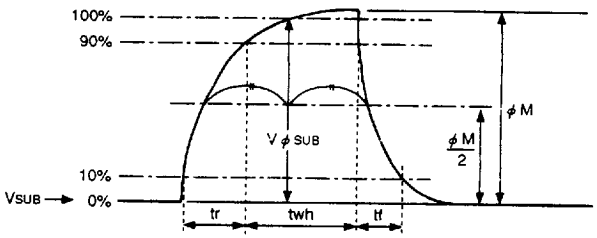
VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG. In addition, VRGL is the average value of VRGLH and VRGLL.

$$V_{RGL}=(V_{RGLH}+V_{RGLL})/2$$

Assuming VRGH is the minimum value during the interval twh, then:

$$V_{\phi RG}=V_{RGH}-\overline{V_{RGL}}$$

(5) Substrate clock waveform



Clock Switching Characteristics

Item	Symbol	twh			twl			tr			tf			Unit	Remarks
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock	VT	2.3	2.5						0.1			0.1		μs	During readout
Vertical transfer clock	Vφ1, Vφ2, Vφ3, Vφ4										0.005		0.25	μs	*1
Horizontal transfer clock	Hφ	41	46		41	46			6.5	9.5	*2	6.5	9.5	ns	During imaging
Horizontal transfer clock	Hφ1		5.6						0.007			0.007		μs	During parallel-serial conversion
Horizontal transfer clock	Hφ2					5.6			0.007			0.007		μs	
Reset gate clock	φRG	11	14		76	80			6.0			5.0		ns	
Substrate clock	φSUB	1.5	1.65							0.5			0.5	μs	During drain charge

*1 When vertical transfer clock driver CXD1267 is used. tr and tf are defined by the rise and fall times for 10% to 90% of the interval between VVL and VVH.

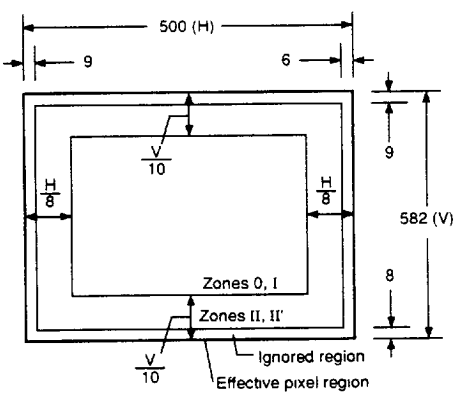
*2 Assumes tr−tf≦2ns.

Image Sensor Characteristics

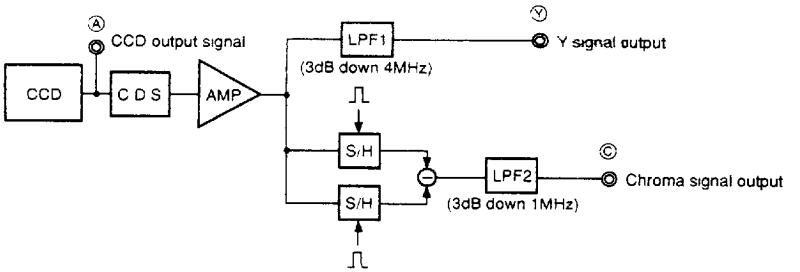
(Ta=25°C)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	290	380		mV	1	
Saturation signal	Ysat	630			mV	2	Ta=60°C
Smear	Sm		0.007	0.01	%	3	
Video signal shading	SHy			20	%	4	Zones 0 and I
				25	%	4	Zones 0 to II
Uniformity between video signal channels	△Sr			10	%	5	
	△Sb			10	%	5	
Dark signal	Ydt			2	mV	6	Ta=60°C
Dark signal shading	△Ydt			1	mV	7	Ta=60°C
Flicker Y	Fy			2	%	8	
Flicker R–Y	Fcr			5	%	8	
Flicker B–Y	Fcb			5	%	8	
Lateral stripes R	Lcr			3	%	9	
Lateral stripes G	Lcg			3	%	9	
Lateral stripes B	Lcb			3	%	9	
Lateral stripes W	Lcw			3	%	9	
Lag	Lag			0.5	%	10	

Zone Definition of Video Signal Shading



Measurement System



Note) Adjust the amplifier gain so that the gain between Ⓐ and Ⓨ, between Ⓐ and Ⓒ equals 1

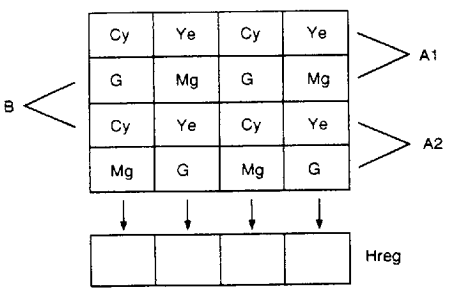
Image Sensor Characteristics Measurement Method

◎Measurement conditions

1) In the following measurements, the substrate voltage is set to the value indicated on the device, and the device drive conditions are at the typical values of the bias and clock voltage conditions.

2) In the following measurements, spot blemishes are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of Y signal output or chroma signal output of the measurement system.

◎Color coding of this image sensor & Composition of luminance (Y) and chroma (C) signals



Color Coding Diagram

As shown in the left figure, fields are read out The charge is mixed by pairs such as A1 and A2 in the A field.
(such pairs as B in the B field)
As a result, the sequence of charges output as signals by the horizontal shift register (Hreg) is, for line A1, (G+Cy), (Mg+Ye), (G+Cy), and (Mg+Ye).

These signals are processed to form the Y signal and chroma signal (color difference signal). The Y signal is formed by adding adjacent signals, and the chroma signal is formed by subtracting adjacent signals. In other words, the approximation:

$$Y=\{(G+Cy)+(Mg+Ye)\}\times 1/2$$
$$=1/2\ \{2B+3G+2R\}$$

is used for the Y signal, and the approximation:

$$R-Y=\{(Mg+Ye)-(G+Cy)\}$$
$$=\{2R-G\}$$

is used for the chroma signal. For line A2, the signals output from Hreg in sequence are

$$(Mg+Cy)-(G+Ye)-(Mg+Cy)-(G+Ye)$$

The Y signal is formed from these signals as follows:

$$Y=\{(G+Ye)+(Mg+Cy)\}\times 1/2$$
$$=1/2\ \{2B+3G+2R\}$$

This is balanced since it is formed in the same way as for line A1. In a like manner, the chroma signal is approximated as follows:

$$-(B-Y)=\{(G+Ye)-(Mg+Cy)\}$$
$$=-\{2B-G\}$$

In other words, the chroma signal can be retrieved according to the sequence of lines from R–Y and –(B–Y) in alternation. This is also true for the B field.

◎Definition of Standard Imaging Conditions

1) Standard imaging condition I : Use a pattern box (luminance 706 cd/m², color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t=1.0mm) as an IR cut filter and image at F5.6. The light intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

2) Standard imaging condition II : Image a light source with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t=1.0mm) as the IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity
Set to standard imaging condition I. After selecting the electronic shutter mode with shutter speed of 1/250 s, measure the Y signal (Ys) at the center of the screen and substitute the value into the following formula.

$$S=Ys \times \frac{250}{50} \text{ [mV]}$$

2. Saturation signal
Set to standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with average value of Y signal output, 200mV, and measure the minimum value of the Y signal.

3. Smear
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity to 500 times the intensity with average value of Y signal output, 200mV. When the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value Y Sm (mV) of the Y signal output and substitute the value into the following formula.

$$Sm=\frac{YSm}{200} \times \frac{1}{500} \times \frac{1}{10} \times 100 \text{ [\%]} \quad \text{(1/10V method conversion value)}$$

4. Video signal shading
Set to standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjust the luminous intensity so that the average value of the Y signal output is 200mV. Then measure the maximum (Ymax [mV]) and minimum (Ymin [mV]) values of the Y signal and substitute the values into the following formula.

$$SHy=(Ymax-Ymin)/200 \times 100 \text{ [\%]}$$

5. Uniformity between video signal channels
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then measure the maximum (Crmax, Cbmax [mV]) and minimum (Crmin, Cbmin [mV]) values of the R–Y and B–Y channels of the chroma signal.

$$\Delta Sr= | (Crmax-Crmin)/200 | \times 100 \text{ [\%]}$$
$$\Delta Sb= | (Cbmax-Cbmin)/200 | \times 100 \text{ [\%]}$$

6. Dark signal
Measure the average value of the Y signal output (Ydt [mV]) with the device ambient temperature 60℃ and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
After measuring 6, measure the maximum (Ydmax [mV]) and minimum (Ydmin [mV]) values of the Y signal output and substitute the values into the following formula.

$\Delta Ydt = Ydmax - Ydmin$ [mV]

8. Flicker
1) Fy
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then measure the difference in the signal level between fields (ϕYf [mV]). Then substitute the value into the following formula.

$Fy = (\Delta Yf/200) \times 100$ [%]

2) Fcr, Fcb
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, insert an R or B filter, and then measure both the difference in the signal level between fields of the chroma signal (ϕCr, ϕCb) as well as the average value of the chroma signal output (CAr, CAb). Substitute the values into the following formula.

$Fci = (\Delta Ci/CAi) \times 100$ [%] (i=r, b)

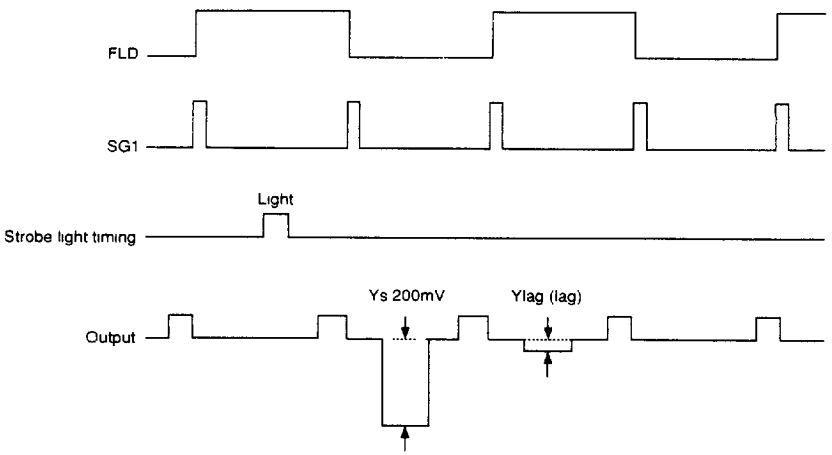
9. Lateral stripes
Set to standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 200mV, and then insert a white subject and R, G, and B filters and measure the difference between Y signal lines for the same field (ϕYlw, ϕYlr, ϕYlg, ϕYlb [mV]). Substitute the values into the following formula.

$Lci = (\Delta Yli/200) \times 100$ [%] (i=w, r, g, b)

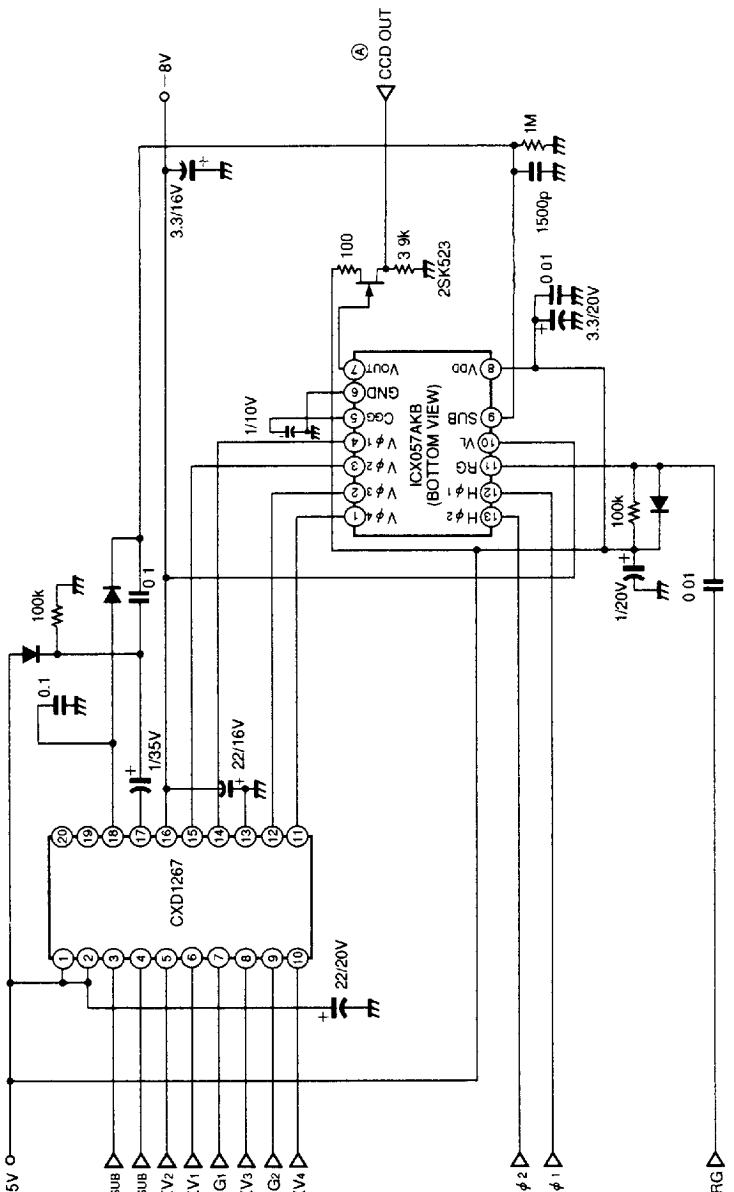
10. Lag

Adjust the Y signal output value generated by strobe light to 200mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Ylag). Substitute the value into the following equation.

Lag = (Ylag/200) × 100 (%)

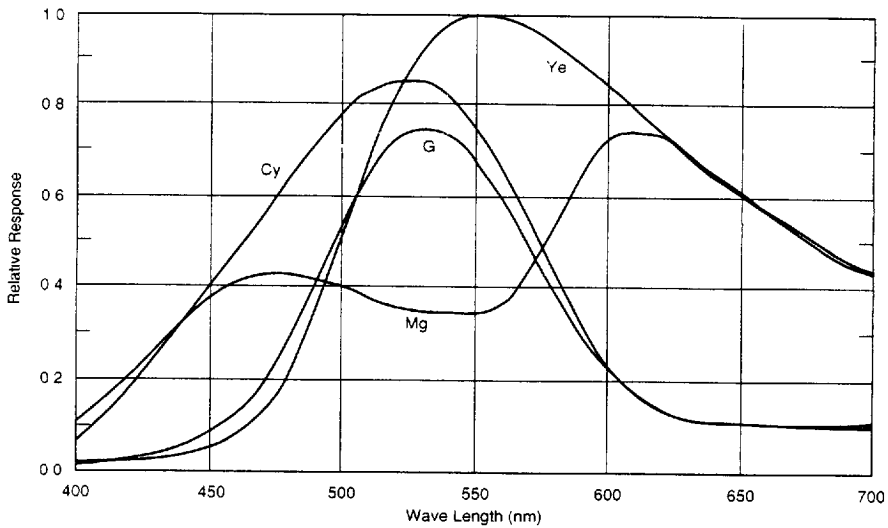


Drive Circuit

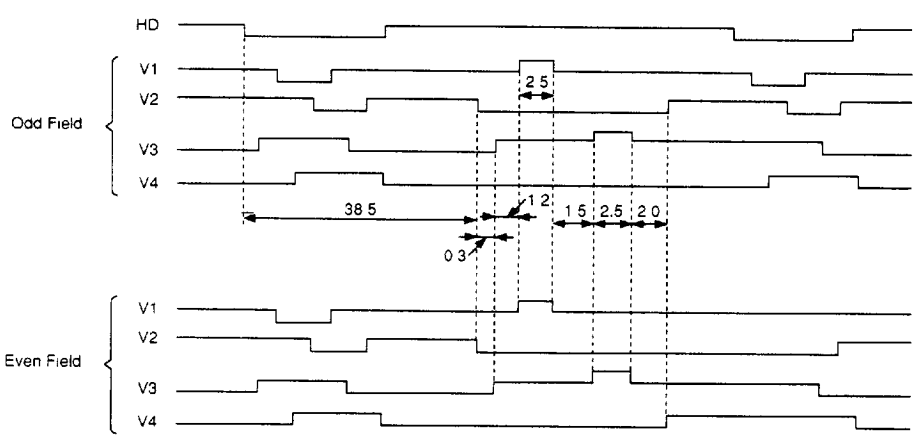


*) For head separate type camera, there are some case where this circuit can not apply.

Spectral Sensitivity Characteristics (includes lens characteristics, excludes light source characteristics)

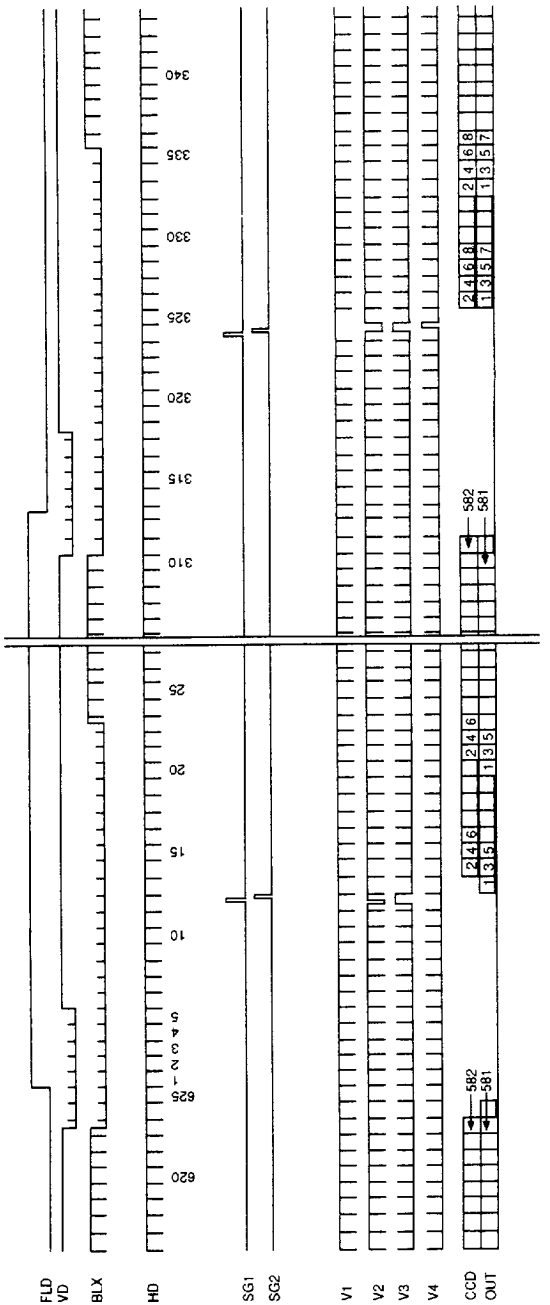


Sensor Readout Clock Timing Chart

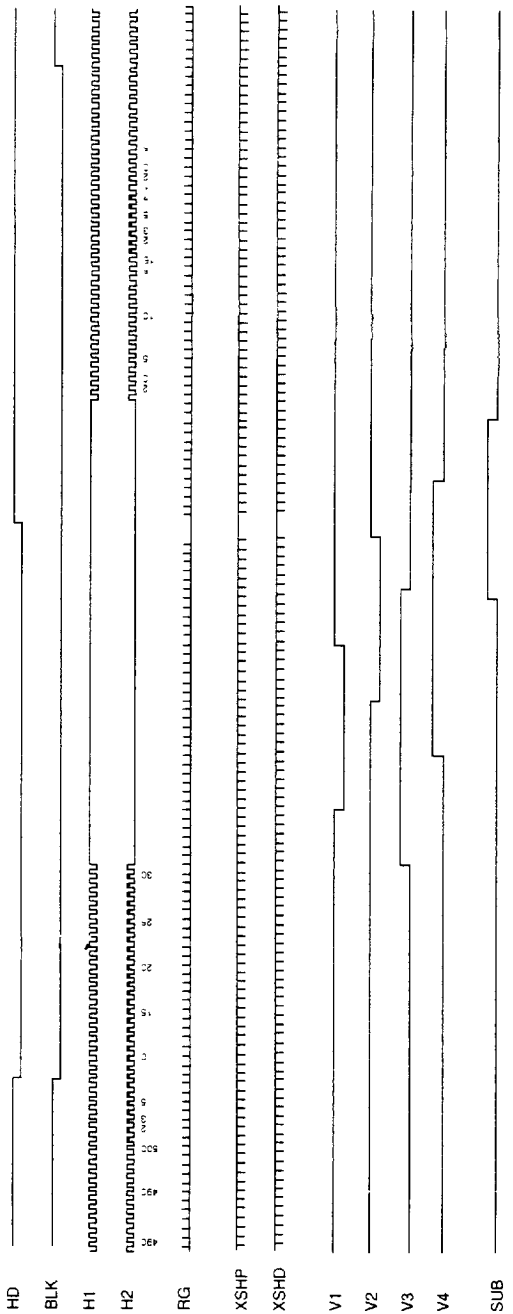


Unit: μs

Drive Timing Chart (Vertical Sync)



Drive Timing Chart (Horizontal Sync)



(During electronic shutter operation)

Notes on Handling

1) Static charge prevention
CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
a) Either handle bare handed or use non chargeable gloves, clothes or material. Also use conductive shoes.
b) When handling directly use an earth band
c) Install a conductive mat on the floor or working table to prevent the generation of static electricity.
d) Ionized air is recommended for discharge when handling CCD image sensor.
e) For the shipment of mounted substrates use boxes treated for the prevention of static charges.

2) Soldering
a) Make sure the package temperature does not exceed 80°C.
b) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a grounded 30W soldering iron and solder each pin in less than 2 seconds. For repairs and remount, cool sufficiently
c) To dismount an imaging device do not use a solder suction equipment. When using an electric desoldering tool use a thermal controller of the zero cross On/Off type and connect to ground.

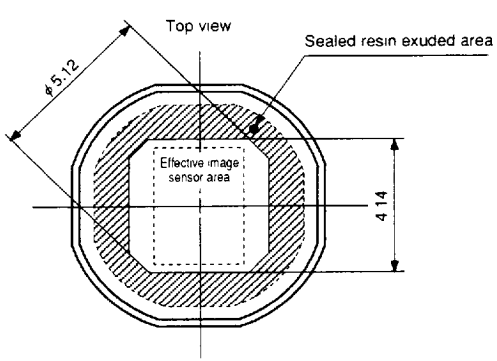
3) Dust and dirt protection
a) Operate in clean environments (around class 1000 will be appropriate).
b) Do not either touch glass plates by hand or have any object come in contact with glass surfaces. Should dir stick to a glass surface blow it off with an air blow. (For dirt stuck through static electricity ionized air recommended.)
c) Clean with a cotton bud and ethyl alcohol if the glass surface is grease stained. Be careful no to scratch th glass.
d) Keep in case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
e) When a protective tape is applied before shipping, just before use remove the tape applied for electrostatic protection. Do not reuse the tape.

4) Do not expose to strong light (sun rays) for long periods, color filters are discolored

5) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or usage in such conditions.

6) CCD image sensors are precise optical equipment that should not be subject to mechanical shocks.

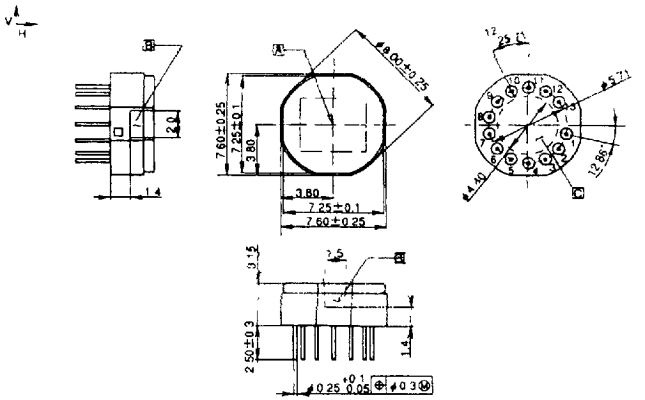
7) Eclipse (to get dark around the four corners of the picture) may occur when some object lenses are in the open iris state.



Package Outline

Unit . mm

13 pin PCA (Ceramic)



PACKAGE STRUCTURE

PACKAGE MATERIAL	Ceramic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	ASTM F15
PACKAGE WEIGHT	0.4g

1. A is the center of the effective image sensor area.
2. Two specified points B are the reference surfaces for horizontal measurements.
3. Specified area C is the reference surfaces for height measurements.
4. The center tolerance of the effective image area specified relative to the center of package* is ±0.15mm.
5. The rotation angle is less ±1° at point B.
6. Height from the bottom surface C to the effective image area is 1.44±0.15mm.
7. Planar orientation of the effective image area relative to the bottom surface C is less than 60μm.
8. Thickness of the cover glass is 0.75mm and the refractive index is 1.5.

* center of package: The center is halfway between the two pairs of opposite sides, as measured from the reference points B.